ARMY TM 11-5820-847-34
NAVY NAVELEX 0969- LP- 169- 5020
AIR FORCE TO 31R5-2G-282

TECHNICAL MANUAL

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL FOR MODEM, DIGITAL DATA MD-1002/G (NSN 5820-01-043-7646)

This copy is reprint which includes current pages from Change 1 and 2

DEPARTMENTS OF THE ARMY, THE NAVY, AND THE AIR FORCE

AUGUST 1977

WARNING
HIGH VOLTAGE
is used in this equipment
DEATH ON CONTACT
may result if safety precautions
are not observed.

115 volts ac is present within the QPSK/BPSK modem. Perform all possible maintenance with power removed. If necessary to perform operations with covers removed and power on, be extremely careful to avoid contact with high voltage.

DON'T TAKE CHANCES!

ARMY TM 11-5820-847-34
NAVELEX 0969-LP-169-5022
AIR FORCE TO 31R5-2G-282
C2

CHANGE
No 2

DEPARTMENTS OF THE ARMY,
THE NAVY, AND THE AIR FORCE
WASHINGTON, DC, *13 April 1982*

Direct Support and General Support Maintenance Manual
MODEM, DIGITAL DATA MD-1002/G
(NSN 5820-01-043-7646)

TM 11-5820-847-34/NAVELEX 0969-LP-169-50201TO 31R5-2G-282, 19 August 1977, is changed as follows:

1. New or changed material is indicated by a vertical bar in the margin of the page
2. Added or revised illustrations are indicated by a vertical bar in front of the figure caption.
3. Remove and insert pages as indicated below.

Remove	*Insert*
i through vi	1 through vi
1-1 through 1-3	1-1 through 1-3
2-1 through 2-6	2-1 through 2-6
2-35 and 2-36	2-35 and 2-36
3-1 and 3-2 .	3-1 and3-2
3-9 through 3-14	3-9 through 3-14
3-19 through 3-40	3-19 through 3-39
3-51 through 3-54	3-51 through 3-54 1
Figure FO-15	Figure FO-15
None	Figure FO-32.1 (1), (Sheet 1 of 2)
None	Figure FO-32.1 (2) (Sheet 2 of 2)
Figure FO-40	Figure FO-40
None	Figure FO-43.1
None	Figure FO-44.1
Figure FO-57	Figure FO-57

4. File this change sheet in the front of the manual for future reference

By Order of the Secretaries of the Army, the Navy, and the Air Force:

E. C. MEYER
General United States Army
Chief of Staff

Official:
ROBERT M. JOYCE
Brigadier General, United States Army
The Adjutant General

H.D. ARNOLD
Rear Admiral, United States Navy
Commander, Naval Electronic Systems Command
LEW ALLEN, JR., *General USAF*
Chief of Staff

Official:
JAMES P. MULLINS
General, USAF, Commander, Air Force Logistics Command

DISTRIBUTION:
To be distributed in accordance with Special Mailing List.

TECHNICAL MANUAL
No 11-5820-847-34
TECHNICAL MANUAL
NAVELEX 0969-LP-169-5020
TECHNICAL ORDER
No 31R5-2G-282

DEPARTMENTS OF THE ARMY,

THE NAVY, AND THE AIR FORCE

WASHINGTON. DC, 19August 1977

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL
MODEM, DIGITAL DATA MD-1002/G
(NSN 5820-01-043-7646)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications-Electronics Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, NJ 07703.

For Air Force, submit AFTO Form 22 (Technical Order System Publication Improvement Report and Reply) in accordance with paragraph 65, Section VI, T.O. 00-5-1. Forward direct to Prime ALCIMST.

For Navy, mail comments to the Commander, Naval Electronics Systems Command, ATTN: ELEX 45053 (O.H.), Washington, DC 20360 In any case, a reply will be furnished direct to you.

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1
INTRODUCTION

1 - 1. Scope

This manual contains the necessary information for troubleshooting, repair and maintenance of Modem, Digital Data MD-1002/G, hereinafter referred to as the QPSK/BPSK modem. Chapter 2 provides a detailed explanation of circuit operation. Direct support troubleshooting and maintenance procedures for the modem are provided in chapter 3, and chapter 4 provides information for general support maintenance. Chapter 5 provides necessary information for the modem power supply, including functional description, maintenance, repair, and troubleshooting. Appendix A contains references and appendix B defines mnemonics used on diagrams.

NOTE

Refer to TM 38-750 for maintenance forms and records, TM 750-244-2 for destruction of Army electronics materiel to prevent enemy use, TM 740-90-1 for administrative storage, DA Pam 310-4 for applicable technical manuals, DA Pam 310-7 for current modification work orders, and to TM 11-5820-847-12, paragraph 1-6, for reporting equipment improvement recommendations

1 - 2. Equipment Designators

Throughout this manual, assemblies and subassemblies are identified by reference designation; e.g., A2A1, A2A2, etc. These designators are the same as those marked on the equipment. The maintenance allocation chart in TM 11-5820-847-12 and the repair parts and special tools lists in TM 11-5820-847-20P and -34P are, however, organized in functional group code (FGC) sequence. To facilitate use of all equipment documentation, a reference designation to functional group code cross-reference index is provided in table 1-1.

Table 1-1. Reference Designation/FGC Cross-Reference

Reference designator	Name	Assembly number	FGC
	Modem, Digital Data MD- 1002/ G	SM-D-877605	00
A1	Control Panel	SM-D-877611	01
A1A1	Switch Assembly, Input Data Rate	SM-D-742008	0101
A1A2	Switch Assembly, I Channel Symbol Rate	SM-D-742008	0102
A2	RF Modem and Bit Sync Assembly	SM-D-877607	02
A2A1	QPSK/BPSK Data Receiver and Modulator	SM-D-877650	0201
A2A2	70-MHz Oscillator	SM-D-731193	0202
A2A4	Quantizer, Phase Channel	SM-D-731213	0203
A2A5	Dump Circuit, Phase Channel	SM-D-731209	0204
A2A6	Integrator, Phase Channel	SM-D-731205	0205
A2A8	Quantlzer, I Channel	SM -D-731213	0206
A2A9	Dump Circuit, I Channel	SM-D-731209	0207
A2A10	Integrator, I Channel	SM-D-731205	0208
A2A12	Data Detector and Driver, I Channel	SM-D-731173	0209
A2A14	Phase Adjust and Detector Driver	SM-D-877680	0210
A2A16	70-MHz Gain Control Amplifier	SM -D-877675	0211
A2A18	Filters and Distribution Amplifier	SM-D-877645	0212
A2A19	Coherent Detector and AGC Loop Amplifier	SM-D-877665	0213
A2A20	X2/X4 Multiplier	SM-D-877660	0214
A2A22	Reference X2/X4 Multiplier	SM-D-877655	0215
A2A24	Phase Lock Loop Amplifier and Sweep Circuit	SM -D-877670	0216
A2A26	Modulation Filter	SM-D-731185	0217
A2A27	70-MHz Output Amplifier	SM-D-731189	0218
A2A29	Bit Sync Buffer	SM-D-877695	0219

Table 1-1 Reference Designation/FGC Cross-Reference-Continued

Reference designator	Name	Assembly number	FGC
A2A30	Timing and AGC, Q Channel	SM-D-877930 or SM-D-731229	0220
A2A31	Timing and AGC, I and Phase Channel	SM-D-877930 or SM-D-731229	0221
A2A32	Quantlzer, Q Channel	SM-D-731213	0222
A2A33	Dump Circuit, Q Channel	SM-D-731209	0223
A2A34	Integrator, Q Channel	SM-D-731205	0224
A2A35	Quadrature Detector	SM-D-877690	0225
A2A36	.Data Detector and Driver, Q Channel	SM-D-731173	0227
A2A47	Acquisition Control	SM-D-877935 or SM-D-877685	0226
A3	Interface and Bit Synchronizer Assembly	SM-D-877609	03
A3A2	LOS/Cable Receiver and Decoder	SM-D-742089	0301
A3A4	LOS/Cable Driver	SM-D-742081	0302
A3A5	Input Interface	SM-D-742037	0303
A3A6	Encoder Switch	SM-D-877730	0304
A3A7	Decoder Switch	SM-D-877700	0305
A3A8	Test Interface	SM-D-877705	0306
A3A9	11-Bit PN Sequence Generator	SM-D-742057	0307
A3A10	Error Comparator	SM-D-742061	0308
A3A1	D/A Meter	SM-D-877725	0309
A3A12	Alarm Circuits	SM-D-742033	0310
A3A13	Phase and Loss of Lock Detector	SM-D-877926 or SM-D-731225	0311
A3A14	Loop Filter	SM-D-731221	0312
A3A15	D/A Converter, Receive	SM-D-731217	0313
A3A16	Counter Encoder, Receive	SM-D-742105	0314
A3A17	Programmable Divider, Receive	SM-D-742109	0315
A3A18	Reference Divider, Receive	SM-D-742133	0316
A3AI9	Reference Oscillator, Receive	SM-D-742129	0317
A3A21	15-MHZ Amplifier, Receive	SM-D742121	0318
A3A22	Mixer/Output Amplifier, Receive	SM-D-742125	0319
A3A23	45-MHz Amplifier, Receive	SM-D-742117	0320
A3A24	45-MHz Phase Lock Loop, Receive	SM-D-742113	0321
A3A27	Encoder Interface	SM-D-742049	0322
A3A28	Decoder Interface	SM-D-742049	0323
A3A29	Line Driver, Stable Clock	SM-C-742053	0324
A3A30	Line Driver, Alternate	SM-D-742053	0325
A3A31	Line Driver, Standard	SM-D-742053	0326
A3A32	Relay Control	SM-D-877710	0327
A3A33	Randomizer/Derandomizer	SM-D-877780	0341
A3A35	Transmit Bit Detector	SM-D-742045	0328
A3A36	Loop Filter	SM-D-731221	0329
A3A37	D/A Converter, Transmit	SM-D-731217	0330
A3A38	Reference Divider, Stable Clock	SM-D-742133	0331
A3A39	Stable Clock	SM-D-731201	0332
A3A40	Counter Encoder, Transmit	SM-D-742105	0333
A3A41	Programmable Divider, Transmit	SM-D-742109	0334
A3A42	Reference Divider, Transmit	SM-D-742133	0335
A3A43	Reference Oscillator, Transmit	SM-D-742129	0336
A3A45	15-MHz Amplifier, Transmit	SM-D-742121	0337
A3A46	Mixer/Output Amplifier, Transmit	SM-D-742125	0338
A3A47	45-MHz Amplifier, Transmit	SM-D-742117	0339
A3A48	45-MHz Phase Lock Loop, Transmit	SM-D-742113	0340
B1	Blower	SM-A-731252	04
B2	Blower	SM-A-731252	05
PS1	Power Supply Assembly	SM-C-742003	06
PS1	Power Supply	SM-D-882227	0601
PS1A1	Transformer Assembly	SM-C-882244	060101
PS1A2	Printed Circuit Board	SM-D-882232	060102
PS1A3	Circuit Card Assembly	SM-C-882239	060103
PS1A4	Component Board Assembly Number 1	SM-C-882245	060104
PS1AS	Component Board Assembly Number 2	SM-D-882247	060105
PS1A6	Heat Sink Assembly Number 1	SM-D-882249	060106

Table 1-1. Reference Designation/FGC Cross-Reference-Continued

Reference designator	Name	Assembly number	FGC
PS1A7	Heat Sink Assembly Number 2	SM-D-882251	060107
PS1A8	Heat Sink Assembly Number 3	SM-D-882253	060108
PS1A9	Terminal Board Assembly	SM-C-882255	060109
PS1A10	Rectifier Assembly	SM-C-882257	060110
W1	Cable	SM-D-877639	07
W2	Cable	SM-D-877640	08
W3	Cable	SM-D-877641	09
W4	Cable	SM-D-877631	10
W5	Cable	SM-D-877632	11
W6	Cable	SM-D-877634	12
W7	Cable	SM-D-877642	13
W8	Cable	SM-D-759619	14
W9	Cable	SM-C-742193	15
W10	Cable	SM-C-742193	16
WI11	Cable	SM-D-877643	17
W12	Cable	SM-D-877634	18
Y1	VCO, Transmit	SM-A-731369-1	19
Y2	VCO, Receive	SM-A-731369-1	20

1-3. Differences in Equipment

In MD-1002/G, procured on Contract DAAK80-79-C-0289 (Hams Corp), the following equipment changes were affected.

a. In integrator cards (SM-D-731205), R14, R22, R31, and R35 (fig 3-14B) are 12-turn potentiometers in place of 3/4-turn potentiometers (fig 3-14A).

b. In timing and AGC cards (SM-D-877930), R4 and R19 (fig. 3-13B) are 12-turn potentiometers In place of 3/4-turn potentiometers (SM-D-731229) (fig 3-13A).

c. In quantizer card (SM-D-731213), a test point is provided on the top of the card (fig. 3-15) for the test troubleshooting VR1 and VR2.

d. In phase and loss of lock detector (old card SM-D-731225, fig. FO-43; new card SM-D-877926, fig FO-43.1) part numbers for U1 and U5 were changed. In timing and AGC (old card SM-D-731229, fig. FO-44; new card SM-D-877930, fig. FO-44.1) R27 was added and part numbers for R9, U2, U3, U7, U8, and U10 were changed.

e. In oscillators Y1 and Y2, the adjustment controls (fig. 3-22.1) are mounted opposite to that on the original position (fig. 3-22) for ease in access to controls.

f. On the power cable (SM-C-759676), a warning label is attached to indicate it should only be used with the MD-1002/G, MD-920A/G, MD-921/G, KY-801/GSC and MX-9922/G.

g. On the top and bottom covers of the MD-1002/G, a warning is inscribed which warns against operating the equipment without covers.

h. The MD-1102/G is issued with the following parts (appendix B, TM 11-5820-847-12):.

(1) Ac power cord. SM-C-759676 (1 ea)
(2) Connector: MS-3126E24-61P (1 ea)
(3) Connector: MS-3126E24-61PW (1 ea)
(4) Chassis Slide Halves. 11OQDJ-20-A-2 (2 ea)
(5) Card extender: SM-D-759649 (1 ea)
(6) Card extender: SM-D-877735 (1 ea)
(7) Card extractor: SM-A-878030-1 (1 ea)
(8) Card extractor: SM-A-878030-2 (1 ea)
(9) Strain relief- SM-A-731358-2 (2 ea)

Items (2), (3), (4), and (9) are used to install the MD-1002/G in an equipment rack. Items (5) through (8) are used for maintenance.

CHAPTER 2
FUNCTIONING OF EQUIPMENT

2-1. General.

a. This chapter contains a description of the functioning of the QPSK/BPSK modem. A functional block diagram description of the entire modem is followed by detailed descriptions of each functional block in the modem. The supporting detailed card descriptions are grouped by function, i e., bit synchronizer, demodulator, etc.

b. Supporting illustrations such as block diagrams and timing diagrams are included within this chapter. An illustration defining resistor, capacitor, and inductor markings is included as figure FO-1

c. The modem power supply functional description is contained in chapter 5.

2-2. Functional Description.

a. General. The QPSK/BPSK modem (fig. 2-1) provides a means of interfacing digital data over an RF communications link by converting baseband data signals to modulated 70-MHz signals (transmit) and converting modulated 70-MHz signals to baseband data (receive). The modem will process data at any rate between 16 kb/s and 9.9999 Mb/s. Self-test, link test, and on-line fault monitoring functions are built into the modem External error-correcting coders/decoders can be employed if required to improve the quality of communications. The modem has independent transmit and receive sections The transmit section accepts a baseband data input and provides either a biphase shift keying (BPSK) or a quadra-phase shift keying (QPSK) modulated 70MHz output. The receive section accepts a noisy BPSK or QPSK modulated 70-MHz input and provides baseband data and reconstructed clock outputs.

b. Input Circuits. The input digital data is accepted through either the LOS/cable inputs from remote users or the standard digital inputs from local users. If used, the LOS/cable input interface compensates and conditions data from a remote user at the other end of an LOS microwave link or a shielded cable. Input selection and circuit functions are described in detail in paragraph 2-3.

c. Transmit Bit Synchronizer/Clock Synthesizer. The purpose of the bit synchronizer is two-fold; derive data clock (timing) for those data streams from the input circuits that do not have an accompanying clock signal, and to smooth any input phase jitter or bit distortion of the input signal. The clock synthesizer allows the transmit bit synchronizer to operate at any five-digit input data rate from 16.000 kb/s to 9.9999 Mb/s. The bit sync/synthesizer form a phase lock loop that acquires the input data with rate offsets (actual rate compared to INPUT DATA RATE switch setting) of over 250 parts per million, and derives both bit rate and twice bit rate clock signals for use in the processing circuits. The phase lock loop also provides the phase jitter and data bit distortion smoothing. The clock input from the digital user can also be selected as the source for the bit synchronizer. An advantage of using the clock as an input is that it always has maximum transition density, providing the transmit bit synchronizer with the highest possible number of phase updates to the phase lock loop. The input data is then retimed by the smoothed clock signal, thus removing distortion from the input data. The bit synchronizer and clock synthesizer controls and circuit functions are described in detail in paragraphs 2-4 and 2-5.

d. Coder and Interface.

(1) The nature of BPSK and QPSK modulation results in an ambiguity between digital ONE's and ZERO's in the detected data stream This ambiguity results because at the receive end of the communications link it is impossible to tell the absolute value of phase of the received signal To eliminate this ambiguity, differential encoding of the input data is provided.In the differential encoder, the standard nonreturn to zero-level (NRZ-L) code (the logic ONE/ZERO information is represented by different levels) is converted to an equivalent NRZ-M (mark) code (the logic ONE/ZERO information is represented by a transition or no transition). The differential decoder in the receive side reconverts the code to NRZ-L.

(2) An interface through high-speed, current mode, balanced line drivers and receivers is provided between the modulator/encoder and an external error correcting coder. This permits selection of high gain coders when required. All encoding functions may be bypassed completely if desired. The controls and cir-

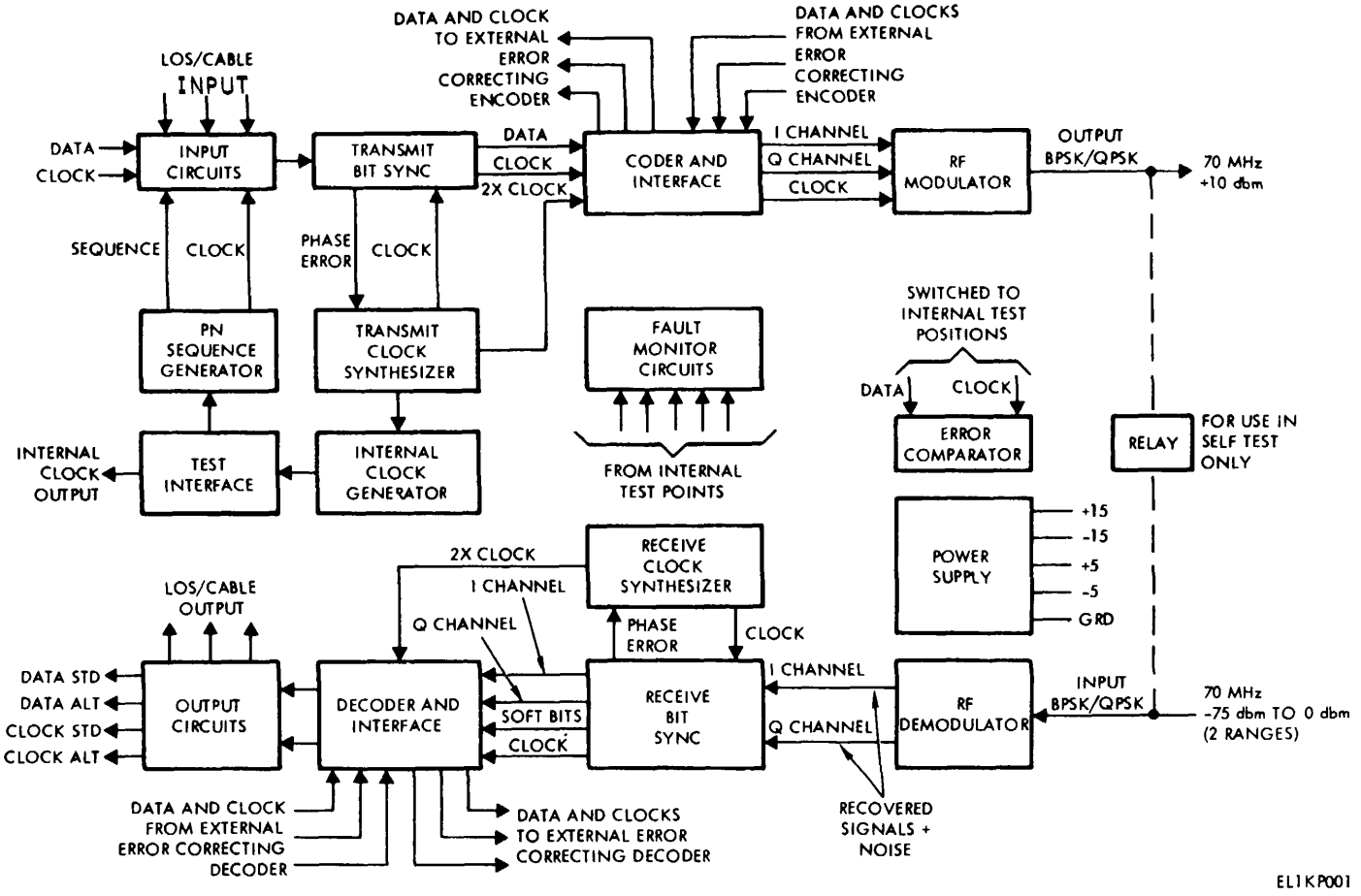


Figure 2-1. PSK/BPSK modem, functional block diagram.

cuit functions of the coder and interface are described in detail in paragraph 2-6.

(3) A data randomizer circuit is provided to enable the demodulator and receive bit synchronizer to operate properly when the data traffic has either very low transition densities or repetitive patterns. The randomizer converts the input data to a pattern that has near random properties. The randomizer function is used only in the QPSK mode, since the demodulator and receive bit synchronizer are less sensitive to repetitive data patterns in the BPSK mode. The randomizer is switch enabled, so that data can be either routed through or diverted around the randomizer logic.

e. RF Modulator. The transmit processing is completed in the RF modulator. This section uses the outputs of the coder and interface to biphase or quadraphase modulate an internally generated 70MHz carrier. Spectrum shaping filters and output amplifiers interface the modulated 70-MHz signal to the rear panel connector. The detailed circuit functions are discussed in paragraph 2-7.

f. RF Demodulator. In the receiving section, the 70-MHz biphase-modulated or quadraphase modulated QPSK/BPSK signal from the earth terminal downconverter is accepted by the RF demodulator The primary function of the RF demodulator is to acquire phase lock to the received 70-MHz signal, derive a coherent reference, and use this reference to demodulate the received data. This process results in output baseband signals which are corrupted by the noise inherent in the satellite communications link. The demodulator provides the capability of operation at any data rate from 16 kb/s to 20 MB/s by selecting the appropriate internal filters based upon the receive SYMBOL RATE switch settings. Detailed functional and circuit descriptions are provided in paragraph 2-8.

g. Receive Bit Synchronizer/Receive Clock Synthesizer.

(1) The data bit decision and clock recovery functions are accomplished by the receive bit synchronizer and the receive clock synthesizer. The combination of these functional blocks forms a phase locked loop which regenerates the clock signals required for the signal processing circuits. The function of this phase locked loop is essentially the same as the transmit bit synchronizer/synthesizer described in *c* above.

(2) The receive bit synchronizer must also provide digital output data based on a noisy baseband input. To do this, a matched filter which uses an integrate and dump technique is employed. The noisy baseband signal input is integrated over a full bit period, the integrator output is quantized at the end of the bit period, and the integrator is then dumped so that every integration process is started from the same reference level The output of the receive bit synchronizer is the result of the quantization, which provides an eight-level, three-bit code for each input bit. The three-bit code consists of a sign bit, which represents the actual ONE/ZERO bit decision, and two soft bits which represent the quality of the bit decision. The soft bits are required for operation with an external error correcting decoder such as the maximum likelihood or Viterbi equipments. Detailed functional and circuit descriptions are provided in paragraphs 2-9 and 2-10.

h. Decoder and Interface. The decoder and interface circuits reconstruct the original communications link input data When error correction encoding has been performed at the transmit end of the link, an external decoder may be selected as required for processing the received signal. The built-in differential decoder is independently selectable. For uncoded inputs, all decoding functions may be by-passed completely. A data derandomizer circuit is provided to convert the received data to its original pattern. The derandomizer is manually selectable, so that received data can be routed through or be allowed to bypass the derandomizer logic. The details of the circuit functions and selection are provided in paragraph 2-11.

i. Output Circuits. The output circuits provide standard data and clock signals from the decoder and interface output to a local digital user An identical alternate data and clock output is also furnished. The LOS/cable outputs permit interfacing the QPSK/BPSK modem with a remotely located user by means of an ICF modem. Either an LOS microwave link or shielded cables are used to perform the remote interface function. Detailed circuit functions are discussed in paragraph 2-12.

j. Internal Clock Generator The transmit clock synthesizer provides signals which are used by the internal clock generator to provide a stable output clock to the digital user at the selected input data rate. These circuits are discussed in detail in paragraph 2-13.

k. Test and Monitor Circuits. Test and monitor circuits within the QPSK/BPSK modem allow monitoring of the operation of the link and provide a means of rapidly localizing malfunctions Primary signals within the modem are monitored and their status is displayed on front panel lamps or the front panel meter. A pseudo-random sequence generator provides a known modulated signal at the output for link testing transmission. An error comparator in the receiver section detects and initiates a display of errors occurring in this pattern as received from the communications link. For self-testing, the transmitter output is relay-coupled into the receiver, and the error comparator evaluates the pattern at various functional block outputs These functions are discussed in paragraph 2-14.

2-3. Input Circuits

a. General. The input circuits (fig. 2-2) accept LOS or cable inputs to the LOS/cable receiver and decoder, or standard data and clock to the input interface The LOS/cable receiver and decoder provides cable equalization and also converts the bipolar NRZ format to logic level NRZ-L outputs (fig. 2-3). The bipolar NRZ format represents ONE bits by alternating positive and negative voltages. Positive and negative comparators in the LOS/cable receiver and decoder detect the voltage excursions and develop ICF 1 and ICF 2 signals which are OR'ed by the input interface card to develop logic level ONE bits. The bipolar NRZ-ZERO bits are represented by ground levels. In this case, the outputs of both comparators are high with a resultant logic level ZERO from the OR gate (ICF data). In the test mode, a similar bipolar NRZ link test signal from the LOS/cable driver is relay switched (by K1) to the comparators and is inserted in place of the ICF signals. The input interface logic receives standard input clock and data, ICF data, and a test sequence from the PN sequence generator.

(1) With the STD/CLK/ICF switch set to STD, the standard input data is routed through the input line receivers, gated through the data select gates, and applied through the output OR gate to the transmit bit synchronizer.

(2) With the STD/CLK/ICF switch set to CLK, the input standard data is gated through the data select gates to the data register and is loaded into the register by input standard clock. Standard data is then transferred from the data register directly to the encoder and interface, bypassing the transmit bit synchronizer. To maintain synchronization, the accompanying standard clock is divided by two to provide a signal with one transition during each bit period, and routed to the data input of the transmit bit synchronizer

(3) When the STD/CLK/ICF switch is in the ICF position, the OR'ed ICF data is gated through the data select gates and, via the output OR gate, to the bit synchronizer.

(4) When the MODE switch is set to the OPERATE position, the input data selection is controlled by the STD/CLK/ICF switch as indicated above. If the MODE switch is set to either the LINK or TEST position, the STD/CLK/ICF switch is disabled, and the test sequence from the PN sequence generator is routed to the transmit bit synchronizer input. If the MODE switch is set to the TEST position, the test sequence is also gated to a level converter which provides a bipolar +1 volt test output.

b. LOS/Cable Receiver and Decoder (fig. FO-2) The LOS/cable receiver and decoder (A3A2) receives inputs from an interconnect facility cable or LOS microwave link, and provides selection, filtering, equalization, amplification, and decoding of the received signal.

(1) The input selection, filtering, and equalization functions of the circuits are controlled by four card mounted switches, S1 through S4. The functions of these switches are given in table 2-1.

(2) If an LOS input (P1-2) is used, AR1 provides a stage of preamplifcation, with a gain of 25 dB. The output of AR1 is applied through one of the switchable lowpass filters to S2. The low pass filters consist of resistor R5 and the capacitor combinations shown below:

S1 position	*3dB bandwidth*	*Capacitors*	*Capacitance*
1	5t0 kHz	C9 + C2	509 pf
2	3.6 MHz	C9 + Ct	95 pf
3	10 MHz	C9	39 pf

(3) If one of the cable inputs is used, S4 is used for input selection The selected input is routed through S1, which provides the capability of switching into the circuit a stage of cable equalization (L2, LA, R10, R12), and then to S2 which selects either the LOS or the cable input for further processing.

(4) The input selected by S2 is amplified by AR2. Resistor R2 permits adjustment of the gain of AR2 to obtain the proper output level (2.4V p-p at TP1) regardless of the input signal level. Switch S3 permits the selection of a second stage of cable equalization (L3, R14), a lowpass filter (C12) which eliminates system noise above 15-MHz, or a straight through path to the next stage.

(5) Data from AR2 is applied through normally open contacts of relay [(1 to differential comparators } U1 and U2. The threshold of comparator U1 is set to +0.3 volt and the threshold of comparator U2 is set to -0.3 volt. When a ONE bit is received, the threshold level of one of the comparators is exceeded, with a resultant ground level output from that comparator. When a ZERO bit is received, both comparators produce positive outputs (These signals are OR'ed in the input interface card to produce NRZ coded data.)

(6) When the SOURCE switch is set to the TEST position, relay K1 is deenergized and the link test data from the LOS/cable driver is routed to the comparators.

c. Input Interface (fig. FO-3). The input interface (A3A5) receives standard input data and clock from the digital user, ICF 1 and ICF 2 data from the LOS/cable receiver and decoder, and test sequence data from the PN sequence generator. The data to be transmitted to the bit synchronizer is selected by inputs from the front panel STD/CLK/ICF switch and the transmit MODE switch.

(1) The standard input data, received via P1-30 and 28 is applied through one section of dual line receiver U3 to AND gate input U5-1 and to steer inputs 2 and 3 of flip-flop U1. If the STD/CLK/ICF

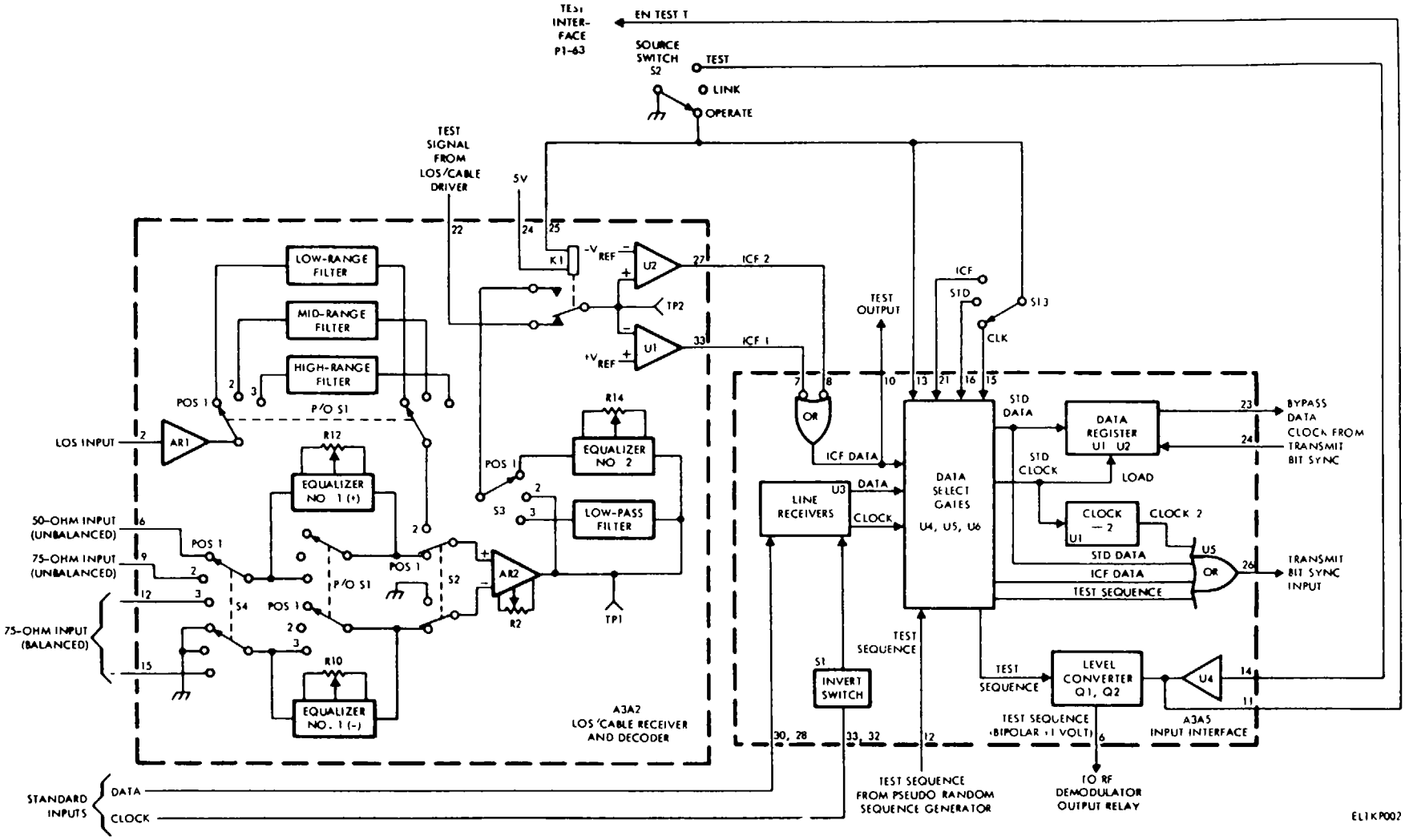


Figure 2-2. Input circuits, functional block diagram

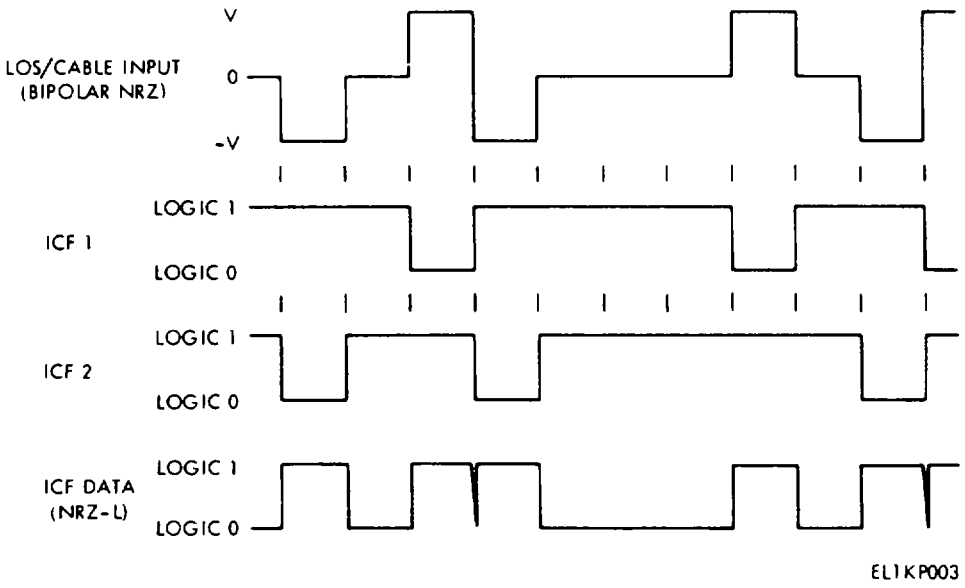


Figure 2-3. Bipolar NRZ to NRZ conversion

Table 2-1. Operation of LOS/Cable Receiver and Decoder Selection Switches.

Switch	Position	Function
A3A2S1	1	Selects input filter for use at input data rates from 16 kb/s to 225 00 kb/s if LOS microwave input is used, selects no first stage of equalization if any cable input is used
	2	Selects input filter for use at input data rates from 225 01 kb/s to 1 8000 Mb/s if LOS microwave input is used
	3	Selects input filter for use at input data rates from 1.8001 MB/s to 5.000 Mb/s if LOS microwave input is used, selects use of first stage of equalization if any cable input is used
A3A2S2	1	Selects operation with cable inputs.
	2	Selects operation with LOS microwave input
A3A2S3	1	Selects use of second stage of equalization at decoder input
	2	Selects use of no equalization or filtering at decoder input
	3	Selects use of lowpass filter at decoder input
A3A2S4	1	Selects 50-ohm unbalanced cable input.
	2	Selects 75-ohm unbalanced cable input
	3	Selects 75- ohm balanced cable input

switch is in the STD position and the MODE switch is in the OPERATE position, AND gate U5 pins 2, 4 and 5 are enabled by a ground input on P1-16 and standard data is gated through OR gate U5 (output pin 8) to provide the data input to the transmit bit synchronizer.

(2) Standard input clock is received through switch S1 (which permits clock inversion) and applied through the second section of dual line receiver U3. If the STD/CLK/ICF switch is in the CLK position and the MODE switch is in the OPERATE position, the line receiver is enabled by a ground input on P1 15 to gate the clock to the trigger inputs of both flip-flops of U1. In this mode, standard data is loaded in flip-flop U1 (output pin 5) at the input clock rate and shifted to flip-flop U2 by the clock input from the frequency synthesizer The output of U2 is then routed directly to the encoder and interface circuits. The clock divided by two output of U1-9 is OR'ed by U5 and used as the data input to the bit synchronizer.

(3) The ICF 1 and ICF 2 data from the LOS/cable receiver and decoder are applied to pins 1 and 2 of OR gate U6. The OR'ed output (U6-3) is applied to pin 4 of AND gate U6 and to the test circuitry via P1-10. If the STD/CLK/ICF switch is in the ICF position and the transmit MODE switch is in the OPERATE position, gate U6 is enabled by a ground input on P1-21 and ICF data, externally jumpered from P1-9 to P1-27, is applied through OR gate U5 to provide the data input to the bit synchronizer.

(4) The test sequence input (P1-12) from the PN sequence generator is applied to pins 9 and 12 of AND gates of U6 When the MODE switch is in the OPERATE position, U6-8 is disabled by a ground input at P1-13 The test sequence is gated via OR gate U5 to the bit synchronizer when the transmit MODE

switch is in the LINK or TEST positions. The STD/CLK/ICF switch is also disabled when MODE switch is in the LINK or TEST position, which disables the standard data, standard clock, and ICF inputs Refer to figure 2-2 for the switch connections. When the MODE switch is in the TEST position, U6-11 is also enabled by a ground input at P1-14 and its output is inverted by U4. Transistors Q1 and Q2 and diode bridge CR1 through CR4 develop a bipolar 1: volt test sequence to the receive bit synchronizer when U6-11 is enabled.

2-4. Transmit Bit Synchronizer

a. General. The bit synchronizer (fig. 2-4) provides a phase lock loop to maintain synchronization of transmitted bit rate and data. The input NRZ-L data is clocked into the bit detector phase flip-flop at beginning of bit period and into the data flip-flop at mid-bit period. Also at mid-bit period, the contents of the two flip-flops are transferred to the storage register. The transition detector compares the data from the storage register (preceding data bit) with the content of the data flip-flop (present data bit) to determine whether a transition has occurred. An adder compares the stored phase bit with the present data bit. These bits are the same if bit rate is in sync or slightly behind data and the adder output is a ONE. If bit rate is ahead of data, the phase flip-flop loads the preceding bit and the adder output is a ZERO. Thus, the transmit bit detector acts as an early/late transition detector. If a transition has occurred, the adder output is gated to the loop filter.

The $\overline{\text{DATA}}$ output of the data flip-flop is applied to a retriggerable one-shot circuit The circuit has a relatively long output pulse and is retriggered by normal data transitions so frequently that its output is not allowed to expire. However, when data input ceases, the pulse expires and a loss of lock signal is routed via an OR gate to the alarm card. A second one-shot receives outputs from the loop filter up/down counter overflow circuits Whenever the counter capacity is exceeded, the one-shot is triggered to develop a negative output to indicate loss of lock.

The loop filter arithmetic circuits receive the phase MSB and transition bit (the MSB is jumpered to three loop filter inputs). These bits are added to bits previously received to develop an up or down count to the accumulator. The accumulator is equipped with overflow detection circuits that provide an input to the loss of lock circuits on the transmit bit detector.

The accumulator output is added to the contents of the input register to develop an 8-bit digital control word representing phase error The adder output is then loaded into a storage register on the D/A converter card The output of the D/A input register is converted to an analog current by the D/A converter The analog current is used as a phase correction signal to the transmit frequency synthesizer.

b. Transmit Bit Detector (fig FO-4). The transmit bit detector (A3A35) receives data and bit rate inputs and provides outputs to the loop filter indicating whether bit rate leads or lags the data. The transmit bit detector also provides a loss of lock indication when data stops or when the loop filter up/down counter overflows (in either direction).

(1) The transmit data input (P1-12) is applied to pin 2 of data flip-flop U3 and pin 2 of phase flip-flop U4 (the other flip-flops of U3 and U4 are not used). The bit rate complement (P1 15) is delayed by double inversion through circuits of U2 and loads data into phase flip-flop U4. If clock and data are exactly in sync or if clock lags data, phase flip-flop U4 is loaded near the leading edge of data. If clock leads data, the flip-flop is loaded near the trailing edge of data. The Q output of U4 is applied to the C input of storage register U6.

(2) Bit rate true (P1-34) is received through circuits of U1 and, at mid-bit period, clocks storage register U6 to load the contents of phase flip-flop U4 into the C stage and to load the previous data bit from data flip-flop U3 into the A stage. Bit rate true also loads the new data bit into data flip-flop U3. Refer to figure 2-5 for bit detector timing.

(3) Exclusive OR U10 compares the new data bit from the Q output of U3 with the previous data bit from the QA output of storage register U6 to determine whether a data transition has occurred. The data transition signal enables gate U8 and is routed to the loop filter via P1-24.

(4) The MSB input to the loop filter is formed by adder U7 This circuit sums the output of data flip-flop U3 and the output from QC of storage register U6 (with a constant ONE carry input). Since the data flip-flop and storage register are clocked simultaneously, the adder inputs will be the same if the phase flip-flop loaded the current data bit (clock in sync with the data or clock lagging data). With both inputs the same, the adder output is a ONE Assuming a data transition and clock leading data, the phase flip-flop would load the previous data bit, the adder inputs would differ, and the adder output is a ZERO. The adder output is AND'ed with the transition bit and the resultant output MSB (U8-12) is routed to the loop filter via P1-23.

(5) Circuit U5 is a retriggerable one-shot with an output pulse period exceeding six seconds The one shot is triggered each time a data ZERO is loaded into flip-flop U3, thus maintaining a high to pin 3 of U8 If data ceases, the one-shot output expires and a loss of lock indication (logic ZERO) is developed by gate U8 at P1-17.

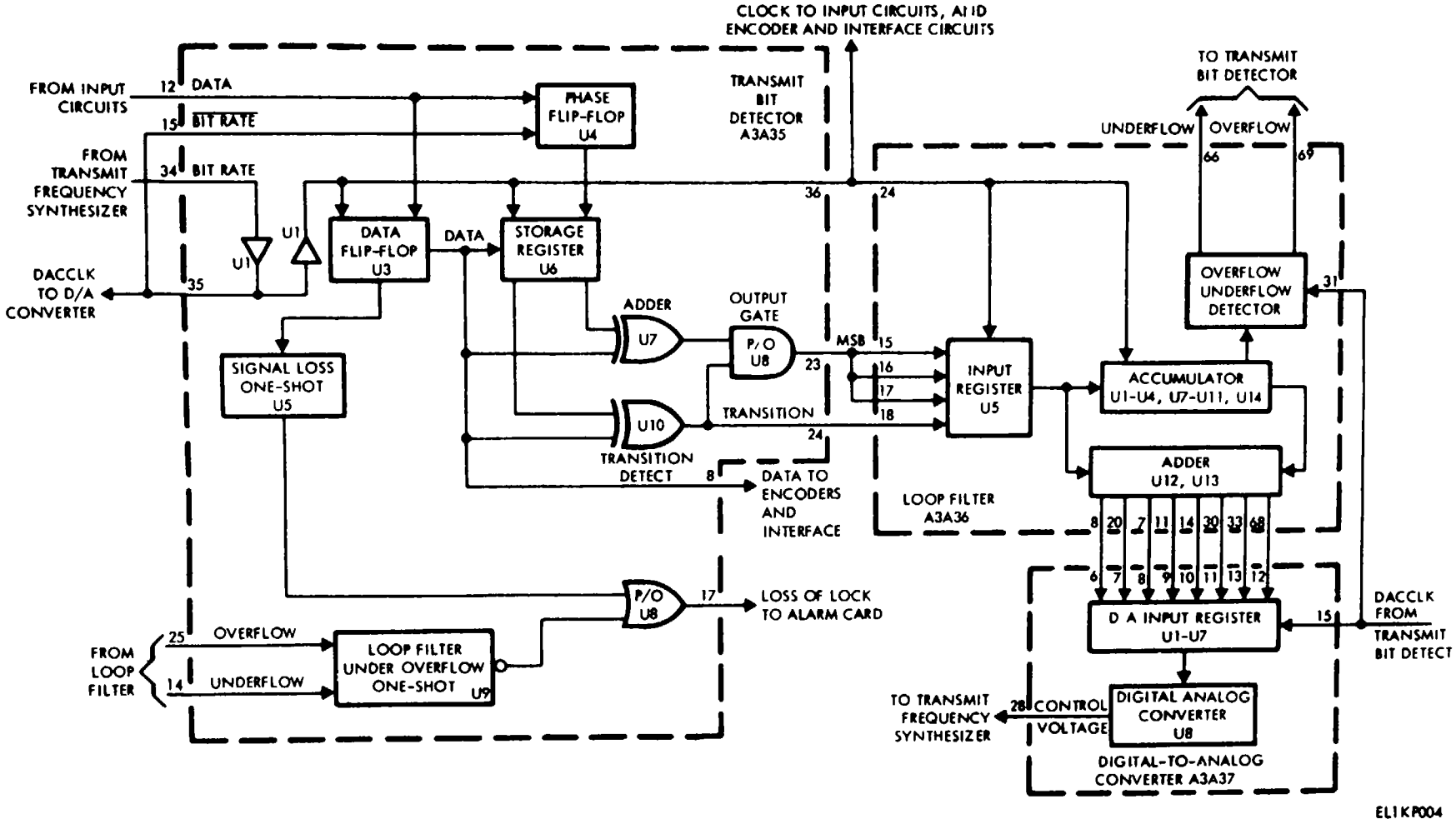


Figure 2-4. Transmit bit synchronizer, functional block diagram

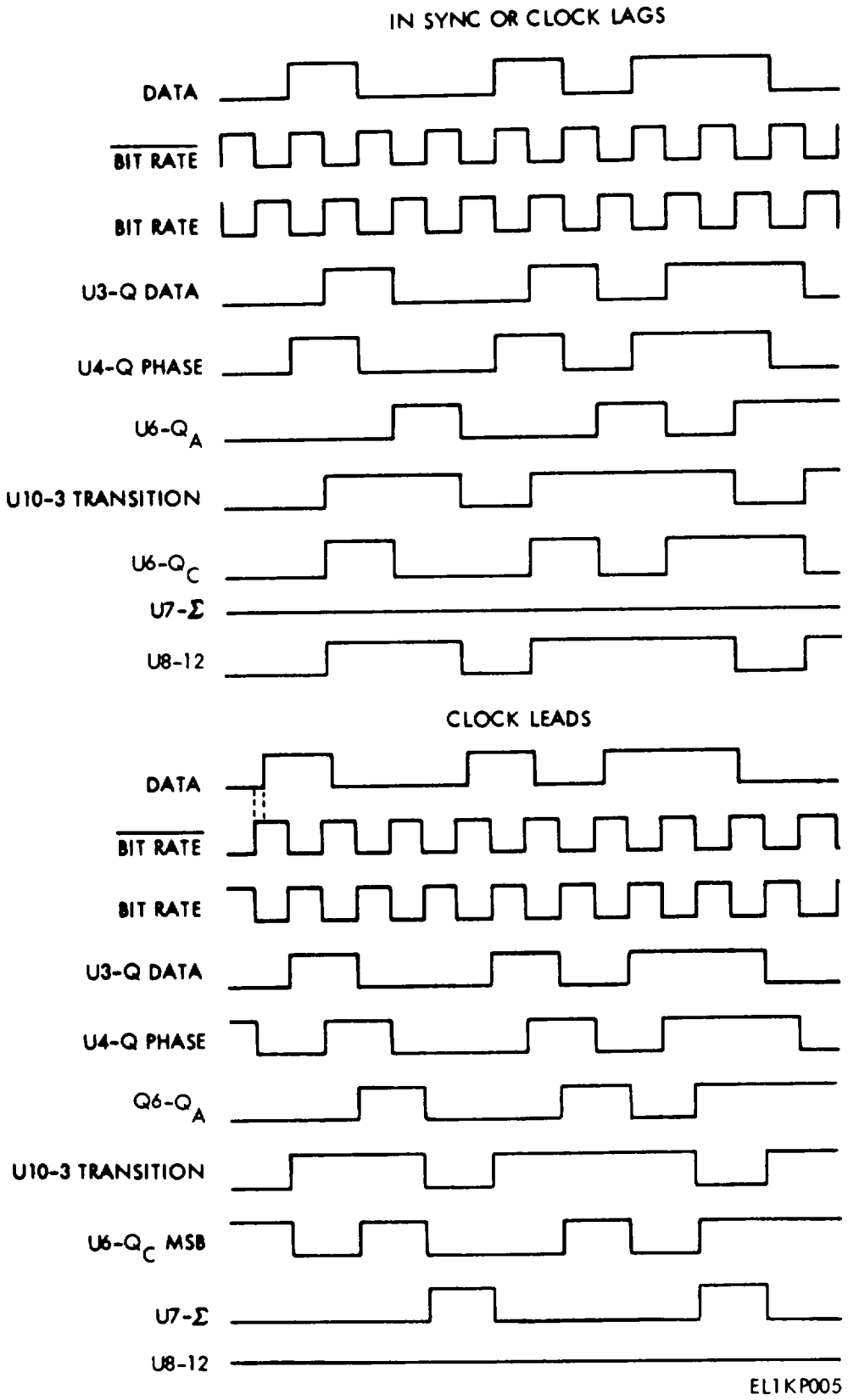


Figure 2-5. Transmit bit detector, timing diagram.

(6) Loss of lock is also developed when the loop filter up/down counter overflows. Either an under or an over count signal from the loop filter triggers one shot U9. The negation output of the one-shot, via U8, then provides a loss of lock signal to the alarm card.

(7) The bit detector also provides true and complement clock and data outputs. Bit rate complement from U1-6 is routed to the loop filter and the D/A converter. Bit rate true from U1-8 is routed to the loop filter, the input circuits, and the randomizer/derandomizer in the encoder and interface circuits. Data true from U3-5 is routed to the randomizer/derandomizer in the encoder and interface circuits.

c. Loop Filter (fig FO-5). The loop filter (A3A36 receives four input bits developed from the phase error decision and the transition signal, and bit rate timing inputs The circuit provides the digital equivalent of a lead integrate analog filter and its output is an eight bit word to the D/A converter.

(1) Figure 2-6 illustrates the loop filter function. The four bit word representing the phase error input is loaded into an input register. An arithmetic unit accumulates the successive phase words by adding each phase X ord input to the number stored in the arithmetic unit. An 8-stage up/down counter increases the accumulator capacity. The counter is incremented up or down each time the capacity of the arithmetic unit is exceeded. The final output to the D/A converter is developed by adding the input word to the accumulator output. The output, therefore, is a function of two factors; the phase word in the input register, and the cumulative result of previous phase words.

(2) The phase word, which is developed from the phase error decision and the transition signal, is load

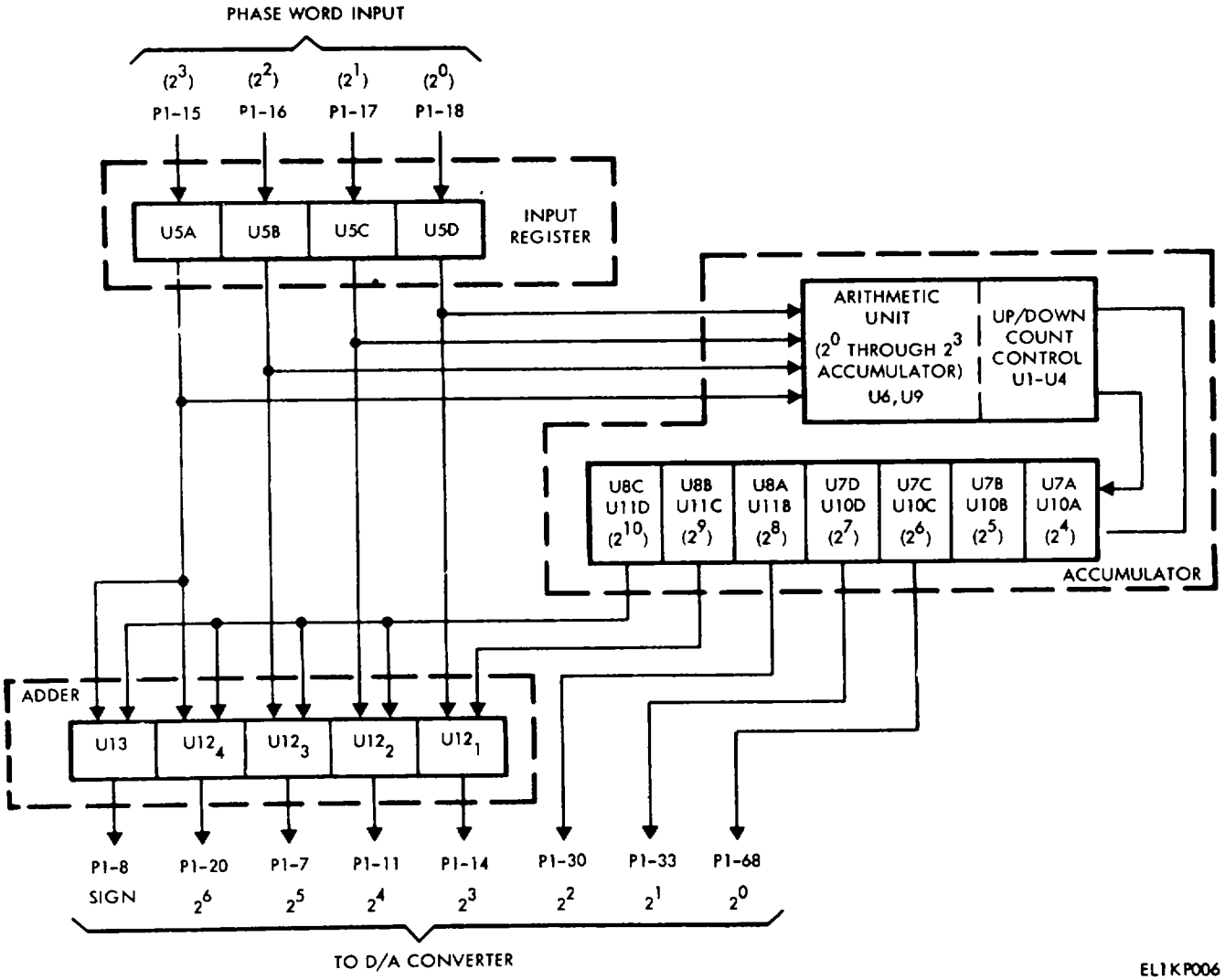


Figure 2-6. Lop filter, functional block diagram.

ed into the input register by bit rate clock applied to P1-24. The format of the phase word is defined in table 2-2. When no transition has occurred, the phase word input is all ZERO's. When a transition occurs, the phase word represents a weight and magnitude associated with the detected phase error. In the transmit bit synchronizer, P1-15, P1-16, and P1-17 are connected together in the card file; thus the input phase word associated with each transition is either a +1 or -1 depending on the early/late gate operation of the transmit bit detector.

Table 2-2. Phase Word Format

Phase error input	P1-15 (2^3)	P 16 (2^2)	P1-17 (2^1)	P1-18 (2^0)
+7	0	1	1	1
+5	0	1	0	1
+3	0	0	1	1
+1	0	0	0	1
0	0	0	0	0
-1	1	1	1	1
-3	1	1	0	1
-5	1	0	1	1
-7	1	0	0	1

(3) Adder circuit U6 adds each new phase word with the sum of the previous associated words circulated through register U9. As an example of adder operation, assume U9 contains a binary 9 (1001) and a phase word representing +3 (0011) is present in the input register. The result at the sum output of U6 is a binary 12 (1100), which is entered into U9 at the end of the clock period. The next phase word will be entered into the input register U5 and simultaneously added to the contents of U9 during the next clock period. Assuming this next phase word is a -5, the result at the sum output of U6 will then be:

$$\begin{array}{r} 1100. \\ +1011. \\ \hline (1)0111. \end{array}$$

where the parenthetical 1 represents a carry output. The 4-bit sum output of U6 is a binary 7, which is 5 less than the previous number. In the case where the input phase word represents no transition (0000), the sum output of U6 is identical to the contents of U9, and the output of U9 does not change.

(4) Up/down count control to the balance of the accumulator circuitry is controlled by U1-U4. As shown in table 2-2, the LSB (P1-18) of the phase word input is a transition/no transition indicator and the MSB (P1-15) is a sign indicator. When a positive phase word is present in input register U5 (QA low and QD high), the up count control is generated if a carry output from U6 is present. U6-14 high will result in a low at U2-6, and an up count control pulse will be developed at U4-11 after U3-6 goes high on the next clock pulse. When a negative phase word is present in input register U5 (QA and QD high), the down count control is developed at U4-8 if no carry output is developed by U6 (U6-14 low).

(5) Since the binary counter chain of U7 and U8 upcounts once each time an overflow from U6 occurs and downcounts each time an underflow occurs, each successive counter stage contains an increasingly significant bit in a binary number representing the phase word accumulation. The status of counters U7 and U8 are transferred into storage registers U10 and U11 at the end of each clock period.

(6) The outputs of the phase word accumulator beginning with the bit representing 26 are used to provide the less significant bits to the D/A converter. The two most significant bits of the phase accumulation are added to the input register state by adder U12 with the input but representing 20 weight being used to develop the 23 input to the D/A converter The magnitude of each D/A converter input word is therefore equivalent to:

(Input register state x 8) +
(Phase word accumulation ÷ 64)

The sign bit to the D/A converter is developed by adder U13

d. Digital-to-Analog Converter (fig. FO-6). The digital-to-analog (D/A) converter (A3A37) accepts the 8-bit output of the loop filter and develops an equivalent analog output to control the frequency of the frequency synthesizer. The 8-bit output of the loop filter is applied to steer inputs of flip-flops U1 through U4. These flip-flops are loaded at bit rate and their outputs drive the D/A converter The D/A output provides a current source (maximum ±2.5 milliamperes) to control the frequency of the synthesizer.

2-5. Frequency Synthesizer

a. General. The frequency synthesizer (fig. 2-7) functions as the voltage controlled oscillator (VCO) for the bit synchronizer. The effective VCO center frequency is selected by five front panel digit switches while tuning is accomplished by the control input from the bit synchronizer. The synthesizer operates over the center frequency range of 10 kHz to 9.9999 MHz, while the tuning range available to the bit synchronizer is a minimum of ±0.025 percent of the selected bit rate. The frequency synthesizer utilizes an indirect phase lock loop to develop a stable programmable reference frequency that is then mixed with the output of a VCO. The VCO is tuned by a control input from the bit synchronizer. The difference frequency output between the programmable reference and the VCO is down counted to produce the center frequency selected by front panel switches.

(1) The synthesizer reference frequencies are developed from a 15-MHz temperature compensated

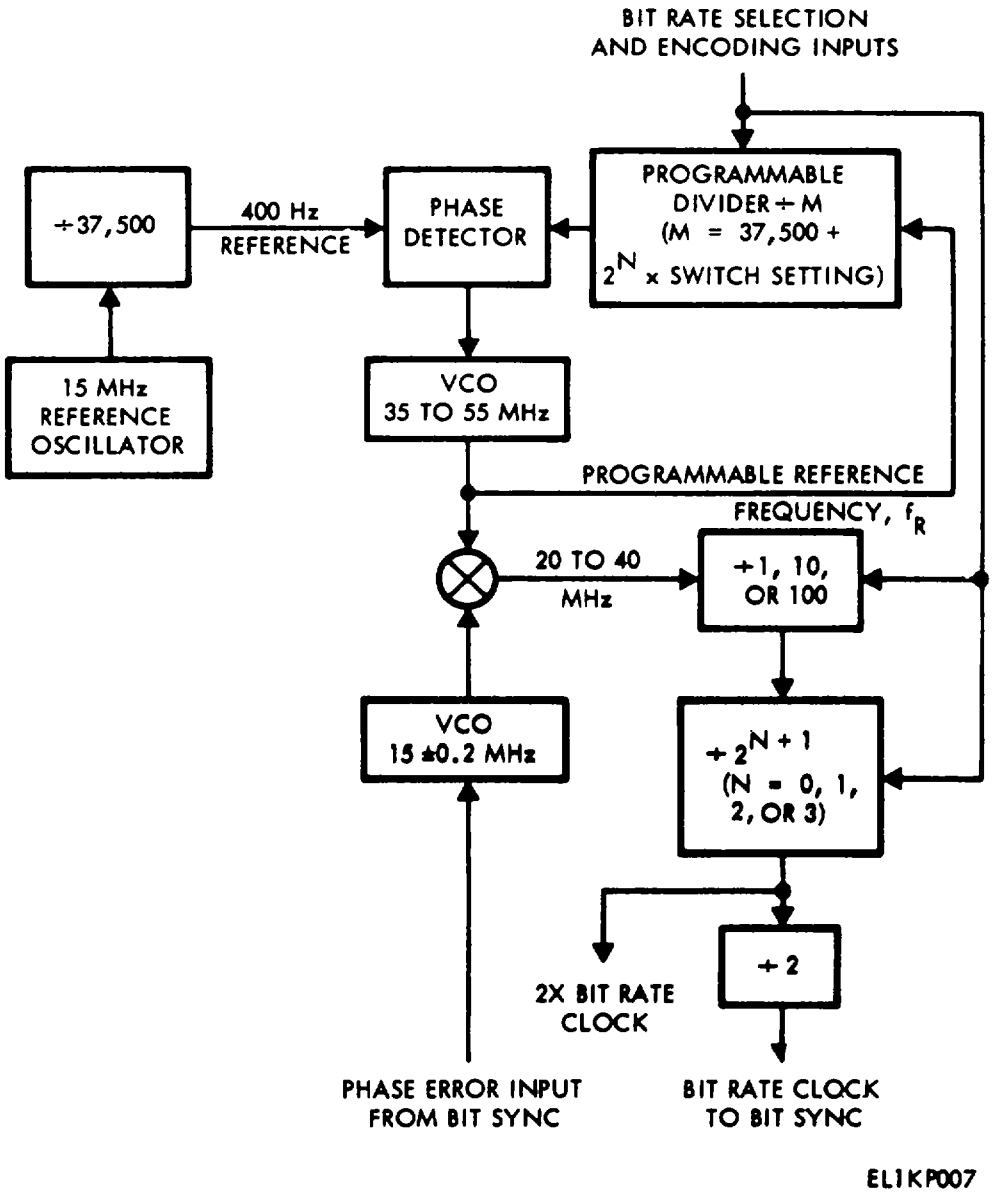


Figure 2-7. Frequency synthesizer, general block diagram

crystal oscillator (TCXO). The output of this oscillator is divided by 37,500 by the reference divider to develop a 400 Hz reference signal to the phase detector.

(2) The phase detector produces a voltage proportional to the phase difference between the 400 Hz reference signal and the programmable divider output signal. This voltage is then applied to the VCO to adjust the output frequency between 35 and 66 MHz. The VCO output frequency is applied back to the programmable divider input.

(3) The programmable divider divides the VCO output by a number, M, which varies between 87,500 and 137,499 depending on the encoded bit rate selection control inputs. Since the programmable divider output is applied back to the phase detector input, a feedback loop exists which adjusts the VCO to maintain a 400-Hz programmable divider output. Therefore, the VCO provides an internal programmable reference frequency, f_R, at a rate equal to 400 Hz x M, where M is the selected division ratio of the programmable divider.

(4) The final output frequency is derived by mixing the programmable reference frequency with the output of the 15-MHz VCO, which is controlled by the bit synchronizer. The resultant difference frequency is then divided by selectable decade and binary counters to produce a nominal output rate equal to selected data rate; however, the exact output rate is dependent on the 15-MHz VCO output.

(5) The output frequency is controlled by using the digital thumbwheel switch settings, a number, N, which is derived from the digital thumbwheel switch settings, and the decade switch setting to control the various internal frequency dividers. Operation over the full output frequency range is accomplished by operating in three decade ranges, as indicated on the thumbwheel decade selection switch, and by internally subdividing each decade range into four octave ranges. The octave range of operation defines the value of N as indicated in table 2-3.

Table 2-3. Synthesizer Range Selection

Range	Digital thumbwheel switch setting	N
A	10000 to 12499	3
B	12500 to 24999	2
C	25000 to 49999	1
D	50000 to 99999	0

(6) To illustrate the frequency synthesis process, assume a case in which an input data rate of 170.00 kb/s has been selected. It can be seen from table 2-3 that the digital thumbwheel switch settings will cause the synthesizer to operate in range B (N2). The programmable divider ratio, M, is given by the expression:.

$$M = 87{,}500 + (2^N \times \text{switch setting})$$

therefore:.

$$M = 37{,}500 + (4 \times 17{,}000)\ 105{,}500.$$

Since the internal phase locked loop forces the programmable reference frequency, f_R, to be equal to 400 x M, then:

$$f_R = 400 \times 105{,}500 = 42{,}200{,}000 \text{ Hz}$$

The center frequency input to the decade divider is obtained by subtracting 15-MHz from f_R, which yields a center frequency of 27,200,000 Hz. The divide by 10 function is selected in this case, and the decade counter produces an output of 2,720,000 Hz. Since N is 2, the $\div 2^{N+1}$ -counter output is 2,720,000 Hz÷8, or 340,000 Hz. This signal is available as the 2 x bit rate clock. The final ÷2 stage produces a bit rate clock at 170,000 Hz, which is equal to the INPUT DATA RATE switch setting of 170.000 kb/s.

(7) Internal operating rates and ratios for various INPUT DATA RATE switch settings between 1.0000 and 9.9999 Mb/s are given in table 2-4. For the switch settings shown, the decade divider is programmed to divided by 1. Operation in the lower decade ranges is identical except that the decade divider is programmed to divide by 10 or 100 as required.

b. Description.

(1) The output of the 15-MHz reference oscillator (fig. 2-8) is applied to a power divider, which provides an output to the internal clock generator and drives a level converter. The converted 15-MHz signal is applied to a fixed counter on the reference divider card. The counter divides by a ratio of 37,500 to produce a 400-Hz reference pulse to the phase detector.

(2) The phase detector used the 400 Hz reference signal to produce an internal voltage ramp each time a reference pulse is received. The output pulse from the programmable divider is then used to sample the ramp voltage. The resultant phase detector output is a voltage proportional to the phase difference between the reference pulse and the programmable divider output. When the loop is locked, this voltage is used to control the 45-MHz VCO via the loop filter. For acquisition, a frequency detector generates a voltage proportional to the difference between 400 Hz and the output rate of the programmable divider. This voltage is added to the loop filter input, and is also used as a test output.

(3) The 45 MHz VCO output is amplified and filtered on the 45.MHz amplifier card, and distributed to the internal clock generator, the mixer, and the programmable divider input via a power divider.

(4) The programmable divider counts down the VCO output to maintain operation of the phase lock loop at 400 Hz. This is accomplished by first dividing the VCO output by the constant 37,500 plus 1, 2, 4, or 8 times the bit rate switch setting, dependent upon the selected bit rate octave. The 400-Hz output pulse from the programmable divider closes the phase lock loop.

Table 2-4. Divider Ratio and VCO Outputs

Range	Switch setting		Multiplier		Constant		Divider ratio	VCO output (MHz)	VCO -15 MHz		2N+1	2R out (MHz)	R out (MHz)
D	99999	×	1	+	37500	=	137499	54.999600	39.999600	+	2	19.999800	9.999900
(N=0)	50000	×	1	+	37500	=	87500	35.000000	20.000000	+	2	10 000000	5.000000
C	49999	×	2	+	37500	=	137498	54.999200	39.999200	+	4	9.999800	4.999900
(N=1)	25000	×	2	+	37500	=	87500	35.000000	20.000000	+	4	5.000000	2.500000
B	24999	×	4	+	37500	=	137496	54.998400	39 998400	+	8	4.999800	2 499900
(N=2)	12500	×	4	+	37500	=	87500	35 000000	20.000000	+	8	2 500000	1.250000
A	12499	×	8	+	37500	=	137492	54 996800	39 996800	+	16	2 499800	1.249900
(N=3)	10000	×	8	+	36500	=	117500	47 000000	32 000000	+	16	2 000000	1 000000

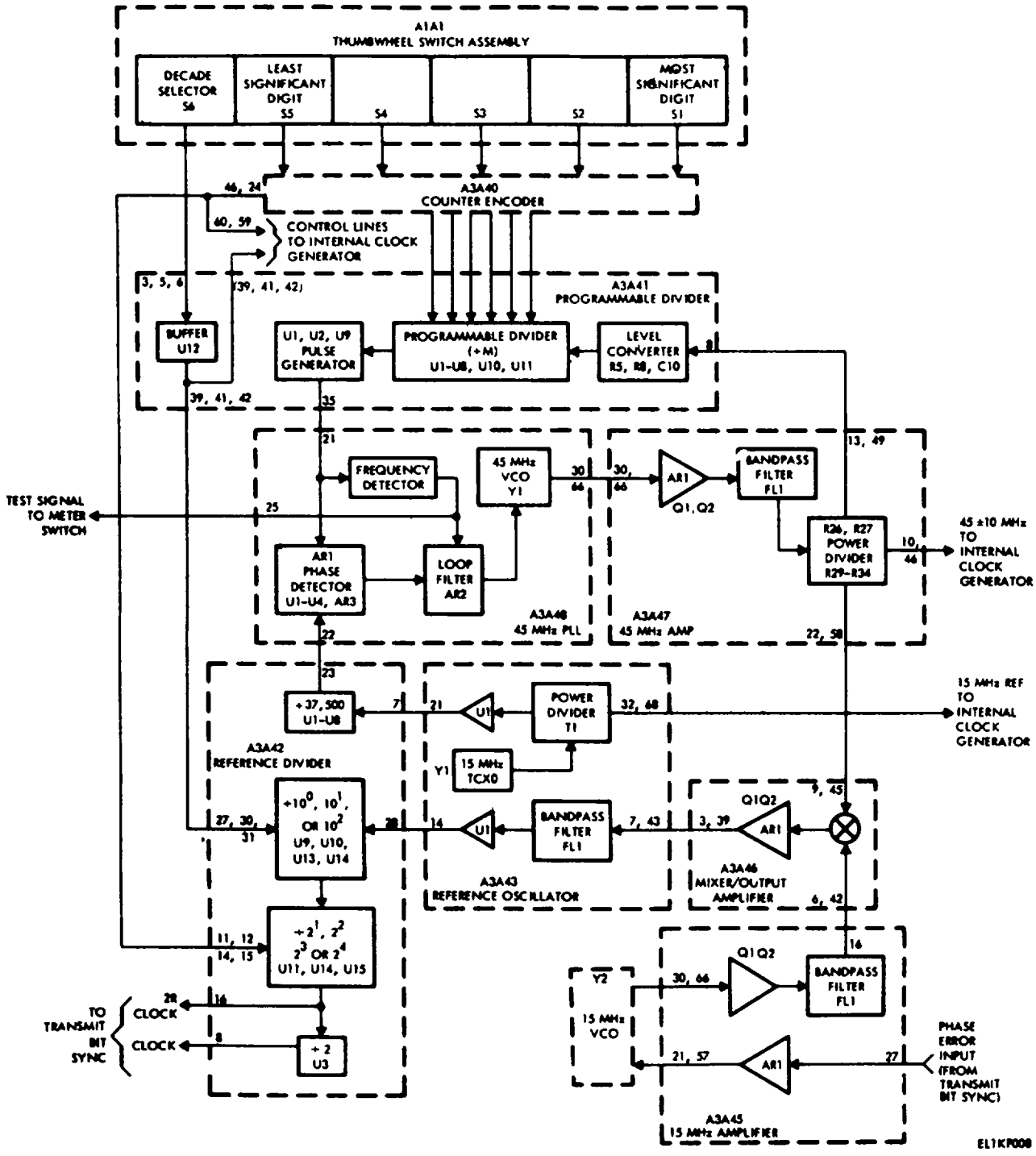


Figure 2-8. Frequency synthesizer, functional block diagram.

(5) The counter encoder decodes the digital thumbwheel switch settings to determine the octave range of operation and control the number of times the programmable divider divides by the thumbwheel switch setting. The decoder octave range output is also provided to the internal clock generator and the programmable binary counter. The counter encoder also provides the constant 37,500 input to the programmable divider.

(6) The control input from the bit synchronizer is applied through a current-to-voltage amplifier to the 15 ±0.2-MHz VCO The 15 ±0.2-MHz VCO output is amplified, filtered, and applied to the mixer/output amplifier. The difference frequency output from the mixer, ranging from 20 to 40 MHz, is routed through a low pass filter to a divider chain. A decade divider is included to provide ÷1, ÷10, and ÷100 functions. The ÷1 function is used for all bit rates over 1.0000 MHz. The ÷10 and ÷100 functions provide decade division for frequencies below 1.0000 MHz. Following the decade counter, a binary counter provides division ratios of 2, 4, 8, or 16, as selected by the counter encoder, to produce twice the desired bit rate. The output stage is a divide by two flip-flop which provides the bit rate output.

c. Reference Oscillator (fig FO-7). The reference oscillator card (A3A43) contains the 15-MHz temperature compensated crystal oscillator (TCXO) and a 30 MHz bandpass filter. Also included on this card is a power divider and level converters.

(1) The reference frequency for the synthesizer is developed by 15-MHz TCXO Y1. This oscillator is stable within ±2 ppm/3 months. The oscillator output is transformer-coupled to one half of dual high speed ECL to TTL level converter U1. The output of U1 is compatible with the divide by 37,500 circuit on the reference divider.

(2) Bandpass filter FL1 receives the 20-to40MHz output of the mixer/amplifier card through a 3 dB attenuator (R3, R5, and R6). The filter center frequency is at 30 MHz, the 1 dB bandwidth is 20-MHz, and the 15 dB bandwidth is 30 MHz The 30 dB bandwidth is 40 MHz The output of FL1 is applied through a resistive power divider to the other half of ECL to TTL level converter U1 The level converter output then drives the selectable decade and binary dividers on the reference divider card and the other power divider output (P1-32, 68) is available to the internal clock generator circuit.

d. Reference Divider (fig. FO-8). The reference divider (A3A42) provides a divide by 37,500 countdown of the output of the 15-MHz TCXO to produce 400-Hz reference pulses to the phase lock loop The reference divider card also contains a decade counter to divide to 20-40-MHz output of the mixer/amplifier by 1, 10, or 100 dependent upon the front panel decade rate range selected. The decade counter output is then applied to a straight binary counter that further divides the clock signal by 2, 4, 8, or 16(2 N+1) depending on outputs from the counter encoder. The output of the binary counter is 2 times bit rate which is further divided by two to produce bit rate.

(1) The level converted 15-MHz output of the temperature compensated crystal oscillator (TCXO) is divided by a J-K flip-flop of U3 (P1-7) to develop 7.5 MHz into binary counters U4 and U5. Counters U4 and U5 are short-counted to divided by 75 (rather than 256) by utilizing the load inputs to preset a count of 181 each time a carry output from U5 occurs. The 100-kHz is used to clock the divide by five counter U6, divide by 50 counters U7 and U8, and output flip-flop U12.

(2) The divide by five counter, U6, is preset to count six and the output count 10 is detected by U2 to again preset the counter and to enable divide by 50 counters U7 and U8. These counters are shortcounted by presetting to count 206 using the carry output of U8 and the decoded count 10 output of U6 vis U2-3, U1-10, and U2 -11. The 400-Hz carry output of U8 steers flip-flop U12 high and then low at a 400-Hz rate to produce a 400-Hz, 50-microsecond positive pulse from the flip-flop (P1-23).

(3) Control for decade counters U9 and U10 is developed from the bit rate select range switch via inverters in the programmable divider. When no decimal division is required, U13-12 is enabled by the ÷1 control signal (high on P1-31) and clock is routed directly through U13 and U14 to binary counter U11. The ÷10 control signal (high on P1-30) enables U13-9 to select the QD output of U9 to the binary counter, and the ÷100 control signal (high on P1 -27) enables U13-2 to select the QD output of U10 to the binary counter.

(4) The counter encoder provides a four bit word to enable one of the U15 AND gates depending on the digital thumbwheel switch settings These gates receive the ÷2, ÷4, ÷8, and ÷16 outputs of binary counter U11 and gate the selected output which is equal to selected rate times two. Bit rate times two (U14-6) is divided by a flip-flop of U3 to develop the bit rate output.

e. 45-MHz Phase Lock Loop (fig. FO-9). The 45 MHz phase lock loop card (A3A48) contains a phase detector, a loop filter, a 35-55 MHz VCO, and a frequency discriminator. The synthesizer phase locked loop is closed through the programmable divider card, where the VCO output is counted down to 400 Hz.

(1) The phase detector section of the phase lock loop is formed by analog switch U1, amplifier AR1, and analog gate U4 This section uses the hold-sample-hold technique to develop the phase error voltage AR1 and C1 form an inverting integrator circuit The maximum negative output voltage is deter-

mined by VR1 and CR1, which acts as a clamp at -6.2 volts. The integrator receives input currents from one of two sources: a positive input current from the +15 volt supply via R2 and gate U1, or a negative input current from the -15-volt supply via R1 and gate U1. At the beginning of the reference period, the positive reference pulse applied to P1-22 closes three parallel connected gate sections of U1l and allows current to flow through R2 to the integrator. At this time the remaining gate section of U1 is also closed (fig. 2-9), but the current through R2 is much greater than the current through R1, therefore, the integrator output goes negative until the -6.2 volt clamp voltage is reached. The three parallel-connected gate sections of U1 are opened at the end of the reference pulse and the integrator voltage begins a positive ramp due to the input current from R1. The output pulse from the programmable divider is applied to P1-21. When this negative-going pulse arrives, the output of U2-2 opens the U1 gate section connected to R1. The integrator receives no input current, and the integrator output voltage remains constant while the programmable divider output pulse is present. Since this pulse is also applied to P1 -23, an internal analog gate in U4 is simultaneously closed. This allows the integrator output voltage to be transferred to C5, which acts as a storage element. The voltage on C5 is buffered internally by U4 and the buffered voltage appears on U4-11. At the end of the output pulse from the programmable divider, U1-3 is closed, the internal gate in U4 is opened, and the integrator output ramp continues until the next reference pulse arrives. If the loop is operating in sync with the reference pulse and the required VCO output frequency is 45MHz, the hold signal would occur at mid-bit period as the integrator output is crossing through the zero volt level. A positive or negative output of U4 provides speed up or slow down control to the 45 $\pm$10 MHz VCO via the loop filter, AR2.

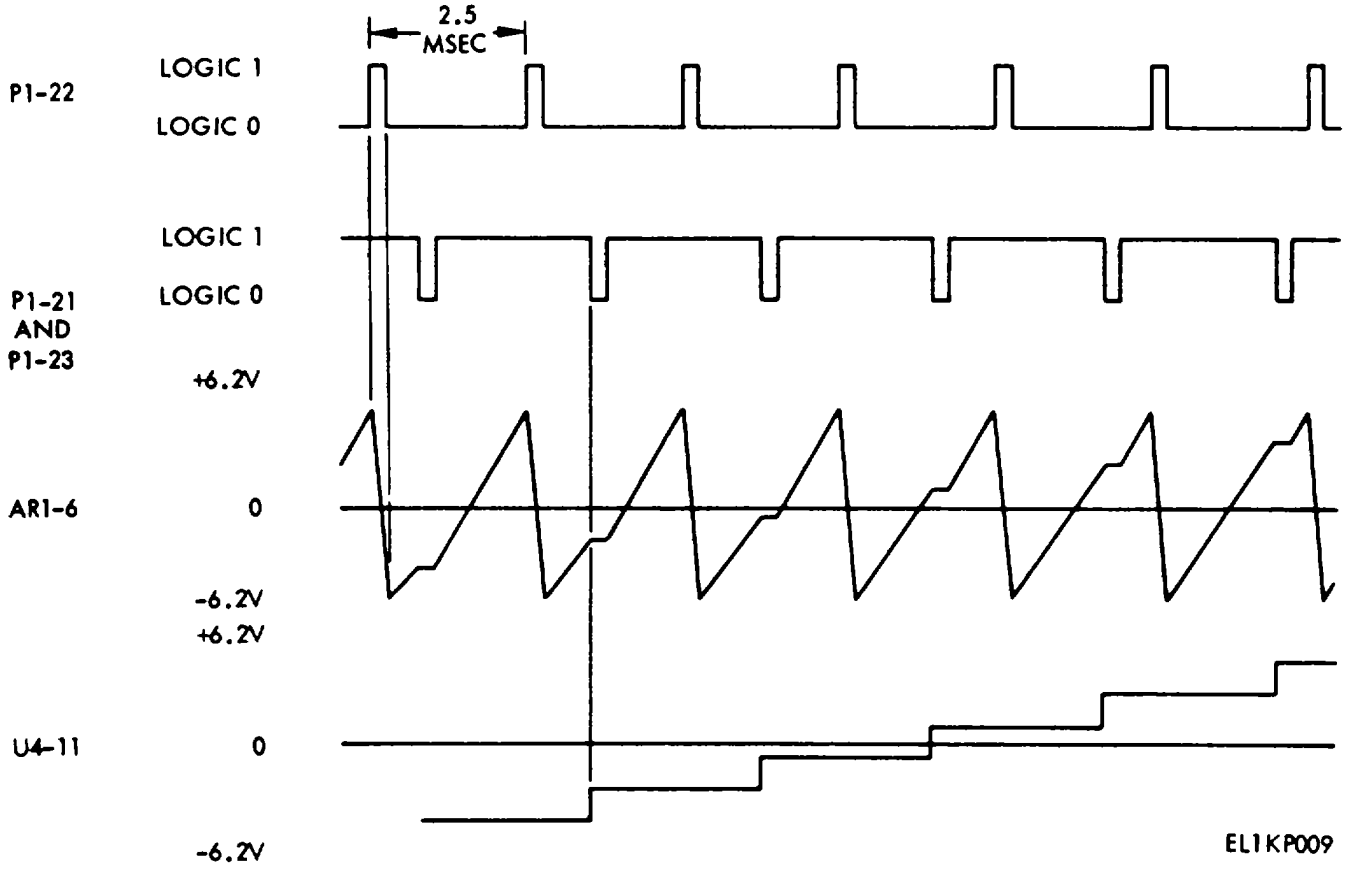


Figure 2-9. Synthesizer phase detector, timing diagram.

(2) Amplifier AR2 and associated components form the loop filter at the input to the 45 ±10 MHz oscillator. The amplifier has a dc gain of approximately 80. A positive 10-volt output of the amplifier will drive oscillator Y1 to operate at 35 MHz, while a negative 10-volt output causes the oscillator to operate at 55 MHz.

(3) The frequency discriminator is formed by one-shot U3 and operational amplifier AR3. The one shot circuit is triggered by the trailing edge of each sample pulse and develops an output that is adjusted to one-half reference bit period in duration (1.25 milliseconds). When the phase lock loop is operating at 400 Hz, the average output of amplifier AR3 to the loop filter, which represents the sum of the currents through R20 and R15, is zero. When the loop is off frequency, (not phase locked) the output of AR3 to the loop filter provides an error voltage via the loop filter AR2 to correct the oscillator output. Resistors R18 and R21 condition the AR3 output to be compatible with the front panel meter.

f. 45-MHz Amplifier (fig. FO-10). The 45-MHz amplifier (A3A47) consists of three amplifier stages followed by a low pass filter. The amplifier input from the 45 ±10 MHz VCO is amplified, filtered, and routed to the programmable divider, the mixer/output amplifier, and the internal clock generator. The 35 to 55 MHz output of the phase lock loop card, which is received at approximately -8 dBm, is further attenuated by 20 dB across resistors R5 through R7 and applied to the RF amplifier stages. The RF amplifier stages are formed by operational amplifier AR1 and transistors Q1 and Q2. The amplifier has an overall gain of approximately 40 to 45 dB as controlled by variable resistor R24. The amplifier bandwidth is 70 MHz. Each stage of the amplifier is transformer coupled to the next, and the output of transformer T2 is applied to 56 MHz low pass filter FL1. Filter FL1 suppresses harmonics of the signal and provides an output that is attenuated, split, and routed to the mixer/output amplifier and the programmable divider.

g. Programmable Divider (fig. FO-11). The programmable divider (A3A41) functions within the phase lock loop to count down the 35to 55MHz output of the 45 ±10-MHz VCO to provide 400-Hz sample pulses to the sample and hold circuits. This is accomplished by first dividing the VCO output frequency by a 37,500 constant, then further dividing by the digital INPUT DATA RATE switch setting multiplied by 1, 2, 4, or 8. The divider ratio is thus 37,500 + (2^N x switch setting) as illustrated in figure 2-10.

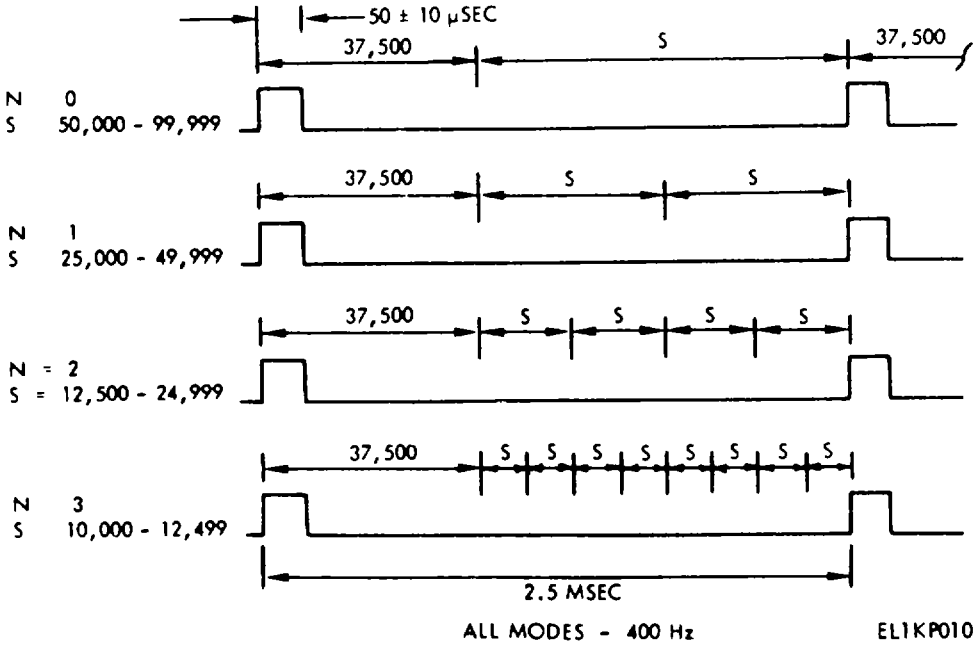


Figure 2-10. Counter divide by 37,500 +2N switch setting modes.

(1) The decade counters used in this application count clock pulses in a normal binary sequence up to a count of 9 (1001) which generates a carry output. The next clock pulse causes the counter to increment to 0 (0000), and the counting sequence is repeated. To achieve a specific count, the counter is preloaded with the 9's complement code for the desired number (see table 2-5). For example, assume a count of 6 is desired. In this case, the counter would be preloaded with the 9's complement of 6, which is a binary 3 (0011). Then, six clock pulses will cause the decade counter to increment to a count of 9, causing a carry output.

(2) Counters U3 through U7 are decade counters that correspond to the least significant digit through the most significant digit, respectively. The counter array receives either the 9's complement of the fixed program constant of 37,500 (which is 62499) or the 9's complement output of the INPUT DATA RATE thumbwheel switch setting via the counter encoder. Counter U8 receives the output of the counter encoder that determines the multiplier; i.e., the number of times the switch selection shall be multiplied. By using 9's complementing, the counter array is preset to the value that will cause the desired number of clock pulses to result in a counter overflow.

Table 2-5. Thumbwheel Switch Coding

Switch setting	9's complement coding
0	1001
1	1000
2	0111
3	0110
4	0101
5	0100
6	0011
7	0010
8	0001
9	0000

(3) Because of the high clock rate, prescaling is required. Prescaler U11 divides by either 10 or 11 depending on whether Ull-3 is high or low, respectively. Counter U3 is loaded with the least significant digit and controls the counting of U11. Prescaler U11 repeatedly counts to 11 until U3 provides a carry out, after which U3 disables itself using the carry output via U1, and U11 provides a divide by 10 function. Transistor Q1 provides the ECL to TTL interface.

(4) To determine how the counter array increments the required number of times for each programmed input, assume a count of 12340 is desired. The 9's complement code for this number is equivalent to a BCD 87659, which would be the initial state loaded into U3 through U7. Since U3 in this case is preset to a count of 9, the carry output (U3-15) would be high, forcing U11 to function simply as a ÷10 counter The output rate from U11 is used to clock the rest of the counters, U4 through U7. U2 is connected to decode a load enable signal to the counters when a count of 8 is reached in U4, and U5 through U7 have all reached a count of 9. At this time, the total number of times that the ÷10 output of U11 has occurred is 9998-8765 (the original state of U4 through U7), or 1233 times, and the total number of input pulses has been 1233 x 10, or 12330 input pulses. Since the load input is now enabled, the counter array will reload on the next output transition from U11, or after 10 more input pulses have been received. Therefore, the total number of input pulses occurring from the time the counter array is originally preloaded to the time the next preload occurs is 12330 + 10, or the desired count of 12340. If the desired count had been 12345, counters U4 through U7 would have functioned in the same manner. However, U3 would have been preloaded to a count of 4 (9's complement of 5), and U11 would have been forced to act as a ÷11 counter 5 times before reverting to a ÷10 counter. Therefore, 5 extra input pulses would have occurred during the process and the total count would have been 12340 + 5, or the desired count of 12345.

(5) The overall timing of the programmable divider is illustrated in figure 2-11 for a switch setting of 16480. At the end of the 37,500 count, flip-flop U9-6 is low, forcing U10-8 high which causes the counter encoder to present the switch setting code to the counter array (U8 through U7) program inputs. When a count of 9998 is reached in U4 through U7, the next clock pulse into the counter array will load the switch program. Since the state of U8 is at 9, the resultant carry output from U8-15 also allows U8 to load a program from the counter encoder into US. The program received by U8 is the 9's complement of the switch setting multiplier plus 1. In this case, the synthesizer is operating in range B (table 2-3), N is 2, and the multiplier 2N is 4. The 9's complement of 4 is 5, so the counter encoder programs U8 with 5 + 1, or 6. The counter array continues to count, and each successive count of 9998 results in reloading the switch setting and advancing the state of US. At the end of the third switch setting count cycle, U8 is advanced to a state of 9 which, in conjunction with the high output of U9-6, satisfies gate U10 and presents a low to the counter encoder from U10-8. This low causes the counter encoder to present the program constant 62,4999 (9's complement of 37,500) to the counter array and a program 9 to U8. The next count of 9998 in U4 through U7 has several effects. The counter encoder program is loaded, and the carry pulse from U8-15 allows U9-6 to toggle back to a low state as well as steering U9-2 high on the next clock pulse. Now, during the 37,500 count, the low output of U9-6 holds U10-8 high even though U8 is in the 9 state, and switch settings are reapplied to the counter array program inputs. The output of U9-2 is

used to control the sample function in the phase detector. This output, which was steered high at the beginning of the 37,500 count, is steered low by U1-2 when a count 6840 is decoded at U2-11. Thus, U9-2 is high for 231 (6480-6249) cycles of the +10 counter (U11) output, resulting in a 52 +10 As pulse which repeats each time the divider process goes through a complete cycle.

(6) The inverters of U12 route the +1, +10, and +100 control signals from the INPUT DATA RATE switches to the divider circuits on the reference divider card.

h. Counter Encoder (fig FO-12). The counter encoder (A3A40), when enabled, gates the 9's complement 20-bit code from the five digital INPUT DATA RATE thumbwheel switches (4 bits per switch) to preload the programmable divider card. When thumbwheel switch inputs are inhibited, the counter encoder output is a binary equivalent of the decimal 62499 (9s complement of 37500). The multiplier control section of the counter encoder is programmed by the three most significant thumbwheel switch settings. These digits are examined to determine proper encoding for the programmable divider multiplier section and the binary counter on the reference divider. When inhibited, multiplier coding is 9 (1001).

(1) Circuits U2 through U4, U7, and U11 through U13 provide for gating of the thumbwheel switch 9's complement code to the programmable divider when enabled by the load signal received via P1-12. Each input is either inverted twice or not at all to produce no change when the counter encoder is enabled by a high on P1-12. The NAND and AND gates, however, provide a binary equivalent of the decimal 62499 to the programmable divider when the switch inputs are inhibited by a low on P1-12. The outputs are tabulated in table 2-6.

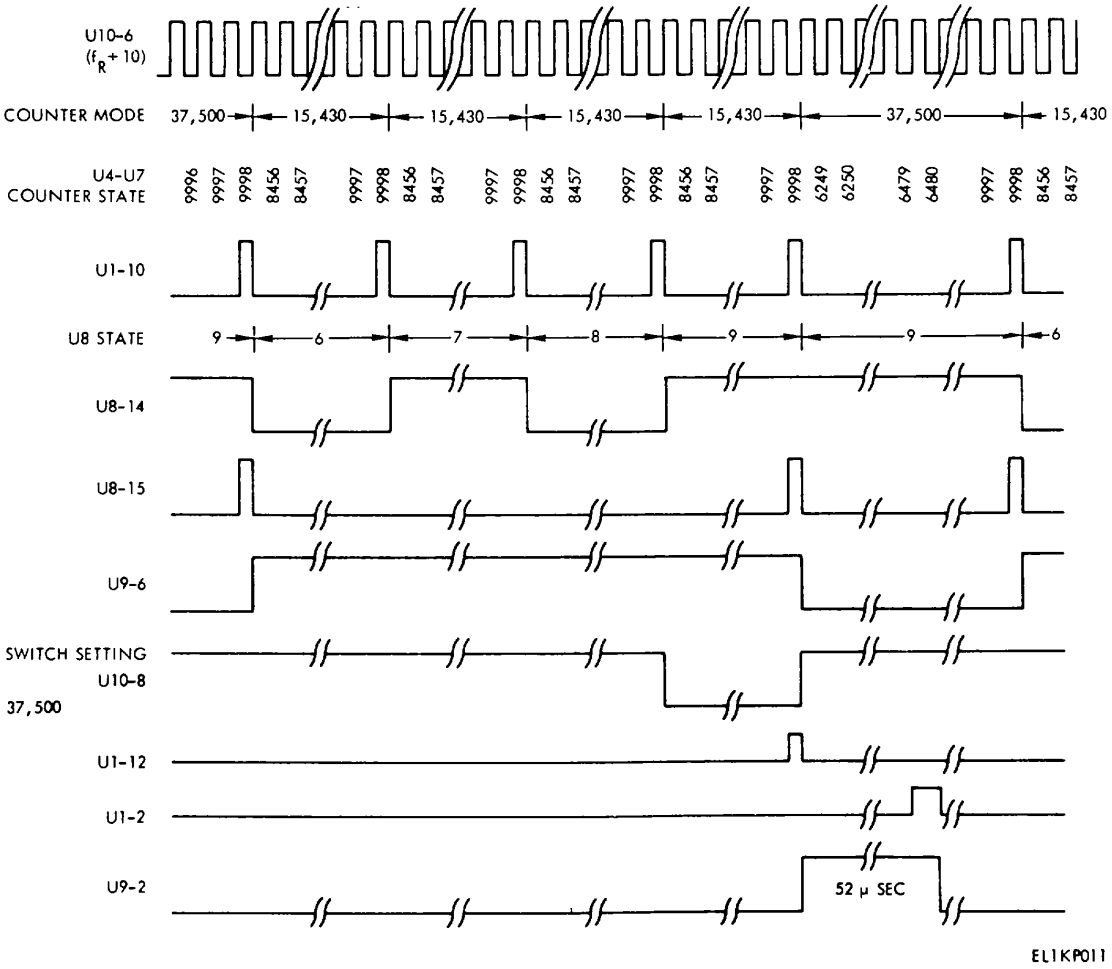


Figure 2-11. Programmable divider, timing diagram.

Table 2-6. Counter Encoder Program Outputs.

Digit	Bit	Pin	(P1-12 low) constant code
	2*	P1-31	1
1	21	P1-26	0
(least significant)	2'	P1-62	0
	2'	P1-67	1
	2'	P1-33	1
	2'	P1-28	0
2	2'	P1-64	0
	2'	P1-82	1
	2'	P1-39	0
	2'	P1-7	0
3	2'	P1-9	1
	26	P1-6	0
	2'	P1-8	0
	21	P1-45	1
4	2	P1-18	0
	2'	Pl-55	0
	2'	Pl-57	0
	21	P1-ll	1
5	2'	P1-48	1
(most significant)	2	P2-21	0

(2) To program the multiplier section of the programmable divider and for control of the binary counter on the reference divider, 4-bit digital com- parators U1, U6, U6, U8S, U9, and U10 are used to examine the three most significant digits of the thumbwheel switch outputs. Output changes occur at the 50,000, 75,000, and 87,500 points of the 9's complemented binary input to the counter encoder (see table 2-7).

(3) The digital comparators are arranged to detect these numbers and provide the correct output code. Comparator U8 controls the change at the 50,- '000 point. The most significant thumbwheel switch digit (4-bits) is applied to the AO through A3 inputs of the comparator and the B inputs are tied to a fixed count of 5 (binary 1010). Since the A > B input (pin 4) to this comparator is high while the other cascade in- puts are low, an A = B output is impossible. The com- parator A> B output goes high when the most signifi- cant digit is equal to or greater than a binary 5 (switch setting >4). The code change occurring at 75,- 000 is detected by comparators U5 and U9 connected in cascade. Connections to U5 are identical to those of U8 except the second most significant digit is examin- ed for a 5 or greater. The outputs of U5 are connected to the cascade inputs of U9 while the AO through A8 inputs are connected to the most significant digit. The BO through B8 inputs of U9 are connected such that the comparator examines inputs for a magnitude equal to or greater than 7. The code change of 87,600 is similarly detected by cascaded comparators U1, U6 and U10 which are connected to detect the digits 5, 7, and 8, respectively. Gates U14 and U16 provide the appropriate output codes to the synthesizer as indicated in table 2-8.

i 15-MHz Amplifier (fig. FO-18). The 15-MHz amplifier card (A3A46) contains a current-to-voltage amplifier, an RF amplifier, a bandpass filter, and an attenuator. The current-to-voltage amplifier receives the control input from the bit synchronizer and provides a correction voltage to the 15-MHz VCO. The remainder of the circuits on the card receive the out- put of the VCO and provide amplification and filter-

Table 2-7. Counter Encoder Range Decoding.

Range	Thumbwheel switch settings	Counter encoder binary inputs	Comparator outputs					
			US-7	US-5	U9-7	U9-5	U10-7	U10-5
A	10000 to 12499	89999 to 87500	0	1	0	1	0	1
B	12500 to 24999	87499 to 75000	0	1	0	1	1	0
C	26WO to 49999	74999 to 50000	0	1	1	0	1	0
D	50000 to S99	49999 to 00000	1	0	1	0	1	0

Table 2-8. Multiplier and Divider Control Outputs.

Range	N	2N	Z	Multiplier program Z 9's complement of 2N + 1				Binary counter control (+2N + 1			
				P1-71	P1-61	P1-29	P1-35	+2 P1-58	+4 P1-24	+8 P1-60	+16 P1-46
A	3	8	2	0	0	1	0	1	0	0	0
B	2	4	6	0	1	1	0	0	1	0	0
C	1	2	8	1	0	0	0	0	0	1	
D	0	1	1	0	0	0	0	0			
P1-12 low	-	-	9	1	0	0	1-	-	-	-	

ing of the 15-MHz input to the mixer.

(1) The current-to-voltage amplifier, AR1, receives the control current output of the bit synchronizer digita/analog converter. AR1 produces an output voltage proportional to the input current with a scale factor of 3.8 V/mA. The resultant correction voltage output from AR1 is routed to the control in- put of the 15-MHz VCO.

(2) The output of the 15-MHz VCO is received through a 6-dB attenuator formed by resistors R14, R15, and R16 and applied to the two-stage RF amplifier. This is the same type amplifier as used ;n the 45 MHz amplifier except that it has no input operational amplifier stage; therefore, the gain is fix- ed at approximately 24 dB. The amplifier output, at approximately 19 dBm, is applied across a 6-dB attenuator formed by resistors R1, R5, and R6 to bandpass filter FL1. The filter center frequency is 15 MHz, the 20-dB bandwidth is 9 MHz, and the 40 dB bandwidth is 15 MHz. The filter output is applied through 3-dB attenuator R2, R7, and R8 to the mixer/output amplifier.

j. Maxer/Output Amplifier (fig. FO-14). The mixer/output amplifier card (A3A46) contains a double balanced mixer that accepts a 45 ±10 MHz input and a 15-MHz input to develop a 30 ±10 MHz output The card also contains a three-stage RF amplifier and attenuators for matching and level setting The out- put (20 to 40 MHz) is routed to a low pass filter on the reference oscillator card.

(1) The high level 456 10 MHz input is applied across a 2 dB attenuator formed by R8, R11, and R12, and provides a +7 dBm input to mixer U1. The 15 MHz input is applied across a 6 dB attenuator formed by R23 through R25 to provide a 0 dBm input to the mixer. The difference frequency output, 20 to 40 MHz, is applied across a 26-dB attenuator formed by resistors R9, R10, and R13 through R16 to the RF amplifier.

(2) This three-stage amplifier is identical to the circuit used on the 45 MHz amplifier card. The amplifier output is applied through a low pass filter on the reference oscillator card to the programmable decade and binary counters on the reference divider card.

k. 15-MHz VCO. The 15MHz VCO, Y2, is a Vectron Laboratories, Inc., VCO part number 272-1208.
The center frequency stability is 1 kHz/day. The con- trol voltage input is +5.0 volts peak, producing a deviation of ±200 kHz. A screwdriver adjustment permits maintenance adjustment of center frequency.

2-6. Encoder and Interface

a. General

(1) The encoder switch section of the encoder and interface (fig. FO-15) permits selection of bit sync data or bypass data, provides differential encoding when selected, and provides gating for selection of externally error coded data, internally generated PN sequence data, or data with no error coding. Selection between biphase modulation or quadraphase modulation is also made by the coder switch section. The coder interface section contains the line drivers and receivers required to interface with an external error encoder.

(2) Bypass data from the input circuits and data from the bit synchronizer are applied to the input gates of the randomizer/derandomizer. When the STD/CLK/ICF switch is in the CLK position, bypass data is gated to the randomizer logic; in either of the other switch positions, bit synchronizer data is gated to the randomizer logic If the randomizer logic is enabled (RANDOMIZER TRANSMIT switch in ON position), the selected bit synchronizer or bypass data is altered by the randomizer logic to produce a near random data stream. When the RANDOMIZER TRANSMIT switch is OFF, the selected input data stream bypasses the randomizer logic and is unaltered

(3) Data from the randomizer data output circuit is applied to the input data gates of the encoder switch. The input data gates serve as a buffer, with both inputs of the multiplexing function connected to the randomizer output. If the differential encoder is enabled (DIFF ENCODE switch in ON position), each data ONE bit received at the input develops a transition at the output while each data ZERO bit produces no transition. When the DIFF ENCODE switch is set to OFF, the data passes through the encoder unchanged except for a one-bit period delay. The output of the differential encoder is applied to the BPSK enable gates. If the modulator is in the biphase mode, the output from the differential encoder is applied to both the I and Q channels of the modulator along with bit rate clock. The output from the differential en- coder is also supplied to the coder interface and thence to the external coder. Data from the input data gates of the encoder switch is also applied to the data demultiplexer which converts the one serial data stream into two parallel data streams. These two data streams are clocked out of the data demultiplexer at 1/2 the clock rate. When the modulator is operating in the QPSK mode without external encoding, the QPSK enable gate transfers the parallel outputs from the data demultiplexer to the I and Q channel inputs of the modulator through the OR gates. The I and Q channel outputs are displaced from each other by 1/2 bit period so that the data transitions do not coincide.

(4) Data, bit rate clock, and two times bit rate clock are routed via the coder interface to an external coder. If the TRANSMIT ERROR CODING switch is set to EXT, externally coded data (symbols) and accompanying clock are returned via the coder interface

and applied to the modulator via the OR gates. Any of the external coder interface clock signals may be inverted by switches located on the coder interface card. When external coding is not selected, the externally coded data and accompanying clock are disabled. Both of the data streams (symbols) from the external coder are gated at two times the symbol rate to develop I and Q outputs which are displaced from each other by a 1/2 bit period. The QPSK/BPSK switch selects the output of the offset gate (when operating in the error coded QPSK mode) or the out- put of the I channel gate (when operating in the error coded BPSK mode) as the Q channel data stream.

(5) Self-test provisions have also been made so that two PN sequences can be used as modulator inputs when the PN sequence enable gate has been activated. The activation of the appropriate enable gate is controlled by the switching logic in response to front panel switch settings.

b. Randomizer/Derandomizer (fig. FO-16). The randomizer/derandomizer (A3A33) receives transmit data from either the bit synchronizer or directly from the input interface. The serial data stream is then randomized or not randomized, depending on the setting of the RANDOMIZER TRANSMIT switch

(1) When the STD/CLK/ICF switch is in the CLK position (P1-21 grounded), bypass data from the input interface is gated from U2-1 to U2-6 When the STD/CLK/ICF switch is in the STD or ICF positions (P1-21 at logic ONE), transmit bit syn- chronizer data on U2-13 is gated to U2-6

(2) The randomizer shift register (U4 and U5) and associated binary counters (U7 and U8) are enabled whenever P1-48 is low. This applies a logic ONE via U1-10 to the clear inputs of U4, U5, U7 and U8.
Conversely, a logic ONE at P1-48 disables the randomizer logic by applying a low to the clear inputs of U4, U5, U7 and U8.

(3) The randomizer is formed by the modulo-2 addition of the input data stream with the modulo-2 addition of' the ninth and eleventh stages of the sixteen-stage shift register U4 and U5. With the randomizer logic disabled, the shift register outputs are all low, thus U3-U12 and U3-13 are low, which causes a low at U3-2. Pin 15 of U8 is also low because counter tJ8 is held in a cleared state, therefore U3-3 is low. With U3-3 and U3-2 both low, U3-4 is low, causing data applied at U3-5 to be non-inverted. This noninverted data is routed to U6'-2 where it is clock- ed through flip-flop U6 to P1-59.

(4) When the randomizer logic is enabled, binary counters U7 and U8 are used to ensure that on all ZERO's data input to the randomizer shift register results in a randomized data output. With the shift register starting at a cleared state (all outputs low), the outputs at U3-11 and U3-6 will be low as data logic ZERO's are applied to U3-5. While U3-11 remains low, binary counter U7 and U8 is stepped (counted up) by incoming clock pulses. The output at U3-6 will remain low until the binary counter , reaches the maximum count and a carry is generated at U8-15 The carry causes U3-3 to go high, which drives U3-6 high The carry pulse starts the randomizer shift register, and the output sequence is a 2047 bit maximal length sequence The carry pulse x from U8 is generated only once for an all logic ZERO's input, and 256 ZERO's are required to produce a carry. The 2047 bit sequence has only ten consecutive bits at logic ZERO

c Encoder Switch (fig. FO-17) The encoder switch (A3A6) receives transmit data directly from the randomizer/derandomizer and, if selected, provides differential encoding The one serial data stream required for BPSK or the two parallel data streams required for QPSK are also generated and gated by the coder switch

(1) Data from the randomizer/derandomizer is applied to inputs P1-5 and P108. This data can be-either bypass data or data from the transmit bit synchronizer. When the STD/CLK/ICF switch is in the CLK position (P1-9 grounded), output pin 2 of inverter U4 is high to enable pin 10 of AND gate U6. In this mode, bypass data from the randomizer/deran- domizer card is gated to the differential encoder formed by adder U7 and one flip-flop section of U8 and the transmit bit sync data input (P1-5) is disabled. In any other switch position, transmit bit sync data from the randomizer/derandomizer is gated to the differential encoder Bit rate clock is always pre- sent at P1-46 and twice bit rate clock is always pre- sent at P1-11 The inverters of U3 and U4 and variable capacitor C1 provide a delay and duty cycle adjustment for the twice bit rate clock to the external coder interface.

(2) When differential encoding is selected (DIFF ENCODE switch is set to ON), ground is applied through P1-6 to the pin 3 input of adder U7. Since this adder is also grounded at a second input (pin 4) and data is applied to the third (pin 1), the sum output will be the same as the data input Thus, JK flip-flop U8 will toggle each time a negative clock transition occurs when data is a logic ONE and will not switch when data is a logic ZERO. If differential encoding is not selected, a logic ONE is applied to one input of the adder (pin 3). In this mode, the data is added to ONE (effectively inverted) and the result is applied to the K input of the flip-flop. Thus, the data simply shifts through flip-flop U8 The Q output of U8 is routed via P1-7 to the external error correcting coder and is also applied to pin 12 of AND gate U6

(3) The output from the input data gates (U6-6) is also applied to the four inputs of JK flip-flop U13.
The 1/2 clock rate outputs from U8 pins 9 and 7 serve as the clock inputs to U13. The outputs of U13 pins 5

and 9 are the demultiplexed and differentially en- coded I and Q channel inputs to the QPSK modulator. Alternate data bits from U6-6 are clocked into the flip-flops of U13 by the outputs of U8. Thus the out- puts of U13 (pins 5 and 9) will change state only when the alternate data bits being gated in by the outputs of U8 are high.

(4) When the external error encoder is being used, the coded I channel, Q channel and twice clock signals are received at P1-65, P1-22, and P1-14, respectively. The I and Q signals are clocked through the D flip-flops of U16 by the twice bit rate clock. The inverted I channel signals from U16-6 are forwarded to the modulator through U12. After being clocked through U16, the Q channel signal is applied to the offset gate U9-2 where it is delayed for an additional half bit period so that the I and Q channel bit transitions are separated by one-half bit period. The inverted Q channel signals from U9-6 are applied to the QPSK/BPSK gate. For biphase operation, U14-2 is high and U14-9 is grounded. The I channel signal from U16-6 is then also applied to the Q channel modulator through U14-6 and U12-8. For quadraphase operation, U14-2 is grounded and U14-9 is high so that the Q channel signal from P1 -22 is applied to the Q channel modulator through U9-6, U14-6, and U12-8.

(5) Selection of the modulator input signals is provided by front panel switches through the switching logic of U4 and U11 BPSK operation is selected by grounding P1-13, which enables U6-11 and U10-11 so that the data is applied to both the I and Q channels of the modulator along with bit rate clock If differentially coded BPSK is desired, P1-6 is also grounded For BPSK operation with differential coding and external error coding, P1-15 must also be grounded In this case, U6-11 and U10-ll are disabled, the differentially coded data stream is routed from U8-3 to the encoder, and the error encoder out- put returns to U16-2 The BPSK data (from U16-6) is supplied to the I channel input of the modulator through U12-6 and is supplied to the Q channel input of the modulator through U14-3, U14-6, and U12-8.

(6) To select QPSK operation, P1-13 is high so that the differentially coded I and Q channel data from U13-5 and U13-9 is supplied to the I and Q channel inputs of the modulator. When in the QPSK mode, the data is always differentially coded. When the external error coder is used with QPSK, P1-15 is grounded so that data (I and Q channel) from the external coder is applied to U16-2 and U16-12. The I channel data is applied directly to the modulator through U12-6. The Q channel data is delayed by one-half bit period and is then routed to the modulator through U14-8, U14-6, and U12-8.

(7) When P1-16 is low (self-test), the BPSK and QPSK gates are disabled and a PN sequence is applied to the modulator through U10-3 and U10-8. The PN sequence and accompanying clock are supplied through P1-23, P1-24, and P1-25. U5 and U9 develop the bit rate clock used to drive the PN sequence generator (P1-71) and the twice bit rate clock to the modulator (P1-30). Twice bit rate clock is externally jumpered from P1-35 to P1-24.

d. Encoder Interface (fig. FO-18). The encoder interface (A3A27) card provides the interface between the QPSK/BPSK modem and the external error coder.

(1) Circuits U1 through U5 are identical dual line drivers that convert logic inputs to differential out- puts. Line drivers U1 and U2 accept logic level data and clock from the coder switch and provide differential outputs to the coder. A logic ONE is the off state of the driver and a logic ZERO is the on state (fig. 2-12). A logic ONE is zero volt while a logic ZERO is between -70 and -135 millivolts, and the drivers have a current sink of between 3.5 and 7 milliamperes.

(2) Line receivers U6 and U7 receive differential input signals such as those generated by line drivers U1 through U5, and produce TTL logic compatible outputs. The outputs switch when a differential input voltage of 25 millivolts is received. Line receivers U6 and U7 are enabled by a high on pin 6 only 'when the TRANSMIT ENCODER switch is in the EXT position. Otherwise, the outputs remain high when a low is applied to pin 6.

(3) Switches S1 through S6 provide the capability of inverting the appropriate balanced input/output signals. On all switches, position 1 provides the normal polarity and position 2 provides the inverted polarity.

2-7. RF Modulator

a. General. I channel data, Q channel data, and clock from the coder switch are applied to the input flip-flops of the QPSK/Bi K data receiver and modulator (fig. FO-19). The two NRZ data streams are converted to a bipolar form such that the data switches between +0.5 volts to drive the two double balanced mixers. To develop the two 90-degree phase quadrature inputs required at the mixers, the output of a 70-MHz crystal osciallator is applied to the input port of a quadrature hybrid power divider The quadrature outputs of the hybrid are phase modulated by the bipolar data signals in the double balanced mixers. A resistive delta pad is used to sum the two mixer outputs to obtain the desired biphase or quadraphase PSK signal For biphase operation, the I and Q data streams are identical. In the quadraphase mode, the I and Q data streams to the mixers are different and are offset one from the other by half a bit period.

(1) The quadraphase or biphase modulated

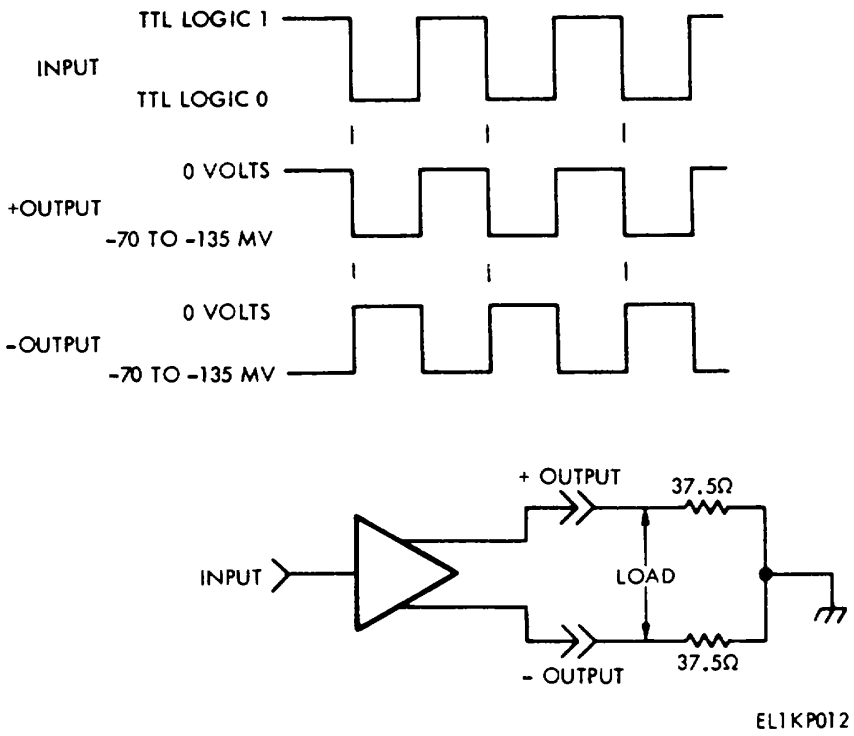


Figure 2-12. Encoder interface output.

carrier signals from the combiner are then amplified and relay switched through the modulation filter. For low data rates, neither relay is energized and the modulated carrier is routed through the 3 MHz band- pass filter. At high data rates, K2 is energized and both filters are bypassed. Between these extremes, K1 is energized, K2 is deenergized, and the modulated carrier is routed through the 12 MHz bandpass filter.

K1 and K2 are switched by the relay control (A3A32) which detects the settings of the TRANSMIT DATA RATE and TRANSMIT ERROR ENCODING switches to provide relay control as shown in table 2-9. The output of the modulation filter is amplified and routed to the rear panel connector and the internal test relay. The amplifier output is monitored via a peak detector and comparator. If the output power level falls below a preset value, a transmit power fault alarm signal is developed.

(2) A peak detector and comparator are also used to monitor the 70-MHz crystal oscillator. If the power level falls below a threshold value, a modulator test fault is developed. Similarly, the bipolar data inputs to the mixers of the modulator are constantly monitored. If data is present at the mixer inputs, the average dc voltage will be zero. However, if data is 2 not present at the modulator input, or if a failure has occurred, the average dc voltage will be ±0.5 volt, then, the loss of data detector will develop a fault indication. This loss of data indication is OR'ed with the oscillator fault indication to develop a modulator test fault indication.

b. QPSK/BPSK Data Receiver and Modulator (fig. FO-20). The QPSK/BPSK data receiver and modulator card (A2A1) uses the NRZ baseband data and clock to biphase or quadraphase modulate a 70- MHz carrier. Also contained on this card is a monitor circuit to determine if the NRZ data streams have been level converted and are driving the double balanced mixers which are used as the phase modulators. A single 70-MHz carrier is received by this card and is divided into two quadrature components for application to the phase modulators.

(1) The flip-flops of U3 receive and shape the I and Q channel baseband data from the encoder switch. The clock signal accompanying the data signals is used to clock the flip-flops of U3. When the modulator is operating in the biphase mode, the I and Q channel inputs are identical (A, fig. 2-18). For the quadraphase mode, the I and Q channel data streams are different and offset by one-half bit period (B, fig. 2-13). The dual 50-ohm line drivers of U6 receive the I and Q channel data from U3 and drive the level converters. For the I channel data, the level converter is composed of CR10-14, R80, R83, R84 and R86. This level converter shifts the TTL levels from pin 8 of U6 to a bipolar signal that swings +0.5 volts at pin 4 of

Table 2-9. Modulator Filter Selection.

Operational configuration	Data rate	K1 status	K2 status	Filter bandwidth
BPSK no EXT encoding	16 kb/s to 999 99 kb/b	D	D	3 MHz
	1 Mb/s to 2 4999 Mb/s	E	D	12 MHz
	2.5 Mb/s to 9 9999 Mb/s	E	E	No filtering
BPSK EXT encoding	16 kb/s to 499 99 kb/s	D	D	3 MHz
	500 kb/s to 1 2499 Mb/s	E	D	12 MHz
	1 25 Mb/s to 4 9999 Mb/s	E	E	No filtering
QPSK no EXT encoding	50 kb/s to 1 2499 Mb/s	D	D	3 MHz
	1 25 Mb/s to 4 9999 Mb/l	E	D	12 MHz
	5 Mb/s to 19 999 Mb/s	E	E	No filtering
QPSK EXT encoding	50 kb/s to 499 99 kb/s	D	D	3 MHz
	500 kb/s to 2 4999 Mb/s	E	D	12 MHz
	2.5 Mb/s to 9 9999 Mb/s	E	E	No filtering

D - Deenergized
E Energized

U7. Therefore, the double balanced mixer, U7, acts as 0 or 180 degree phase shifter to the 70-MHz signal at pin 1 of U7 For the Q channel data, the level converter is composed of CR1-4 and CR6, R1, R2, R4, and R7.

(2) A 70-MHz carrier at +10 dBm is applied to P1-13 The quadrature hybrid, U4, power divides the 70-MHz input carrier and routes one of the output signals (U4-2) to U2. A second output signal (U4-3), is phase shifted by 90 degrees relative to the U4-2 out- put and applied to the I channel double balanced mixer (U7-1). The resulting phase modulated signals from U2-6 and U7-6 are summed together by the resistive combiner composed of R48, R49, and R52, amplified by AR2, and applied to the modulation filter via P2-8. The BPSK and QPSK modulation waveforms are shown in figures 2-14 and 2-15, respectively.

(3) The converted I and Q channel data streams into the mixers, U2 and U7, are constantly monitored by two loss of data detectors Since these are identical, only the loss of data detector associated with U7 is discussed If a data input is present at U7-3. the average dc voltage will be zero If the data input is interrupted or a failure occurs, the voltage at U7-3 will be plus or minus 0 5 volt. Resistor R81 and capacitor C8 form a loss pass filter which time averages the data signal at the U7 input AR3 receives the filter output, provides a gain of 10, and drives the dual comparator, U5 Normally, the outputs of U5 will be low, indicating that the AR3 output is more positive than -0.9V but less than +0.9V If the output of AR3 goes more negative than this normal range, U5-12 will become high, indicating that U7-3 is constantly at +0 5 volts and data is not present. Similarly, if U7-3 is always -0 5 volts, U5-7 will become high indicating that no data input is present at U7-3. The circuits of AR1 and U1 monitor the data input to U2 and provide a high level output whenever a data signal is not present at U2-3 Diodes CR5 and CR7 through CR9 perform an OR function such that P2-23 is high whenever pin 12 or 7 of either U1 or U5 go high and is low only when pins 7 and 12 of both U1 and U5 are low.

c 70-MHz Crystal Oscillator (fig FO-21). The 70-MHz oscillator card (A2A2) contains a stable crystal oscillator (tolerance of :0 001 percent). Also included on this card is a status monitoring circuit that provides an indication if the modulator is not processing transitions or if the 70-MHz oscillator output power drops below 0 dBm

(1) The oscillator output is detected by the peak detector comprised of CR1, L2, and C5' The detected output is compared to a 200 mV reference voltage derived by R5 and R4. Thus, when the peak detector output falls below 200 mV, the output of AR1 will switch to a positive voltage This signal, applied through CR2 to AR2, is ANDed with the status signal ',P1-21) from the data receiver and modulator. The status signal from the modulator is positive when no modulation is present. If either the modulator signal is positive or an oscillator failure signal from AR;1 is

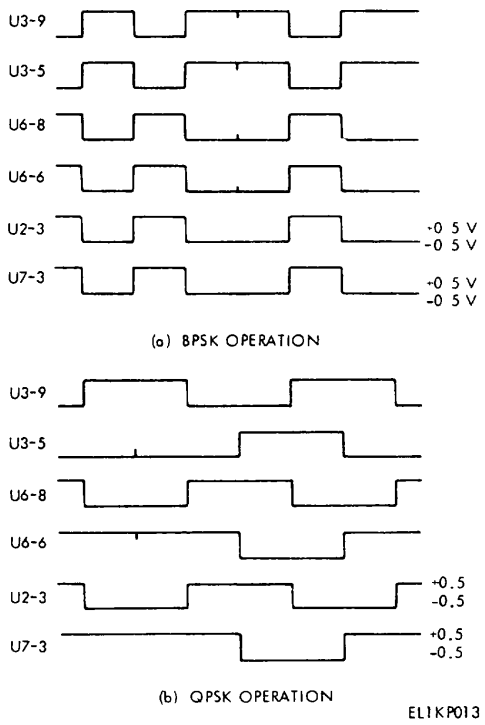


Figure 2-13. Data receiver and modulator, timing diagram.

positive, the resulting positive voltage across R9 will cause the output of AR2 to go to a positive voltage.
This positive output voltage causes the TRANSMIT MODULATOR TEST indicator on the front panel to be extinguished.

d. Modulation Filter (fig FO-22) The modulation filter (A2A26) accepts a 70-MHz QPSK/BPSK modulated input signal (P1 -27) and routes it through relays to a filter or a power matching pad When relays K1 and K2 are deenergized, the modulated in- put signal is fed through 3-MHz bandwidth filter FL1 and out (P1-24) to the 70-MHz output amplifier. If relay K1 is energized and relay K2 deenergized, the input signal is fed through 12 MHz bandwidth filter FL2. If relay K2 is energized, the input signal is fed through the 10 dB power matching pad to the 70-MHz output amplifier. Filter selection is based upon data rate, QPSK/BPSK operating mode, and external encoder selection. When the 10-dB pad is selected (K2 energized), band limiting is performed by the 70-MHz output amplifier.

e. 70-MHz Output Amplifier (fig. FO-23). The 70-MHz output amplifier (A2A27) receives the QPSK/BPSK modulated signal from the modulation filter This input (P1-27) is fed through a 6 dB im- pedance matching pad to wideband amplifier AR1, which is the first stag(of a three-stage amplifier. AR1 has a bandwidth of 120 MHz with gain adjustable by R28. The output from the first stage is transformer-coupled to two successive stages of common-emitter amplifiers, Q1 and Q2, respectively. Each stage has a bandwidth in excess of 40 MHz with 70 MHz being the center frequency. The output of the last stage is transformer-coupled through a 2-dB im- pedance matching pad (R31, R34, R35) to the output, P1-10. The output signal power monitor is composed of peak detecting diode CR1, operational amplifier AR2, and comparator AR3. The voltage derived from the peak detecting diode is amplifier by AR2 and routed to the comparator, AR3. A reference voltage of +2.9V dc is derived from the resistive network formed by R42 and R43 and applied to the inverting input of the comparator. The negative peak detected voltage is inverted by amplifier AR2 and applied to the non-inverting input of comparator AR3 For any output power level in excess of +16 dBm, the voltage at the noninverting comparator input is more positive than the reference, and the comparator output is positive. When the voltage at the noninvertlng comparator in- put is less than the reference, the comparator output voltage goes to ground This output signal (P1-3) is used to activate the TRANSMIT PWR FAULT indicator and audible alarm on the front panel.

2-8. RF Demodulator

a. General. The RF demodulator (fig. 2-16) accepts the noisy IF signal, phase locks an internal carrier reference to the input signal, and uses the carrier reference to demodulate the input and provide a noisy baseband output signal to the receive bit synchronizer

(1) The noise on the 70-MHz input signal is band-limited by the input filter and the remaining signal and noise is fed to the 70-MHz gain controlled amplifier The signal is then mixed with a 48.6-MHz signal from the voltage controlled crystal oscillator. The resulting difference signal (21 4 MHz) is separated and applied to two filters in a selectable filter array. One output signal from the filter array is amplified and divided again. These two signals are then used as the inputs to the I and Q channel data detectors. The second signal from the filter array undergoes narrower filtering to further improve the signal-to-noise ratio and is used as the input to the carrier recovery and AGC loops.

(2) The amplified narrowband signal is applied to an envelope detector, the output of which drives the AGC amplifier. The gain control loop is closed by comparing the envelope detector output to a fixed reference level in the AGC amplifier, amplifying the difference, and applying the resultant output back to

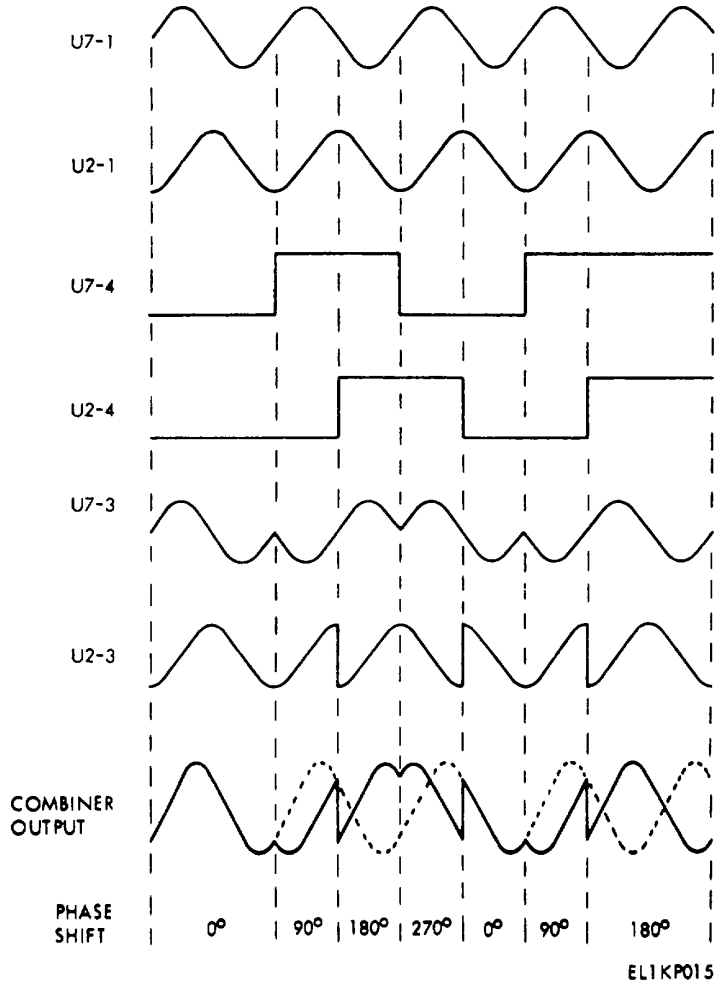


Figure 2-14. Modulation waveforms for BPSK operation.

the 70-MHz gain controlled amplifier for level correction.

(3) The times two multiplication process performed on the biphase shift key modulated IF signal results in an unmodulated carrier output at twice the 21.4 MHz IF center frequency, or 42.8-MHz. The 42.8-MHz signal is filtered to remove any unwanted harmonics and applied to a phase detector and loop amplifier for BPSK operation. Similarly, a second doubling process is performed on the 42.8-MHz out- put of the first doubler and results in an unmodulated carrier output at four times the 21.4-MHz IF center frequency, or 85.6 MHz, for QPSK operation. The 85.6-MHz signal is filtered and applied to the phase detector and loop amplifier.

(4) The phase detector compares this signal (42.8 MHz for BPSK, 85.6 MHz for QPSK) with the doubled or quadrupled output of a stable 21.4 MHz crystal oscillator. Any difference between the two signals results in an error voltage at the output of the phase detector. This error voltage is fed back to control the phase of the 48.6-MHz VCXO, forming a phase lock loop. The loop functions as a narrow band tracking filter with the 21.4 MHz crystal oscillator output being the desired coherent reference. The loop bandwidth is changed when the QPSK/BPSK modem is switched between BPSK and QPSK operation. However, within either mode of operation, the loop bandwidth remains unchanged regardless of bit rate changes.

(5) In the coherent detector, an additional 42.8 or 85.6 MHz output from the reference oscillator times two/times four multiplier is shifted 90° in phase and is compared with the 42.8 or 85.6 MHz signal

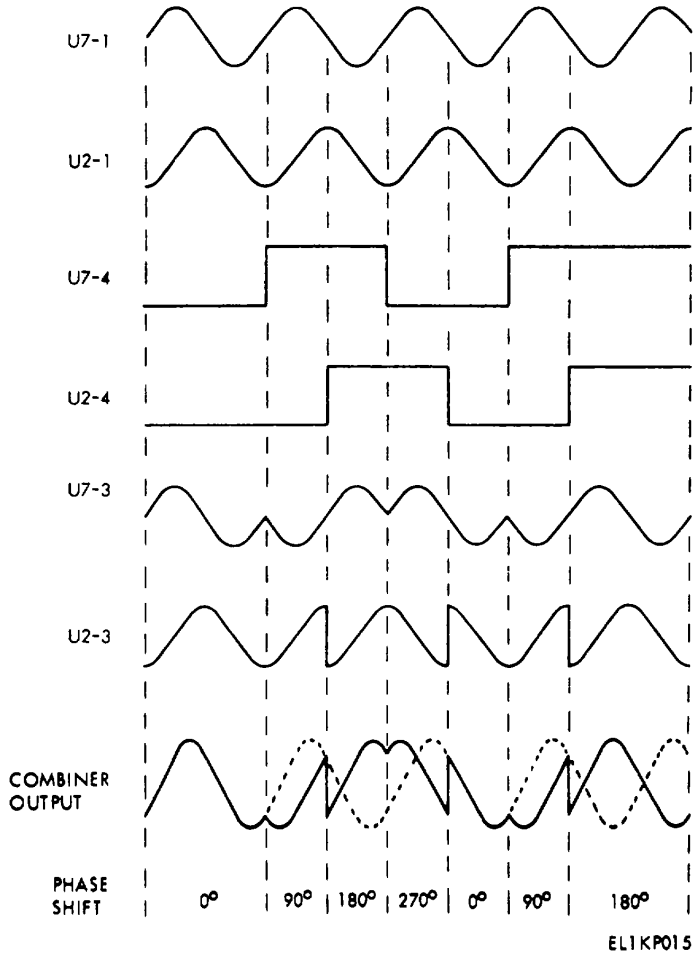


Figure 2-15. Modulation waveforms for QPSK operation.

developed from the narrowband filter output of the X2/X4 multiplier. The coherent detector, therefore, develops an output that is shifted 90 degrees with respect to the output of the loop phase detector. Thus, the output of the coherent detector will be at a maximum when the loop is locked. The coherent detector contains a level detector which disables the sweep circuit when the loop is locked. The level detector also controls the sweep generator such that when the loop is not locked, sweep action is initiated for reacquisition.

(6) In both the I and Q channels, the phase detector used for the data detector is a double balanced mixer. At the inputs to the data detector, the required phase relationship between the IF signal and the reference oscillator is maintained by using a programmable electronic phase shifter to precondition the 21.4-MHz reference input to the data detectors. Each phase detector output is applied to a buffer amplifier which provides isolation and short circuit protection, as well as power gain.

b. Description.

(1) Maximum receiver sensitivity is obtained by opening switch S1 (fig. FO-24) on the input filter card to deenergize relay (K1) which bypasses the 20-dB attenuator. With the attenuator bypassed, the demodulator will accept input signal levels from -75 dBm to -20 dBm. For input signals which are expected to vary from -55 dBm to 0 dBm, switch S1 is left closed, and the 20 dB attenuator is inserted in the signal path. Thus, the maximum and minimum power levels applied to the gain controlled amplifier input are the same in either case.

(2) The 70-MHz input is band limited by one of two filters. A 4-MHz bandpass filter is used at low data rates. A 50-MHz bandpass filter is used at high

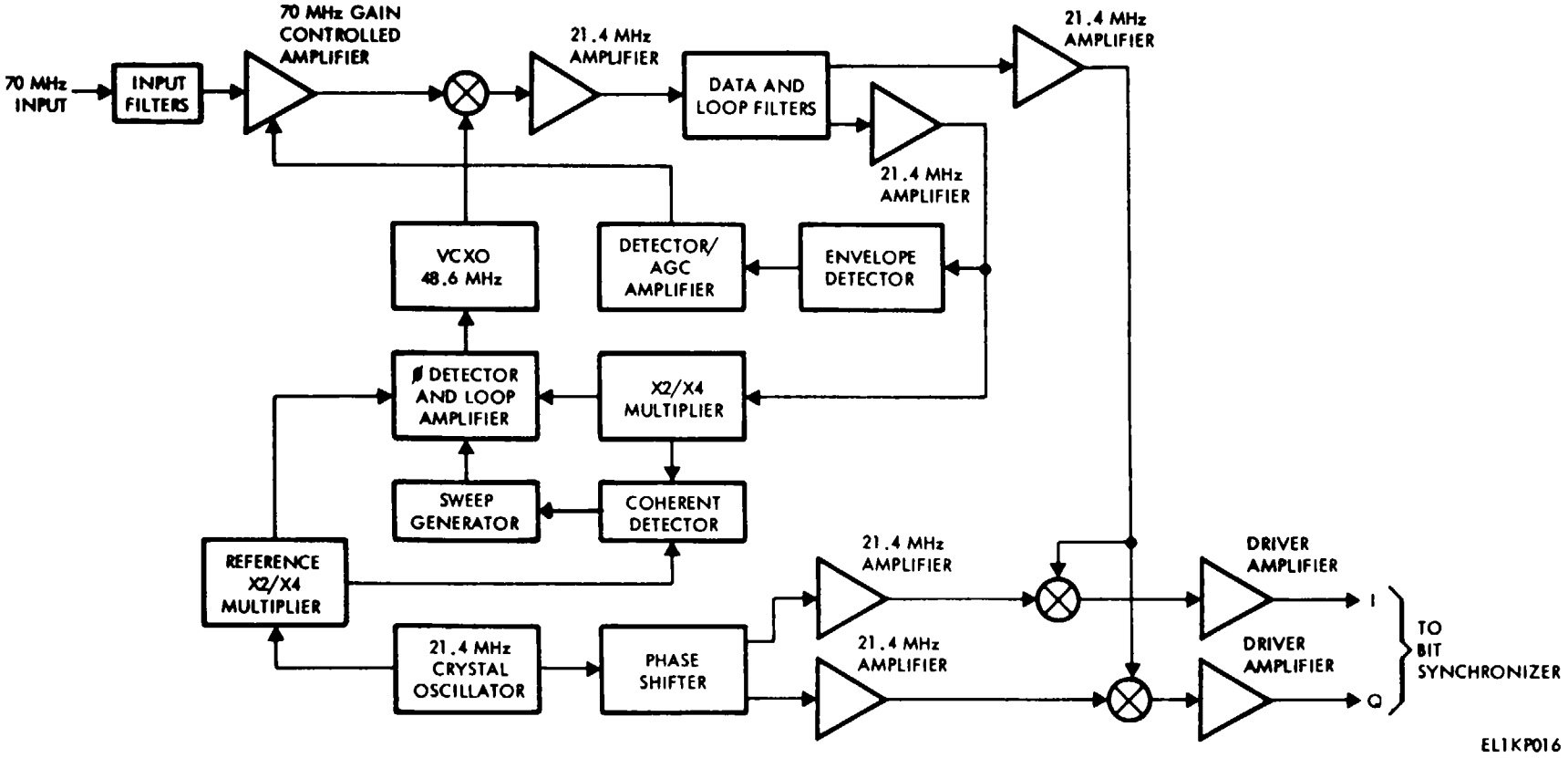


Figure 2-16. RF demodulator, general block diagram.

data rates. Relay K2 switches the filters depending on the I CHANNEL SYMBOL RATE range switch set- ting. Relay K2 is activated by relay driver U21 on the relay control card.

(3) The AGC loop provides an appropriate input voltage to the gain controlled amplifier to maintain a constant power level out of the amplifier. The signal is then down converted to a 21.4-MHz center frequency, and applied to a 40-MHz lowpass filter. The low- pass filter removes any 48.6-MHz local oscillator leakage that may be present at the mixer output, as well as the sum output of the mixer, leaving only the 21.4-MHz difference. The 21.4-MHz signal is then amplified and applied to a power divider which provides two identical outputs.

(4) The outputs of the power divider are used to develop two signals: a narrowband signal (filtered with a bandwidth of 1 to'4 times the symbol rate) which is used to stimulate the AGC and phase lock loops, and a wideband signal (filtered with a bandwidth of 4 to 16 times the bit rate) which is used to develop the baseband output. The filtering is obtained by applying the 70-MHz GCA outputs to an array of filters and relays located on the filter and distribution amplifier card. The filter switching is controlled by relay drivers on the relay control card which, in accordance with the I CHANNEL SYMBOL RATE and RECEIVE QPSK/BPSK switch settings, energize the appropriate relay drivers. The resultant bandwidths and signal paths are summarized in table 2-10. For I CHANNEL SYMBOL RATE switch set- ting of 2.5 Mb/s the wideband filtering is provided by the 40-MHz lowpass filter (FL3) of the 70 MHz GCA and by various amplifier stages.

(5) The narrowband signal level is detected and applied to the AGC Amplifier. The AGC amplifier compares the detected level with an internal reference level, and closes the AGC loop by applying the amplified difference signal signal back to the gain controlled amplifier for correction.

(6) The narrowband signal is also applied to both inputs of a mixer, which functions as a times two multiplier. The resultant 42.8 MHz signal is either filtered (BPSK operation) or applied to a second times two multiplier (QPSK operation) which results in a filtered 85.6 MHz signal. Depending upon whether BPSK or QPSK operation is selected, the 42.8 MHz or the 85.6 MHz signal, with the modulation removed by the X2/X4 multiplication process, is amplified and applied to a power divider. A 42.8 MHz (BPSK opera- tion) or a 85.6 MHz (QPSK operation) signal is also developed from the 21.4 MHz reference oscillator us- ing another X2/X4 multiplier. The phase of this reference signal is compared to the phase of the doubled or quadrupled IF signal by a mixer on the phase loop (PLL) amplifier and sweep circuit card which develops a voltage depending upon the phase relationship of the two signals. The mixer output is amplified by the loop filter and applied to the control input of the 48.6 MHz VCXO to close the phase lock loop.

(7) The doubled or quadrupled IF signal is also compared to the multiplied reference signal after the reference signal has undergone a 90° phase shift. This comparison is done by a mixer which acts as a coherent detector on the quadrature detector card.

The 90° phase shift causes the output voltage from the quadrature detector to be at a steady-state maximum when the loop is locked. Thus, when lock occurs, the threshold of the comparator connected to the coherent detector is exceeded, which switches U2 on the PLL and sweep circuit card and disables the sweep circuit. When the loop is not locked, there is no dc output from the coherent detector and the sweep circuit is activated. In this case, the sweep circuit switches a current to the integrator, causing a voltage ramp to be generated. When the ramp voltage reaches the maximum level (either positive or negative) the sweep switch toggles and reverses the direction of the sweep, thus generating a triangular waveform. This waveform is applied to the VCXO for phase lock acquisition via the loop filter.

(8) I and Q channel baseband signal demodulation is performed by comparing the wideband IF signals to stable 21.4-MHz reference signals using a mixer located in the data detector and driver cards.

To maintain the proper phase relationship between the signals, an electronic phase shifter, programmed by relays under control of the demodulator relay control, alters the phase of the 21.4-MHz reference signals ac- cording to the filter selection. The resulting amplified baseband output is applied to the receive bit syn-

Table 2-10. Bandwidth Filtering Selection.

I CHANNEL SYMBOL RATE	BPSK		QPSK	
	Narrowband filter	Wideband filter	Narrowband filter	Wideband filter
16.000 to 87.999 KB/S	BW-40 kHz Fl4	BW-260 kHz FL1	BW-40kHz FL4	BW--250 kHz FL1
88.000 to 74.999 KB/S	BW-75 kHz FL5	BW-625 kHzFL6	BW-75kHzFL5	BW-626 kHz FL6
75.000 to 149.99 KB/S	BW-250 kHz FL1	BW- 625 kHz FL6	BW-250 kHz FL1	BW-626 kHz FL6
150.00 to 249.99 KB/S	BW-260 kHzFL1	BW-2.5 MHz FL3	BW-86256kHFL6	BW-2.5 MHz FL
250 00 to 629.99 KB/S	BW -625 kHz FL6	BW-2.5 MHz FL3:	BW-625 kHz FL6	BW-2.5 MHZ FL3
680.00 KB/S to2.499 MB/S	BW -2.5 MHzFL3	BW -10 MHI FL1	BW-Y2. MHz FL3	BW-10 MHz FL1
2.5000 to 9 9999 MB/S	BW-10 MHz FL2	None	BW-10=MHz FL2	None

chronizer via a relay, which permits selection of a test signal input to the bit synchronizer.

c. 70 MHz Gain Control Amplifier (fig. FO-25). The 70 MHz gain control amplifier (GCA) (A2A16) receives the 70 MHz QPSK/BPSK modulated signal, bandlimits this input signal to remove extraneous sidebands, provides both coarse and fine gain control, and downconverts the 70 MHz signal to 21.4 MHz.

This 21.4 MHz IF signal is filtered, amplified, and power divided to provide two inputs to the filter and distribution amplifier card.

(1) The 70 MHz input signal from the rear panel connector AT2J1 is routed through the internal test relay, and through P1-7 to the selected band limiting filter. The band limiting filter (FL1 or FL2) is selected by K2 based upon the I CHANNEL SYMBOL RATE and RECEIVE QPSK/BPSK switch settings. The circuits of the relay control card determine when the filter selection relay is energized (table 2-11). When deenergized, the two-pole Butterworth filter with a bandwidth of 4 MHz is the input filter. When K2 is energized, the two-pole Butterworth filter with a bandwidth of 50 MHz is selected. Following the input filter, the signal is applied to a coarse gain control which is provided by a 20 dB pad controlled by K1. If K1 is deenergized (S1 open), the 20 dB pad is bypassed and the filter output is applied directly to the input of AR1. When K1 is energized (S1 closed), a 20 dB pad is placed between the filter output and AR1 to attenuate high level signals. AR1 provides 33 dB of gain to the 70 MHz signal and its output is transformer coupled to the first of two fine gain-controlled amplifier stages. The output of the first gain controlled stage, Q1, is coupled to a fixed gain stage, Q2, through a 50 MHz bandpass filter network composed of R7, L1, and C4. The Q2 output is transformer coupled to AR3 which also provides 33 dB of gain. Transistor Q3 provides a second fine gain control stage. The AGC signal to the two AGC stages is applied through P1-26 to the limiting circuits of VR1. AR2 provides an additional 14 dB of gain to the 70-MHz signal.

Table 2-11. Input Filter Selection.

I CHANNEL SYMBOL RATE	Relay K2 status	
	BPSK	QPSK
16.000 to 49.999 KB/S	D	-
60.000 to 629 99 KB/S	D	D
680.00 KB/S to 1.2599 MB/S	E	D
1.2600 to 9 9999 MB/S	E	E
10.000 to 19.999 MB/S	-	E

(2) To perform the downconversion from 70 MHz to 21.4 MHz, the output of AR2 is applied through an impedance matching network to U1. A 48.6-MHz carrier is also applied through P2-8 to mixer U1. This downconversion is part of the phase locked loop and the 48.6 MHz signal is developed by the loop VCXO. After the downconversion, the signal is filtered by FL3 to remove the 48.6 MHz spur, and the undesired mixing products. AR4 provides 33 dB of amplification to the 21.4 MHz output of FL3. The hybrid power divider receives the output from AR4 and provides two 21.4 MHz outputs via P2--13 and P2-22 to the filters and distribution amplifier card.

d Filters and Distribution Amplifier (fig. FO-26) The filters and distribution amplifier card (A2A18) contains six filters to band limit the QPSK/BPSK modulated signals before routing to the X2/X4 multiplier and to the I and Q channel data detectors. The relay matrix associated with the filters selects, upon command from the relay control card, a filter for the data channel and a filter for the phase locked loop channel. All filters have a two-pole Butterworth response. The filter outputs are amplified to an appropriate level before leaving the card.

(1) From the outputs of the 70 MHz GCA card, two 21.4 MHz QPSK/BPSK modulated IF signals are applied to pins 12 and 28 of P1. These two input signals are routed to the correct filter input by K1, K5, K7, K9, and K13. At the filter outputs, K2, K3, K6, K8, and K14 switch the appropriate filter output to the data demodulator and phase locked loop channels. Pin 8 of K3 is the phase locked loop channel while pin 8 is the data demodulator channel. Filter selection is based on I CHANNEL SYMBOL RATE and RECEIVE QPSK/BPSK switch settings as deter- mined by the relay control card. The outputs from the relay control card activate the appropriate relays. Table 2-12 lists the condition of each relay as a function of symbol rate for BPSK operation while table 2-13 indicates the condition of' the relays as a function of the symbol rate for QPSK operation. For in-stance, when operating at 1 Mb/s in the QPSK mode, the 625 kHz bandpass filter, FL4, is in the phase locked loop and the 2 5 MHz bandpass filter, FL3, is in the data detector channel.

(2) From pin 8 of K3, the 21.4-MHz signal for the phase locked loop channel is routed through a second set of relays and bandpass filters composed of K11, K12, FL4, and FL5. These relays are also con- trolled by the relay control card in accordance with the I CHANNEL SYMBOL RATE and RECEIVE QPSK/BPSK switch positions (see tables 2-12 and 2-13). Filters FL4 and FL5 are crystal filters with bandwidths of 40 and 75 kHz, respectively. The filter output is applied to the wideband amplifier, AR4, which has a gain of 14 dB. This amplified output is then routed to the X2/X4 multiplier card via P2-6.

(3) From pin 2 of K3, the filtered 21.4 MHz IF signal for the data detector channel is routed through K4. For BPSK operation, K4 is deenergized to insert a 3 dB pad in the data detector channel. For QPSK operation, the 3 dB pad is bypassed. AR1 receives the IF signal from K4, provides a gain of 33 dB and

Table 2-12. BPSK Filter Selection.

I CHANNEL SYMBOL RATE	Filter and distribution amplifier relays													
	K1	K2	K3	K4	K5	K6	K7	KS	K9	K10	K11	K12	K13	K14
16.000 to 37.999 KB/S	D	D	E	D	D	D	D	D	D	E	D	E	E	E
38.000 to 74 999 KU/S	D	D	D	D	E	E	D	D	E	D	D	D	E	E
75.000 to 149 99 KB/S	D	D	D	D	D	D	E	E	E	D	E	D	E	E
150.00 to 249 99 KB/S	D	D	D	D	D	D	E	E	D	E	E	D	E	E
250.00 to 629.99 KB/S	D	D	E	D	E	E	E	E	E	D	E	E	E	E
680.00 KB/S to 2.4999 MB/S	E	E	E	D	D	D	E	E	D	E	E	E	E	E
2.5000 to 9.9999 MB/S	E	E	D	D	D	D	E	E	E	D	E	D	D	D

Table 2-13. QPSK Filter Selection.

I CHANNEL SYMBOL RATE	Filter and distribution amplifier relays													
	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	KI3	K14
25.000 to 37 999 KB/S	D	D	E	E	D	D	D	D	D	E	D	E	E	E
38.000 to 74 999 KB/S	D	D	D	E	E	E	D	D	E	D	D	D	E	E
76.000 to 149.99 KB/S	D	D	D	E	D	D	E	E	E	D	E	D	E	E
160.00 KB/S to 629 99 KB/S	D	D	E	E	E	E	E	E	E	D	E	E	E	E
630 00 KB/S to 2.4999 MB/S	E	E	E	E	D	D	E	E	D	E	E	E	E	E
2 6000 to 9.9999 MB/S	E	F	D	E	D	D	E	E	E	D	E	D	D	D

applies the signal to a hybrid power divider. Both outputs of the hybrid are routed through identical amplifier circuits to the data detectors. AR2 and AR3 are wideband amplifiers which provide a gain of 33 dB. The transistor stages of Q1 and Q2 are configured as common-emitter amplifiers and provide an additional gain of 10 dB. Transformer coupling is used at the output of both transistor amplifiers. The transformers are wideband trifiler wound types which have an impedance transformation of 4 to 1.

The output at P2-31 is applied to the I channel data detector and the P2-27 output is routed to the Q channel data detector.

e. Reference X2/X4 Multiplier (fig. FO-27). The reference X2/X4 multiplier (A2A22) is composed of a stable 21.4 MHz oscillator and two X2 multipliers. Each multiplier contains an amplifier, doubling mixer, and bandpass filter. Two relays are used to select either the X2 or X4 output which is amplified, power divided by a quadrature hybrid, and further amplified.

(1) The 21.4 MHz oscillator, Y1, has an output power of +10 dBm at pin 3. This output signal is power divided with one output appearing at P1-14 and the second output applied to AR1. At the output of AR1, which has a gain of 14 dB, the 21.4-MHz carrier is again power divided by R7, R3, and R14 Both outputs of the power divider are routed to the inputs of a double balance mixer, U1, for frequency doubling. The 42.8-MHz output from U1 is applied to pin 8 of relay K1 through an impedance matching pad. For BPSK operation, K1 is deenergized and the 42.8 MHz signal is routed to a 5 MHz bandpass filter, FL1, where undesired mixing products are removed.

(2) For QPSK operation, K1 is energized to route the 42.8-MHz signal from U1 to the input of AR4.

The amplifier stages composed of AR4 and Q1, plus mixer U2, form a second frequency doubling circuit. A gain of 43 dB is provided by the AR4 and Q1 combination which drives U2. The 85.6 MHz output of U2 is filtered by the 10 MHz bandpass filter FL2 and is routed to pin 3 of K2. K2 selects either the 42 8 MHz X2 output (for BPSK) or the 85.6 MHz X4 output (for QPSK) as the input for AR2.

(3) Before the selected signal is applied to the quadrature hybrid power divider, U3, it is amplified by the AR3, Q1 combination which has a gain of 43 dB. Of the outputs from U3, the output from pin 4 is phase shifted by 90 degrees with respect to the output from pin 1. From the hybrid the two signals are routed through Q3 and Q4 to P2-24 and P2-3. The circuits of Q3 and Q4 have a gain of approximately 10 dB.

(4) The 21.4-MHz output from P1-14 is applied to the phase adjust and detector driver card where it is used to derive the reference signals needed by the data detectors. The outputs from the X2/X4 multipliers are applied to the PI,L amplifier and sweep circuit card and the quadrature detector.

f X2/X4 Multiplier (fig FO-28). The X2/X4 multiplier card (A2A20) contains the squaring and quadrupling circuits required for the carrier recovery

process in the RF demodulator The envelope detector and associated amplifier, which form part of the AGC loop, are also located on this card. The output of the squaring or quadrupling circuits is amplified and applied to both the PLL amplifier and sweep circuit and the quadrature detector cards. An internal AGC loop is contained on the card to govern the level of the squared or quadrupled output signals.

(1) From the filters and distribution amplifier card, the 21.4 MHz IF signal is applied through P1-2 and the impedance matching pad composed of R14, R15, R17, R22, and R23 to AR2. The circuits of AR2, AR3, and Q1 form a three-stage amplifier that provides a gain of 58 dB. Resistors R5, R6, and R12 form a power divider which supplies the input to the envelope detector and the first doubling circuit. The circuits of CR1 and CR2 form an envelope detector that develops a positive output voltage which is proportional to the signal power level at its input. The output of the envelope detector is amplified by the circuits of AR1 (voltage gain of 6) and, via P1-29, supplies the gain control voltage to the AGC loop amplifiers on the coherent detector and AGC loop amplifier card. The second output of power divider R5, R6, and R12 is applied through a second power divider and a resistive pad composed of R47, R53, and R54 to both inputs of double balanced mixer U1. The output of U1 is switched by relay K1 to either a band- pass filter (for BPSK operation) or to a second doubling circuit (for QPSK operation). For BPSK operation, the frequency-doubled output of U1 is applied through the 5 MHz bandpass filter, FL1, to relay K2.

Relay K2 routes the filter output to amplifier AR7.

Relays K1 and K2 are energized by a low at P2-1 (for QPSK operation) and are deenergized by a high at P2-1 for BPSK operation.

(2) For QPSK operation, the output of doubler U1 is amplified by ARS and Q5 and applied to both in-puts of a second doubler, U2. Thus, the 21.4 MHz IF signal is doubled twice (quadrupled). This quadrupled output is applied to a 16 kHz bandpass filter, FL2, which removes unwanted mixing products and signals from the quadrupled signal. During QPSK operation, the output from FL2 is routed to amplifier AB7. The output of AR7 is processed by variable gain amplifier Q3 and fixed gain amplifiers AR5 and AR6.

The output signal from AR6 is split by the power divider is amplified by Q4 and is routed via P2-26 to the quadrature detector card. A second output of the power divider is amplified by Q2 and is routed via P2- 10 to the PLL amplifier and sweep circuit card. An output of Q4 is also applied to the envelope detector composed of CR3 and CR4. The detector output is amplified by AR4B which has a noninverting voltage gain of 2 and is filtered by integrator AR4A. The internal AGC loop is completed by applying the output of AR4A to the gain control adjustment which selects the output power level to be maintained by the internal AGC loop.

g. Quadrature Detector (fig. FO-29). The quadrature detector (A2A356) compares the doubled or quadrupled IF signal from the X2/X4 multiplier to the doubled or quadrupled reference source from the reference X2/X4 multiplier which is phase shifted by 90 degrees. The comparison results in a voltage proportional to the phase coherency of the two input signals. Additional circuits are contained on this card to initiate a reacquisition sequence when required.

(1) The doubled or quadrupled output from the X2/X4 multiplier card is routed through P1-14 and a 6 dB impedance matching pad to double balanced mixer U1. Similarly, the doubled or quadrupled out- put from the reference X2/X4 multiplier card is routed through P1-30 and a 4 dB pad to mixer U1. The mixer is used as a phase detector and generates an output voltage related to the phase difference between the two input signals. The U1 output signal is low-pass filtered by R4 and C1 and is amplified by AR1. AR1 has a voltage gain of 5 and provides an out- put through current limiting resistor R7 to P1-27. This output is routed to the lock detector on the coherent detector and AGC loop amplifier card.

(2) The functions connected with the initiation of the reacquisition sequence are performed by U2 and U3. When the FULL SWEEP INITIATE pushbutton switch on the front panel is depressed, a ground is applied to P1-8 causing the voltage at pin 3 of comparator U2 to go low. This causes the comparator, which has a +2.5 volt reference applied to its positive input (pin 2) to switch its output at pin 7 from the low to the high state. The high output from U2 causes the output (pin 3) of U3 to go low and provide a low out- put via P1-6 to the acquisition control card. The same effect is obtained when the input at P1-4 goes low in response to the output from the acquisition control card. A low at P1-4 results in a high at U3-8, a low at U3-6, and a low at P1-6. The low at P1-4 is caused by a rapid decrease in the received signal strength. When the phase lock loop is in lock, the in-puts at P1-8 and P1-4 are normally both high and the output at P1-6 is high, thereby inhibiting the reacquisition sequence.

h. Coherent Detector and AGC Loop Amplifier (fig. FO-30). The coherent detector and AGC loop amplifier (A2A19) contains the phase lock detection circuit and amplifiers for the control voltage to the 70 MHz GCA. Switching circuits associated with the lock detector and delay circuits associated with the lock indication are also located on this card. In addition to the AGC loop amplifier, a driver for the front panel meter and a detector for the front panel receive power indicator are also included on this card.

(1) The output from the quadrature detector card is applied through P2-23 to AR4 and AR5. R34

and C19 form a low-pass filter to eliminate stray high-frequency signals. AR4 is selected as the amplifier for BPSK operation and AR5 is used for QPSK operation. R2 provides an offset adjustment to AR4 to compensate for dc offset from the double balanced mixer on the quadrature detector card in the BPSK mode. Similarly, R18, R22, R26, R30, R35 and R38 compensate for the offsets for the QPSK mode. The appropriate potentiometer is selected by the analog gates of U2 and U3 under the control of the I CHANTNEL SYMBOL RATE thumbwheel switches. The analog gates of U7 determine whether AR4 or AR5 provides the input to summing amplifier AR9. For BPSK operation, P2-14 is high, thereby enabling one of the outputs from AR4. If lock is inhibited by a low at either P2-15 or U4-11, U4-8 is high, U6-6 is low, and the signal at U7-6 is routed to the amplifier AR9, thus providing a low gain to AR9. For BPSK operation with U4-8 being low, the output of U6-3 goes low and the signal at U7-2 is applied to AR9, thereby causing AR9 to have a high gain. When operating in the QPSK mode, P2-14 is low and U4-6 is high, thereby enabling one of the outputs of AR5 to be applied to AR9. If lock is inhibited while operating in the QPSK mode (U4-8 is high), the signal at U7-13 is applied to AR9, thereby again achieving a low gain When U4-8 is low, the AR5 output at U7-9 is routed to AR9, thus providing a high gain.

(2) The output of AR9 is inverted by AR6 and is applied to U8 and ARSA. Analog gate, U8, is used as a switch which is closed when P2-4 is low and is open when P2-4 is high. When closed, capacitor C41 is allowed to charge through CR4 to the output voltage of AR6. When the switch of U9 is open, the charge on C41 is maintained by the high impedance of AR7 and reverse-biased CR4 and CR7 Thus, C41 and CR4 form a peak detector and store the peak positive voltage at the output of AR6. AR7 is a noninverting amplifier and provides a voltage gain of 1 1 The analog gates of U9 select either the output of AR7 or the reference voltage established by R74 at the input to summing amplifier AR8B. The switching of U9 is controlled by comparator U10. If the output of AR7 exceeds the +0 78 volt reference established at pin 10 of U10, U10-7 goes high, causing U5-12 to go low. This applies the output of AR7 to ARSB. However, if the output of AR7 does not exceed +0.78 volts, the output of U10 remains low, U5-10 remains low, and the reference established by R74 is applied to AR8B.

(3) Operationally, the above circuit functions as follows. During the first sweep of the acquisition sequence, P2-15 is low causing AR9 to have a low gain. Also during this first sweep C41 is charging to the peak positive voltage of the AR6 output. If the output of AR7 exceeds 0.78 volts, U4-11 goes low. With U4-11 low, the output of AR7 is connected to the in- put of ARSB and a low is applied to U4-9 to maintain the low gain of AR9. If the output of AR7 does not exceed 0.78 volts, U4-11 remains high and the R74 reference voltage is applied to AR8B causing U4-9 to remain high and allowing AR9 to have a high gain during the second sweep. During the second sweep, the switch formed by U8 is opened and the output of AR6 is applied only to AR8A, which has a voltage gain of approximately 1.3. U10 compares the outputs of AR8A and AR8B to produce a low output if the output of AR8A is greater (more negative) or to produce a high output if the output of ARSB is greater (more negative). The low output from U10 causes P2-16 to go high, indicating that the lock threshold has been exceeded and phase lock should occur. However, if the lock threshold is not exceeded (P2-16 remains low), the acquisition sequence is repeated.

(4) The analog gates of U11 allow the peak detector capacitor C41 to quickly discharge between successive acquisition sequences. At the beginning of each acquisition sequence, P2-5 goes low, causing Ull-9 to go high. This discharges C41 through CR7, Ull-7, CR6, and the R104 and R105 combination. During the sweep cycle, Ull-9 is low, the discharge circuit is disabled, and the AR7 output is connected to C41 through R88 and CR7.

(5) The circuits associated with U12 produce a 0.3 second delay between the initial lock (represented r by P2-10 going low) and the delayed lock condition which is indicated by a low at P1-31. Before lock is achieved, C47 is charged to +5 volts through R116 and R114. When P2-10 goes low, indicating an initial lock condition, C47 begins to discharge through R114 and P2-10. During this time the U12 output is low. As C47 continues to discharge, the voltage at pin 3 of U12 becomes less than the 2 5 volt reference established at pin 2 of U12 by R120 and R122. When this occurs, the output of U12 goes high and U5-2 goes low to indicate delayed lock at P1-31. The output of U5-2 also is routed to U4-12 and U4-2. C41 is discharged by the low at U4-2 during phase lock. The low at U4-12 causes U4-8 to go low, thus placing AR9 in the high gain mode during phase lock.

(6) The noncoherent AGC output from the X2/X4 multiplier card is applied to P1-27 and AR2.

At the input to AR2, R118 provides an offset adjustment to compensate for errors introduced by the envelope detector on the X2/X4 multiplier card. The output of AR2 is a negative voltage which has a magnitude proportional to the input signal strength. A logarithmic amplifier, AR3, receives the output from AR2 and drives AR1B. To provide the proper control signal to the 70-MHz GCA, AR1B inverts the negative output from AR3 and provides a gain of 2.5. R126 provides an adjustment of the static gain of the 70-MHz GCA.

(7) AR1A and U1 provide front panel indications

of the AGC loop activity. A drive voltage for the front panel meter is developed by AR1A. R134 provides a zero adjust capability while R108 provides a full scale gain adjustment The output at P1-12 is applied to the meter when the meter switch is in the DEMOD AGC position U1 compares the AR2 output with a reference to determine if a signal of sufficient magnitude is present at the demodulator input. If the U1 input is more negative than the reference (large signal), P1-14 is low and the front panel RECEIVE POWER FAULT indicator is extinguished. When the U1 input is less negative than the reference (small signal), P1-14 is high and the front panel RECEIVE POWER FAULT indicator is illuminated. K1 selects one of two possible references for U1. For high receive symbol rates (greater than 2.5 Mb/s for BPSK or greater than 5.0 Mb/s for QPSK) the relay is deenergized and R113 determines the reference for U1 For low receive symbol rates, the relay is energized and R115 determines the reference for U1.

i. Phase Lock Loop Amplifier and Sweep Circuit (fig. FO-31) The phase lock loop (PLL) amplifier and sweep circuit card (A2A24) contains the phase detector, loop amplifier, and voltage controlled crystal os- cillator (VCXO) of the carrier recovery PLL. The initial acquisition sweep circuits, which are designed so that the desired sweep rate is obtained in one direction while the circuit retraces at a much faster rate in the other direction, are also contained on this card.

Also contained on this card is a meter drive circuit and selectable offset adjustments to compensate for static errors in the phase detector. In addition, a minisweep circuit is provided to minimize the time required for reacquisition if the phase lock is lost following an initial acquisition.

(1) The basic phase lock loop functions are performed by phase detector U3, loop amplifier AR2, and 48.6 MHz VCXO Y1 P1-26 supplies the doubled or quadrupled reference input from the reference X2/X4 multiplier through a 4 dB resistive pad composed of R29, R30, and R31 to the phase detector. The doubled or quadrupled input from the X2/X4 multiplier card is supplied to U3 through P1-13 and the 3 dB resistive pad composed of R33, R35, and R36. The U1 output is low-pass filtered by R24 and C10 and the resultant phase error signal is routed to the loop amplifier composed of AR2 and associated components. Relay K2 is associated with AR2 to obtain two bandwidths for the PLL For BPSK operation, a 176-Hz loop bandwidth is provided by energizing K2, thus placing R14 and R17 in the signal path. For QPSK operation, a narrower 30 Hz loop bandwidth is attained by deenergizing K2 and placing R12 and R15 in the signal paths. The control voltage from the loop amplifier is applied to the VCXO. P1-8 supplies the nominal 48 6-MHz output from Y1 to the 70 MHz gain control amplifier.

(2) The sweep circuit for initial loop acquisition is composed of AR3, AR5, and U2, U6, and U4. The sweep circuit is activated by a low (0 +0 5 volts) at P1-32. For this condition, U2-1 is internally connected to U2-14. This closes the loop from AR2 to AR3A, to AR5, to AR3B, and back to the input of AR2. The operation of the sweep circuit is as follows.

(a) The output of AR3A is positive (approximately +14 volts).

(b) This positive output from AR3A is limited by VR4, VR5, and attenuated so that the input to K11 is +0.1 volts.

(c) For a positive input voltage from AR3A at the input of integrator AR5, the output of AR5 is a ramp with a negative slope (U4 is in the off state).

(d) The negative-going ramp from AR5 is routed through the circuits of R57 and R61 and through the normally closed contacts of K12, to the input of AR3B.

(e) At the input of AR3B, the negative-going ramp from AR5 is summed with the positive-going ramp from the output of AR2 The summing resistance, composed of both R57 and R61 or R61 only, is determined by the state of K7.

(f) The summing resistors of AR3B are selected such that if the output of AR2 is tracking the ramp from AR5, there will be 0 volts at the output of AR3B. However, if an error exists, then the output of AR3B will be of a polarity to increase or decrease the sweep rate of AR2 to minimize the error voltage at the output of AR3B.

(g) Retrace is initiated when the ramp at the output of AR2 reaches a selected positive value as determined by the conditions of K7. For a wide sweep (+25 kHz), K7 is deenergized (P2-7 is high) and a threshold of +1.45V is selected. For a narrow sweep (+5 kHz), K7 is energized (P2-7 is low) and a threshold of +0.46V is established.

(h) When the output of AR2 exceeds the selected threshold, the output of AR3A goes negative, causing the output of U6A to go high and the output of U6B to go low

(i) U4 assumes the position as shown in figure FO-31 when the output of U6A is high.

(j) When U4 switches, the voltage at pin 7 of U4 switches from ground to -5.5 volts

(k) The negative voltages from AR3A and U4 cause AR5 to quickly integrate down, causing a fast positive-going ramp at the output of AR5.

(l) This fast retrace is again summed with the output of AR2 and the resulting error signal at the output of AR3B is connected to the input of AR2 to correct the error between the ramps from the outputs of AR2 and AR5.

(m) The fast retrace will continue until the negative-going ramp at the output of AR2 again exceeds the threshold established by AR3A (-1 45 volts

for wide sweep and -0.46 volts for narrow sweep).
When this threshold is exceeded, the output of AR3A goes high, causing U6 and U4 to switch states and the sweep cycle begins again.

(3) When phase lock is attained, P1 -32 goes high and U2 is switched to disable the sweep input to loop amplifier AR2. However, the output of AR3A remains high and AR5 continues to ramp in the negative direction. This ramp continues until U4 is switched or until AR5 reaches its output limit of approximately -14 volts. The sweep rate is controlled by the conditions of relays K8, K9, and K11. K8 is deenergized for QPSK operation and is energized for BPSK operation by the high or low state of P2-15. K11 is activated by the FAST/NORMAL sweep switch behind the front panel For FAST sweep operation, P2-25 is low and K11 is energized. When P2-25 is high, K11 is deenergized for NORMAL sweep operation. In addition, when phase lock is attained the delay lock input to P1-6 goes low and causes the output at U1-8 to go high, thereby switching relay K1. This effectively removes the shunt resistors R6 and R9 from the circuits of the loop amplifier, AR2, and results in a narrower loop bandwidth. Whenever the loop is not locked, P1-6 is high and K1 places R6 and R9 in parallel with the loop amplifier components and causes a wider loop bandwidth for acquisition.

(4) If phase lock is lost after initial acquisition, a minisweep is initiated to again reacquire the input signal. To perform the reacquisition, a sample and hold circuit, U5, is used to store the value of the VCXO control voltage present at the time when phase lock was lost. During normal operation, P2-31 is high, causing U5 to continually sample the output of AR2. When lock is lost, the P2-31 input is low and U5 stores the AR2 output voltage until reacquisition oc- curs. When lock is lost, P2-23 is switched to the low state causing K12 to be activated and P2-4 goes high causing U4 to be activated. The activation of U4 allows the integrating capacitor of AR5 to discharge to ground. With K12 switched, the normal sweep in- put from ARBA to the AR6 input is grounded. The normal integrator output via R61/R57 is also disabled when K12 is energized. When energized, K12 also enables the output of the 0.06 Hz oscillator, AR6, to be applied to the integrator input via R98, K12, and R96. The output of AR6 Is a square wave that switches between -14 volts. This input causes the integrator output to be a symmetrical triangular-wave which is attenuated by R86 and R94. This attenuated triangular-wave is summed with the output of U6 at the input of amplifier AR4. The output of AR4, a dc voltage plus a 0.06 Hz triangular-wave, is routed through K12 to the input of ARSB where it is summed with the output of AR2. As during the initial sweep, the output of ARSB is 0 volts if the output of AR2 is tracking the output of AR5 However, if an error exists between the outputs of AR2 and AR5, the output of AR3B will be of a polarity to increase or _ decrease the sweep rate of AR2 to minimize the error voltage at the output of AR3B. When the PLL has again reacquired the input signal, P1-32 goes high and the sweep is disabled. The signals at P2-4, P2-23, and P2-31 then return to their normal state.

(5) Pins 2 and 6 of U2 provide a phase lock in- dication via P1-30. P1-30 is low (0 +0.5 volts) when the PLL is locked and is high (4.5 +0.5 volts) when the PLL is not locked. Phase lock may be manually broken by placing a low on P1-32 which enables the sweep circuit to rapidly slew the VCXO Lock is manually broken by depressing the FULL SWEEP INITIATE pushbutton on the RECEIVE section of the front panel. The output of U6B, which is high during the normal sweep time and is low during the rapid retrace time, is also applied via P2-5 to the acquisition control card to function as a sweep clock.

(6) The control voltage to the 48.6-MHz VCXO is also applied to inverting amplifier AR1, which is a meter drive circuit for the front panel meter that in- dicates the VCXO position. The gain of AR1 is set to give full scale deflection, + 10 volts out of AR2, for the wide sweep (+25 kHz) mode. Resistor R5 is chosen such that for +10 volts across R5, full scale current (200 samps) will flow through R5 to the front panel meter

(7) To eliminate the problem of static phase errors generated by bandpass filters, the phase detector, and interconnecting cables, a dc offset adjustment is included at the input to loop amplifier AR2.
Relays K3 through K6 switch the appropriate offset adjustment from resistors R87 through R93 to the AR2 input. The offset adjustment resistors are connected as listed below. The relays are automatically activated based upon the setting of the RECEIVE I
CHANNEL SYMBOL RATE thumbwheel switches.

R87 for 50.000 to 75.999 KB/S QPSK.
R88 for 76.000 to 149.99 KB/S QPSK.
R89 for 150.00 to 299.99 KB/S QPSK.
R90 for 800.00 to 1259.9 KB/S QPSK.
R91 for 1,2600 to 4.9999 MB/S QPSK.
R92 for 5,0000 to 19.999 MB/S QPSK.
R98 for 16.000 KB/S to 9.9999 MB/S BPSK.

j. Acquisition Control (fig. FO-32, -32.1). The acquisition control card (A2A47) performs the logic , operations associated with the initial acquisition and ; reacquisition processes. The gain control voltage to r the 70-MHz GCA is monitored and an output is ' developed whenever the control voltage changes at an unusually fast rate as it would if the 70-MHz input signal suddenly disappeared at the demodulator in- put. The logic operations control the timing and switching states of the circuits on the coherent detector and AGC-amplifier card, the PLL amplifier and

sweep circuit card, and the quadrature detector card.

(1) Operational amplifier AR2 forms an oscillator circuit whose output pin 6 is positive for approximately 0.7 seconds and is negative for approximately 0.06 seconds. The circuits of CR4 and VR3 convert the +15 and -15 volt outputs of AR2 into a waveform that switches between +5 and 0 volts and is compatible with the TTL input of U3. The remaining input to U3-4 is high when the sweep clock from the PLL amplifier and sweep circuit card is high and is low during the sweep retrace period. The output at U3-3 is normally high except during retrace and those times when the output of AR2 is low. During the time when U3-3 is low, capacitor C3 is allowed to charge and discharge through pins 1 and 14 of U1. When U3-3 is high, the charge and discharge path of C3 through U1 is broken and the existing charge on C8 is maintained by the high input impedance of AR1. The control voltage for the 70 MHz GCA is applied to P1-24. This signal is applied to the inverting input of AR1 and to C8 through the resistive divider network of R9, R8, and R10. Capacitor C8 is charged to approximately 90% of this input voltage. When U1-9 is high, the existing voltage on CS is maintained. If U1-9 is high and the AGC voltage does not change, the output of ARI remains negative since the voltage to its inverting input is greater than the voltage to its noninverting input. If the 70-MHz input to the demodulator increases while U1-9 is high, the voltage at P1-24 will become more positive and the AR1 output will become more negative. If the demodulator input power decreases while U1-9 is high, the voltage at P1-24 will become less positive and the output of AR1 will become less negative and, if the demodulator input decreases sufficiently, may go positive. VR1 and VR2 limit the output of AR1 to +5.8 volts between R4 and R5. This limited output is then attenuated by R5 in conjunction with the parallel combination of R20 and R24. The dual comparator, U2, receives the attentuated output of AR1 and compares this output with the fixed references of +0.5 volts. If the attenuated output of AR1 falls out- side of the range extending from -0.5 to +0.5 volts, the comparator causes the voltage at P1-33 to go low. Consequently, P1-33 goes low if the power level at the input to the demodulator changes suddenly.

(2) The sweep clock output from the PLL amplifier and sweep circuit card is applied via P1-6 to U7. The inverted sweep clock at U7-2 is routed to flip-flop U5 and a second inverter. The output of the second inverter is applied to U3-4 as discussed above and is also divided by two at U5 pins 5 and 6. The second half of U5 develops the quadrature components of the sweep clock after it is divided by two. At the beginning of an acquisition sequence, the flip-flops of U5 are preset and the sweep is retraced. When the retrace beings, the output of U5-5 goes high and the output of U5-9 goes high at the beginning of the first sweep. Therefore, during the first sweep, U8-3 is high while U6-8, U8-6, and U4-8 are low. During the first sweep, these signals inhibit phase lock and enable the peak detector on the coherent detector and AGC loop amplifier card. During the second sweep these signals all switch states and the loop is allowed to lock on the strongest signal detected during the first sweep.

(3) If the signal level into the RF demodulator changes significantly during either of the sweep cycles of the acquisition sequence, the output at P1-33 goes low. This output is externally routed to P1-5 causing U7-6 to go high and U10-8 to go low.

The output of U10-8 is applied to the AGC reset control on the quadrature detector card and causes the acquisition sequence to be reinitiated. The reinitiation causes P1-21 and P1-58 to go low which causes U7-8 to go low and causes a high to appear at both U6-12 and Ull-11. The flip-flops of U5 are preset by the low at U7-8 causing US- 5 to go high. This output at U5-6, inconjunction with the high at U6-12, causes US-11 to go low, which causes U8-8 to go high. This, in turn, causes U7- 10 and P1 -7 to go low. As a result, the storage capacitor of the peak detector on the coherent detector and AGC loop amplifier card is discharged. The high at U11-11 causes Ull-8 to go low and results in a high at P1-14, thus forcing the sweep to retrace. However, the sweep clock remains high during this retrace since it is based upon the operation of AR3B (on the PLL amplifier and sweep circuit card) which is not switched.

(4) At the end of the first sweep and at the beginning of the second sweep the flip-flops of U5 change state. Therefore, P1-50, P1-8, and P1-39 all go high. This enables the demodulator to phase lock to the input signal during the second sweep. When lock is detected, P1-10 goes high and the output of U6-6 goes low. The low from U6-6 is applied to the delay circuit of the coherent detector and AGC loop amplifier card via P1-12. The delayed lock signal is routed to P1-15 and causes the output of Ull-8 and P1-13 to go high. U3-11 goes high due to the delayed lock signal and causes P1-40 to go low. If the FULL/PARTIAL sweep control switch is in the PARTIAL position, the K12 relay on the PLL amplifier and sweep circuit card is energized when P1-40 goes low. This causes the PLL to hold the VCXO output frequency if the demodulator should lose lock. When phase lock is lost, Pl-10 goes low, P1-12 goes high, and Pl-15 also goes high after a slight delay. Since U3-8 is low and U3-11 is high, P1-9 goes low when the input at P1-1i goes high after lock has been lost. This causes the sample and hold circuit on the PLL amplifier and sweep circuit card to go into the hold mode and retain the VCXO frequency at the point where phase lock had last occurred.

(5) When the FULL/PARTIAL sweep control switch is in the FULL position, P1-58 is low, U3-8 is high and U3- 11 goes low when phase lock is lost. This does not activate the frequency hold circuits. However, the low at P1-13, indicating lose of lock, causes the sweep circuit to be activated and the initial acquisition sequence is repeated. If the FULL SWEEP INITIATE pushbutton is depressed, P1-21 will go low causing U7-8 to go low, Ull-11 to go high, and P1-14 to go high. This also causes the initial acquisition sequence to repeat.

k. Phase Adjust and Detector Driver (fig FO-33). The phase adjust and detector driver card (A2A14) provides the reference inputs to the I and Q channel data detectors based upon the 21.4 MHz output of the reference X2/X4 multiplier. The 21.4 MHz input signal is phase shifted by various amounts depending on the I CHANNEL SYMBOL RATE switch setting. The phase shifts compensate for varying phase delays of the 21.4 MHz IF data signals caused by the various bandpass filters. A second phase shifter is used to adjust the Q channel reference signal for 90° of phase shift relative to the I channel reference signal. Each of the two output channels contain a two-stage amplifier circuit. The adjustment, switching, and temperature compensation circuits associated with the phase shifters are also contained on this card.

(1) The 21.4 MHz reference input (P2-6) is applied to phase shifter Z1 via a 20 dB resistive pad. The resistive power divider composed of R29, R30 and R33 splits the output of Z1 into two channels. On channel is amplified by AR5 and Q3 and becomes the 21.4 MHz reference signal for the I channel data detector. The second channel is phase shifted by Z2 and amplified by AR4 and Q2 to become the reference signal for the Q channel data detector. Since the amplifier circuits are identical, the circuit containing AR4 is described while the equivalent reference designators for the circuit containing AR5 are shown in parentheses. The hybrid amplifier AR4 (AR5) provides a gain of approximately 33 dB. Transformer T1 (T3) couples the output of AR4 (AR5) to the Q2 (Q3) amplifier which provides a +18 dBm output to the data detector via T4 (T2) and P1-15 (P1-25).

(2) The amount of phase shift introduced by each phase shifter is controlled by the voltage at the PCV inputs of Z1 and Z2. The circuits of AR2 and AR3 provide the required control voltage to Z2. AR2 is a voltage follower that provides a high impedance to phase shift control R14. The voltage divider circuit composed of R22, R23, and RT1 introduces a temperature compensated input to summing amplifier AR3. As the temperature increases, the resistance of RTI also increases, thereby increasing the current through R23 into the summing amplifier. The AR3 output, which is proportional to the control voltage from R14 and the compensation voltage across RT1, is applied through R24 to Z2.

(3) The negative reference voltage applied across R14 and the remaining phase shift controls, R1 through R13, is supplied by the circuits of AR1 and Q1, which form a voltage regulator. VR1 establishes, via Q1 and R19, a -6.4 volt reference at the noninverting input of AR1. This establishes a constant voltage at the Q1 emitter of 7.1 volts. If the Q1 emitter voltage increases, the inverting input of AR1 becomes more negative, the AR1 output becomes less negative, and the Q1 current decreases to lower the Q1 emitter voltage. Similarly, if the Q1 emitter voltage decreases, the AR1 output becomes more negative, thus raising the Q1 emitter voltage.

(4) To control the amount of phase shift introduced into the AR5 channel by Z1, the circuits of AR6 and AR7 generate a positive control voltage similar to that generated by AR2 and AR3 for Z2.

However, the input to AR6 is provided by any one of thirteen phase shift controls, R1 through R13, based upon the settings of the I CHANNEL SYMBOL RATE and RECEIVE QPSK/BPSK switches. The settings of these switches determine which of the relays, K1 through K7, are energized and thus which potentiometer controls the input to AR6. Table 2-14 indicates the relay conditions for BPSK operation and table 2-15 indicates the relay conditions for QPSK operation. For example, when operating at 1 Mb/s in the QPSK mode, the relays are controlled such that R6 through R13 is selected for each symbol rate range and operating mode. The relay control signals at P1 pins 5 through 11 are derived on the relay control card and are routed through the D/A meter card.

l. Data Detector and Driver (fig. FO-34). The data detector and driver cards (A2A12 and A2A36) demodulate the wideband IF signal by comparing the phase of the IF signal to the phase of a 21.4 MHz reference signal using a high level double-balanced mixer. The resulting bipolar baseband data is then amplified by a wideband feedback amplifier to raise the peak value of the data waveform to 1.4 volts. The data is then routed to the bit synchronizer via a test relay. Since the I and Q channel data detector and driver cards are identical, the following description pertains to both.

(1) The phase detector, U1, is a high level double- balanced mixer. With +18 dBm into the L port (U1-1), the 1-dB desensitization level occurs for +9 dBm into the R port (U1-6). Therefore, for an RMS noise power of +2 dBm into the R port and a +18- dBm reference signal into the L port, there is a margin of 7 dB before the 1-dB desensitization level is reached. The margin is required to prevent saturation on noise peaks.

(2) The modulated signal plus noise is routed

Table 2-14. BPSK Phase Shift Selection.

I CHANNEL SYMBOL RATE	Filter and distribution amplifier relays							
	K1	K2	K3	K4	K5	K6	K7	Potentiometer
16.000 to 37.999 KB/S	D	D	D	D	D	E	D	R11
38.000 to 74 999 KU/S	D	D	D	E	D	E	E	R1
75.000 to 149 99 KB/S	D	D	D	D	D	E	E	R3
150.00 to 249 99 KB/S	D	D	D	D	D	D	D	R13
250.00 to 629.99 KB/S	D	D	D	E	D	D	E	R5
630.00 KB/S to 2.4999 MB/S	D	D	D	D	E	E	D	R9
2.5000 to 9.9999 MB/S	D	D	D	D	E	E	E	R7

Table 2-15. QPSK Phase Shift Selection.

I CHANNEL SYMBOL RATE	Phase adjust and detector driver relays							
	K1	K2	K3	K4	KS	K6	K7	Potentiometer
25 000 to 37 999 KB/S	E	E	E	D	D	E	D	R12
38 000 to 74 999 KB/S	E	E	E	E	D	E	E	R2
75 000 to 149 99 KB/S	E	E	E	D	D	E	E	R4
150.00 to 629 99 KB/S	E	E	E	E	D	D	E	R6
630 00 KB/S to 2 4999 MB/S	E	E	E	D	E	E	D	R10
2.5000 to 9 9999 MB/S	E	E	E	D	E	D	E	R8

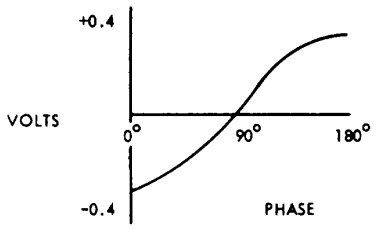
from P1-21 to the R port of the mixer through a 7 dB impedance matching pad and the 21.4-MHz reference signal is routed to the L port of the mixer through a 3 dB impedance matching pad. Derivation of baseband data is illustrated in figure 2-17. The phase detected bipolar baseband data at the L port is amplified by operational amplifiers AR1 and AR2. These amplifiers raise the level of the baseband signal to 1.4 volts peak (noise free).

(3) For signal levels of +18 dBm into the L port and -1 dBm into the R port, a voltage of +0.2 volt results at the output. Thus, the overall gain of the amplifiers is set at 7. The bandwidth of amplifiers AR1 and AR2 in this configuration is nominally 20 MHz, since the baseband signal is band-limited to 20 MHz or less. The frequency response characteristic is determined by C4 and C6.

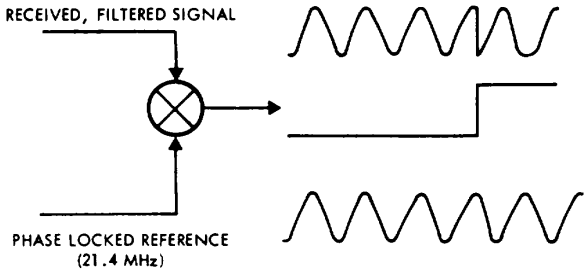
(4) Relay K1 provides a means of switching a test signal from P1-26 to the receive bit synchronizer during portions of the self-test sequence.

m. Relay Control (fig. FO-35). The relay control card (A3A32) contains the logic and relay driver functions required for the modulator, demodulator, and bit synchronizer filter switching. Inputs to the card are from the two most significant digits and the decimal point from the I CHANNEL SYMBOL RATE thumbwheel switch, from the RECEIVE QPSK/BPSK switch, and from the counter encoder card of the receive frequency synthesizer. The input from the counter encoder card at P1-16 is high for thumbwheel digits between 12500 and 25000. The rate switches provide a 9's complement output while the decimal point is unitary. The logic circuits utilize the fact that there are only two break points in each decade of the rate switch. The decimal point information is used to program the four comparators (U7, U10, U17, and U20) to detect whether the selected rate is above or below the breakpoints for the decade range selected. Relays are energized at different receive symbol rates as shown in table 2-16 for BPSK operation and as shown in table 2-17 for QPSK operation.

(1) The logic scheme involves programming four four-bit comparators, U7, U10, U17, and U20, with a break point value for each of the three rate ranges; 10 to 100 kb/s, 100 to 1000 kb/s, and 1 to 10 Mb/s. The inputs at P1-28, P1-24, and P1-20 are high for low, medium, and high ranges, respectively. The 9's complement of the two most significant digits of the selected rate are presented to the four comparators such that U7 and U17 receive the most significant digit and U10 and U20 receive the next most significant digit. Comparator U20 is cascaded with U17, and comparator U10 is cascaded with U7. The A > B out- put of U1? and U7 is high when the binary number represented by the 9's complement input (A) is greater than the threshold (B) programmed by the range inputs. The A < B output is high when the in- put (A) is less than or equal to the threshold (B). For example, when the low decade range is selected, the threshold programmed at the B inputs of U17 and U20 by the high at P1-28 and the low at P1-24 and P1-20 is equivalent to 61, which is the 9's complement of 38 (first two digits of 38000). When a rate less than 38.000 kb/s is selected, the A > B output (U17-5) is high and when a rate equal to or greater than 38.000 kb/s is selected, the A < B output (U17-7) is high. For medium symbol rates, the threshold is 15 (150 kb/s) and for the high range, 13 (1.3 Mb/s).



DATA DEMODULATOR
PHASE DETECTOR CHARACTERISTICS



WAVEFORMS AT DATA DEMODULATOR PHASE DETECTOR
EL1KP017

Figure 2-17. Data detector demodulation waveforms.

Table 2-16. Relay Driver Status for BPSK Operation.

I CHANNEL SYMBOL RATE	P1-29	P1-24	P1-20	First breakpoint			Second breakpoint			U22	U21	U19	U18	U16	U15	U12	U9	U8	U6
				Threshold	A>BU 17-5	A≤BU 17-7	Threshold	A>B U7-5	A≤B U7-7										
25 000 to 37.999 KB/S	1	0	0	38	0	1	75	0	1	off	off	on	off	off	on	on	on	on	on
38 000 to 74 999 KB/S	1	0	0	38	1	0	75	0	1	on	off	off	on	off	off	on	on	on	on
75.000 to 99 999 KB/S	1	0	0	38	1	0	75	1	0	off	off	off	on	on	off	on	on	on	on
100.00 to 149.99 KB/S	0	1	0	15	0	1	63	0	1	off	off	off	on	on	off	on	on	on	on
150.00 to 629.99 KB/S	0	1	0	15	1	0	63	0	1	on	off	on	on	on	off	on	off	off	off
630.00 to 999 99 KB/S	0	1	0	15	1	0	63	1	0	off	on	on	off	on	on	on	off	off	on
1.0000 to 1 2999 MB/S	0	0	1	13	0	1	25	0	1	off	on	on	off	on	on	on	off	off	on
1 3000 to 2 4999 MB/S	0	0	1	13	1	0	25	0	1	off	on	on	off	on	on	on	off	on	on
2.5000 to 9 9999 MB/S	0	0	1	13	1	0	25	1	0	off	on	off	on	on	off	off	off	on	off

Table 2-17. Relay Driver Status for QPSK Operation.

I CHANNEL SYMBOL RATE	P1-28	P1-24	P1-20	P1-16	P1-51	U17-5	U17-7	U7-5	U7-7	U11-6	U11-8	U11-12	U13-6	U13-8	U14-6	U14-8	Activated drivers
16 000 to 37 999 KB/S	1	0	0	X	0	1	0	1	0	1	0	1	1	1	1	1	U6, U8, U9, U12, U15, U19
38 000 to 74 999 KB/S	1	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	U6, U8, U9, U12, U18, U22
75 000 to 99 999 KB/S	1	0	0	0	0	0	1	0	1	1	1	1	1	0	1	1	U6, U8, U9, U12,
100 00 to 149 99 KB/S	0	1	0	X	0	1	0	1	0	1	1	1	1	0	1	1	U16, U18
150 00 to 249 99 KB/S	0	1	0	1	0	0	1	1	0	1	1	1	1	1	1	0	U12, U15, U16
250 00 to 629 99 KB/S	0	1	0	0	0	0	1	1	0	1	1	1	1	1	0	1	U12, U16, U18, U19, U22
630 00 to 999 99 KB/S	0	1	0	0	0	0	1	0	1	1	1	1	0	1	1	1	U6, U12, U15,
1 0000 to 1 2999 MB/S	0	0	1	X	0	1	0	1	0	1	1	1	0	1	1	1	U16, U19, U21
1 3000 to 2 4999 MB/S	0	0	1	X	0	0	1	1	0	1	1	1	0	1	1	1	U6, U8, U12, U15, U16, U19, U21
2 5000 to 9 9999 MB/S	0	0	1	0	0	0	1	0	1	1	1	0	1	1	1	1	U8, U16, U18, U21

(2) In a similar manner, the cascaded comparators, U7 and U10, establish a second threshold for each of the symbol rate ranges For the low range, the threshold is 75 (75 kb/s), for the medium range the threshold is 63 (630 kb/s), and for the high range it is 25 (2.5 Mb/s). The two pairs of cascaded comparators therefore generate two filter relay switching points per symbol rate range

(3) The logic circuits of U1, U11, U13, and U14 receive the outputs from the comparators, the three symbol rate range inputs (P1-28, P1-24, and P1-20), the RECEIVE QPSK/BPSK switch input, and the counter encoder input. Based on these inputs, the logic circuits generate the proper inputs required to activate the appropriate relay drivers. Table 2-18 shows the logic levels present for the various symbol rates of BPSK operation while table 2-19 shows the logic levels present at various points for QPSK operation.

(4) The relay drivers, U4, U5, U6, U8, U9, U12, U15, U16 and U18 through U22, are active (output pin 8 is low) only when one or more input conditions are present The first condition which will cause the drivers to be activated is for the inputs of pins 1, 2, 3,

Table 2-18 . BPSK Relay Control Signal Levels.

I CHANNEL SYMBOL RATE	P1-28	P1-24	P1-20	P1-16	P1-51	U17-5	U17-7	U7-5	U7-7	U11-6	U11-8	U11-12	U13-6	U13-8	U14-6	U14-8	Activated drivers
16 000 to 37 999 KB/S	1	0	0	X	0	1	0	1	0	1	0	1	1	1	1	1	U6, U8, U9, U12, U15, U19
38 000 to 74 999 KB/S	1	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	U6, U8, U9, U12, U18, U22
75 000 to 99 999 KB/S	1	0	0	0	0	0	1	0	1	1	1	1	1	0	1	1	U6, U8, U9, U12,
100 00 to 149 99 KB/S	0	1	0	X	0	1	0	1	0	1	1	1	1	0	1	1	U16, U18
150 00 to 249 99 KB/S	0	1	0	1	0	0	1	1	0	1	1	1	1	1	1	0	U12, U15, U16
250 00 to 629 99 KB/S	0	1	0	0	0	0	1	1	0	1	1	1	1	1	0	1	U12, U16, U18, U19, U22
630 00 to 999 99 KB/S	0	1	0	0	0	0	1	0	1	1	1	1	0	1	1	1	U6, U12, U15,
1 0000 to 1 2999 MB/S	0	0	1	X	0	1	0	1	0	1	1	1	0	1	1	1	U16, U19, U21
1 3000 to 2 4999 MB/S	0	0	1	X	0	0	1	1	0	1	1	1	0	1	1	1	U6, U8, U12, U15, U16, U19, U21
2 5000 to 9 9999 MB/S	0	0	1	0	0	0	1	0	1	1	1	0	1	1	1	1	U8, U16, U18, U21

Table 2-19 . QPSK Relay Control Signal Levels.

I CHANNEL SYMBOL RATE	P1-28	P1-24	P1-20	P1-16	P1-51	U17-5	U17-7	U7-5	U7-7	U11-6	U11-8	U11-12	U13-6	U13-8	U14-6	U14-8	Activated drivers
16 000 to 37 999 KB/S	1	0	0	X	0	1	0	1	0	1	0	1	1	1	1	1	U6, U8, U9, U12, U15, U19
38 000 to 74 999 KB/S	1	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	U6, U8, U9, U12, U18, U22
75 000 to 99 999 KB/S	1	0	0	0	0	0	1	0	1	1	1	1	1	0	1	1	U6, U8, U9, U12,
100 00 to 149 99 KB/S	0	1	0	X	0	1	0	1	0	1	1	1	1	0	1	1	U16, U18
150 00 to 249 99 KB/S	0	1	0	1	0	0	1	1	0	1	1	1	1	1	1	0	U12, U15, U16
250 00 to 629 99 KB/S	0	1	0	0	0	0	1	1	0	1	1	1	1	1	0	1	U12, U16, U18, U19, U22
630 00 to 999 99 KB/S	0	1	0	0	0	0	1	0	1	1	1	1	0	1	1	1	U6, U12, U15,
1 0000 to 1 2999 MB/S	0	0	1	X	0	1	0	1	0	1	1	1	0	1	1	1	U16, U19, U21
1 3000 to 2 4999 MB/S	0	0	1	X	0	0	1	1	0	1	1	1	0	1	1	1	U6, U8, U12, U15, U16, U19, U21
2 5000 to 9 9999 MB/S	0	0	1	0	0	0	1	0	1	1	1	0	1	1	1	1	U8, U16, U18, U21

and 4 to all be high. The second condition which will also cause the drivers to activate is a low at pin 9. If both of the above conditions are met, the driver is also active.

(5) The circuits of U4 and U5 drive relays that control the modulator filters. The conditions under which these relays are energized are described in preceding paragraphs.

2-9. Receive Bit Synchronizer

a. General. The receive bit synchronizer uses a phase locked loop to align the receive frequency synthesizer output clock with the input data. The input baseband signal is applied to an integrator which is controlled by the synchronized clock. The integrator, which is initially discharged to zero at the beginning of each bit period, integrates the input voltage over each bit period. The integrator output is converted to a digital signal (quantized) at the end of each bit period. As a result, three output bits are produced for each input bit. One bit represents the polarity of the input bit (hard decision) and the other two bits (soft decisions) represent the level, or quality, of the hard decision. The integrator acts as a matched filter which is matched to the input data rate by the synchronized clock. The soft decisions are required to obtain the maximum coding gain from the external error-correcting decoder.

(1) The input bipolar NRZ-L data from the I channel data detector and driver is applied to both the I channel data and the phase recovery integrators (fig. FO-36). The Q channel data integrator receives the bipolar NRZ-L data output from the Q channel data detector and driver circuit. Each integrator consists of two integration circuits that operate during alternate bit periods. The outputs of the alternating integration circuits are summed at the circuit output to produce a sample voltage for each bit period. The dump circuits discharge each integration circuit during the period that the other circuit is integrating.

(2) The data integrators charge through each full bit period, the resultant voltage is sampled, and the circuit is then discharged through the data dump circuits. The resultant output is a positive or negative voltage dependent upon whether a ONE or ZERO bit is received (fig. 2-18). The phase integrator is sampled and dumped at mid-bit period; therefore, if a transition has occurred and the system is synchronized, the phase integrator output is at zero volts. The difference, positive or negative, from zero volts is a measure of the extent the generated bit rate is leading or lagging the data.

(3) The data and phase integrator outputs are applied to A/D circuits (quantizers) which convert each signal to a 3-bit sign/magnitude word. The out- put of the data quantizers constitutes the bit synchronizer output. The output of the phase quantizer is used to update the clock synchronization circuit.

(4) The phase quantizer output, which is an indication of the degree of misalinement between the synchronized clock and the input data, is used in conjunction with the hard data decision to generate a digital input word to the digital loop filter.

(5) The loop filter accumulates the input words and develops a binary signal output that represents the weighted sum of the last input word and the accumulation of previous input words.

(6) The loop filter binary output is converted to a voltage level by the D/A converter. This voltage is used to maintain the correct clock phase from the receive frequency synthesizer.

b. Block Diagram Description

(1) Data and phase integration is accomplished by alternating three-amplifier integration circuits (fig. FO-37). An RC network is formed by two variable components; the resistive element is a photo- resistor device which is controlled by the automatic gain control (AGC) circuits, while the value of the capacitive section is relay-selected by control signals based upon the SYMBOL RATE selection This RC network controls the scale factor of the integration circuits to provide a constant final value output (average) regardless of the bit period. The amplifier network serves to linearize the RC integration circuit. On each integrator, the outputs of the alternating integration circuits are applied to a summing amplifier which provides a continuous output to the appropriate quantizer.

(2) The dump circuits of the I data channel are controlled by the bit dump true (IDUMPT) and bit dump complement (IDUMPC), while the dump circuits of the Q data channel are controlled by the bit dump true (QDUMPT) and bit dump complement (QDUMPC) signals from the timing logic. The I channel timing logic also develops the phase channel dump true (ODUMPT) and phase dump complement (ODUMPC) signals. In the dump circuits, a diode bridge current source/sink is formed by a constant- current source via a current mode switch. When the switch is closed, the diode bridge is forward-biased and the integrator charge is dumped to ground. The I channel bit integrator output (I INTOUT) is applied to the bit quantizer and to the AGC section of the I channel timing and automatic gain control circuits The output from the Q channel integrator is applied to the Q channel quantizer and the AGC circuits of the Q channel timing and AGC control circuits. The phase integrator output (SINTOUT) is applied only to the phase quantizer.

(3) The quantizers function identically to convert the input sample voltage to a three bit sign/ magnitude word. The A/D converter compares the in- put with reference voltages to activate the ap- propriate combination of comparators. The comparator

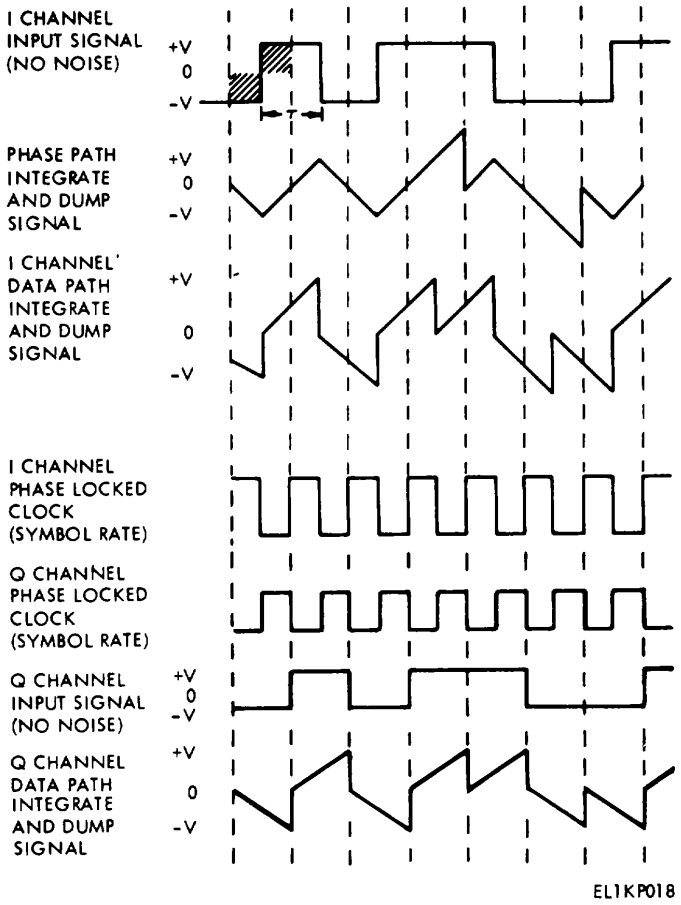


Figure 2-18. Receive bit synchronizer waveforms.

outputs are converted from unitary to binary through an encode matrix and loaded at bit rate into a three-bit storage register. The complemented outputs of the quantizers are applied to the bit synchronizer buffer where the data and phase bits are reclocked. From the buffer, the data (I and Q channel) and phase bits are gated into the decoder switch, where the one- half bit period offset between the I and 0 channel data bits is eliminated.

(4) In the phase and loss of lock detector, the phase and Q channel data bits from the decoder switch are loaded into storage registers. The two magnitude bits of data (IMSBT and ILSBT) and the two magnitude bits of phase (TMSBT and $LSBT) are then compared in magnitude by comparator U8. The data sign bit (EDECISIGNC) is exclusive OR'ed with the previous data sign bit stored in U4 to determine whether a data transition has occurred. Should a large number of consecutive comparisons of data and phase indicate that the phase magnitude is greater (on the average) when transitions occur, the loss of lock detector is activated to develop an alarm signal to the front panel. This signal is also developed when, with no data in, the AGC voltage rises to ap- proximately 12 volts.

(5) The three phase bits plus an indication of bit polarity (from U4) are applied to the code converter, the sign/magnitude code is then converted to a code that is compatible with the loop filter and, if a transition has occurred, the phase bits are gated to the loop filter. If no transition has occurred, the phase bits are meaningless and are effectively discarded (converted to zeros).

(6) In the loop filter arithmetic circuits, the phase bits are compared with phase bits previously received to increment an accumulator. The accumulator increments up or down depending upon whether the bit rate clock is leading or lagging the input baseband transitions. The accumulator contents then provide the three least significant bits to the D/A input

register. The five most significant bits are the filter lead term which is developed by the adder based upon present phase word and accumulator contents.

(7) The output of the D/A input register is converted to an analog voltage by the D/A converter which provides a speed up or slow down voltage to the frequency synthesizer.

(8) The timing and automatic gain control circuits for the I and Q channels perform two separate functions. The timing section receives bit rate clock from the bit sync buffer and develops true and com- plement 1/2-bit rate outputs. The true and complement signals alternately dump the two integrator sec- tions of each integrator card via the respective dump cards. The bit integrator is dumped at the end of bit period; the phase integrator is dumped at mid-bit period. The timing section also contains two delay lines to provide a small delay in the clock phases. This delay compensates for the propagation delay through quantizing circuits. The AGC circuits receive the out- puts of the data bit integrators. The average voltage at the end of each integration is then compared with a fixed reference, and

a. drive signal to the integrator photo-resistors is developed. Since these photo- resistors are in the integrator feedback loop, the appropriate change in their resistance will correct the integrator loop gain.

c. Integrator (fig. FO-38). The data integrators (A2A10 and A2AS4) and the phase integrator (A2A6) each consist of two identical integrating circuits that function during alternate bit periods. Since the data integrators and the phase integrators are identical, the following circuit description is applicable to all.

(1) Data from the demodulator is applied to parallel operational amplifiers AR3 and AR4. Since these are the inputs to identical integration circuits functioning during alternate bit periods, the circuit containing AR3 is described while the equivalent reference designators for the circuit containing AR4 are shown in parentheses.

(2) Data Amplifier AR3 (AR4) is an inverting, unity gain operational amplifier, the output of which is applied to the RC integrator formed by a resistor element in photo-resistor U1, fixed resistor R11 (R19), potentiometer R14 (R22), and capacitors C8, C16, and C18 (C10, C19, and C20). Photo-resistor U1 implements automatic gain control (AGC) within the integrator by adjusting the circuit resistance, and hence its gain, in response to a control voltage from the AGC circuits. Variable resistor R14 (R20) permits compensation for mismatch of resistive elements of U1. Relays K1 and K2 select appropriate capacitance for bit rate ranges as listed below. These relays receive either a ground or an open from the relay control card which is, in turn, controlled by the front panel SYMBOL RATE selection switch.

K1	*K2*	*Capacitance*	*Selected bit rate*
Energized	Energized	0.00474 of	19.200 kHz to 159.99 kHz
Deenergized	Deenergized	0.00068 4f	160.00 kHz to 1 2799 MHz
Energized	Deenergized	pf	1.2800 MHz to 9 9999 MHz (adjustable)

(3) The output of the RC integrating circuit is applied through unity gain noninverting amplifier AR6 (AR7) to the inputs of feedback amplifier AR1 (ARS) and summing amplifier AR2. Operational amplifier AR1 (ARS) is a unity gain inverting amplifier that closes the integrator loop by providing feedback to input amplifier AR3 (AR4). Summing amplifier AR2 is an inverting amplifier with a gain of two that sums the outputs of the two integrators for, application to the quantizer and to the AGC circuits.

(4) The primary difference between the three in- tegrators is in the timing of the integrator dump signals. The data integrators are dumped at end-bit period for each of the two channels and the phase integrator is dumped at mid-bit period of the I channel.
The dump signals discharge the integrating capacitors through diode switches in the dump circuits.

d. Dump Circuit (fig. FO-89). The data dump circuits (A2A9 and A2A88) and the phase dump circuit (A2A5) each consist of two Identical diode switches (with control circuits) to dump the data and phase in- tegrators. Since both data dump circuits and the phase dump circuit are Identical, the following circuit description is applicable to all.

(1) Each dump circuit card contains two identical diode switch dump circuits with associated current mode switching. The dump circuit shown at the top of figure FO-39 is described, while equivalent reference designators for the other circuit are shown in parentheses.

(2) Control to the current mode switch is an ac- coupled, 1/2-bit rate square wave from the timing circuits via P1-85 (P1-16). The constant current source formed by transistor Q1 (Q8) and associated circuits drive the emitter of Q2 (Q4). When switched by the 1/2-bit rate control signal, the collectors of Q2 (Q4) provide 6-volt peak-to-peak signals which back-bias diodes CR1 (CR4) and CR8 (CR6) during the dump interval and allow current to flow from R8 (Rl9) through the diode bridge and R12 (R80). During integrate intervals, diodes CR1 (CR4) and CR3 (CR6) conduct to provide a current source/sink for the diode bridge current and back-bias the diode bridge. The switching threshold of Q2 (Q4) is controlled by potentiometer R16 (R84).

e. Quantizer (fig. FO-40). The data quantizers (A2A8 and A2A82) and the phase quantizer (A2A4) consist of identical circuits that convert their respective integrator analog outputs to sign/magnitude 3- bit digital words. Since the data and phase quantizers are identical, the following circuit description is

applicable to all.

(1) The input analog voltage from the integrator is applied to dual A/D comparators U1, U6, U7, and U10. These comparators also receive fixed inputs from the voltage divider network formed by resistors R5, R8, R11, R15, R19, R23, R26, and R31. From the comparators, the seven-bit unitary representation of the analog input is converted to sign/magnitude binary through gates U2 and U3 (table 2-20) and the resultant 3-bit word is loaded into storage register flip-flops U4 and U8 by the applied clock at the end of each integration period. Outputs of the storage registers are routed through drivers U5, U9, and U11, which provide the complement of the coded output, to the phase and loss of lock detector.

Table 2-20. Quantizer Unitary to Binary Conversion.

Voltage In (P1 - 29)	Digital output SIGN (P1-5)	MSB (P1-6)	LSB (P1-8)
More positive than 0.9 V.	1	0	0
0.6 V to 0.9V.	0	0	1
0.8 V to O6V.	0	1	0
0.0 V to 0.8V.	0	1	1
0.O V to-0.8 V.	1	1	1
-0.8 V to -0.6 V.	1	1	0
-0.6 V to-0.9 V.	1	0	1
More negative than -0.9 V.	1	0	0

(2) The primary difference between the data and phase quantizers is in the timing of the clock pulse to the storage register. The register is clocked at the end of each bit period in the data quantizers and at mid- bit period in the phase quantizer. These clock pulses are appropriately delayed by delay lines in the timing and control circuits to allow for propagation delays in quantizing.

f. Bit Sync Buffer (fig. FO-41). The bit sync buffer (A2A29) receives the data and phase quantizer out- puts plus twice bit rate clock signals (B/S I 2R) from the decoder switch. Flip-flops U2 through U6 are used to gate the data and phase quantizer outputs to the decoder switch. The twice bit rate clock signal (P1 - 64) is divided by two (U2) and both phases of the bit rate clock are available (P1-68 and P1-33). U7 is a 50-ohm driver which provides twice bit rate clock and bit rate clock to the decoder switch. The I channel data bits are clocked by the I channel clock (P1-68 is externally jumpered to P1-28) and the Q channel and phase data bits are gated by the Q channel clock (Pl-33 is externally jumpered to P1-25 and P1-61).

g. Decoder Switch (fig. FO-42). Flip-flops U1O-U14 of the decoder switch (A3A7) receive the quantized data and phase integrator outputs from the bit sync buffer and synchronize the quantized in-
tegrator outputs to twice bit rate clock. The outputs from these flip-flops are applied to the decoder inter- face and phase and loss of lock detector cards. The twice bit rate clock from the receive synchronizer is received by U1 via P1-46. The output of 50-ohm driver U1 is applied to the bit sync buffer card where it is used to develope the bit rate clocks to the timing and AGC control circuits. Other functions of the decoder switch are described in paragraph 2-11 b.

h. Phase and Loss of Lock Detector (fig. FO-43). The phase and loss of lock detector (A3A13) receives the I channel data and phase quantizer outputs plus the AGC voltage from the I channel timing and automatic gain control circuits. The data is routed to the decoder and interface and is examined for transitions, the phase and data magnitudes are compared, and the phase word is routed to the lop filter. Should sync loss or excessive AGC voltage occur, the loss of lock detector provides an output to the front panel.

(1) The 3 bits of phase word received through inverters of U6 are loaded into storage register U7, which provides sufficient delay time (one bit period) to receive the next data sign bit and determine whether a transition has occurred. The data sign bit is applied to adder circuit U9 (output U9-6) where it is compared with the previous data MSB stored in flip- flop U4 (Q output pin U4-6). If a noncomparison occurs indicating that a transition has taken place, the adder (U9) output enables the phase word output gates (U11) in the code converter.

(2) Comparator U8 compares the magnitude of the data bits present at the outputs of U6 with the phase bits stored in U7. Should the magnitude of the phase bits exceed that of the data bits, U8 provides an input to flip-flop U4-12 (via inverter U3) to steer the flip-flop high. Clock to this section of U4 is supplied by the transition detector (U9) output. Therefore, U4 may be clocked high only if the phase magnitude for a data transition interval exceeds the data magnitude. If this condition occurs on more transitions than it does not (on the average), the threshold of voltage comparator U5 will be exceeded, and U5 will provide a low output indicating loss of lock. Variable resistor R9 permits adjustment of the switching threshold of comparator U5.

(3) The adder circuits, U9 and U10, and gate U11 provide phase word code conversion as shown in table 2-21.

(4) Voltage comparator U1 monitors the AGC voltage ctrolling the integrator time constant. If the AGC voltage exceeds +12 volts, U1 provides a low output, which sets U4-9 high and indicates a receive bit sync fault via U5.

i. Timing and Automatic Gain Control (fig. FO-44). The I and Q channel timing and automatic gain control (A2A31 and A2A30) cards consist of identical circuits that provide timing and gain control to data integrators. Control of the phase integrator is also provided by the I channel timing and AGC control. However, since the two timing and AGC circuits

Table 2-21. Phase Word Code Conversion.

	Phase word			Coded word				Effective magnitute
	U6-8	U6-l2	U6-10	P1-28	P1-25	P1-26	P1-27	
	1	1	1	1	0	0	1	-7
	1	1	0	1	0	1	1	-5
	1	0	1	1	1	0	1	4
Positive	1	0	0	1	1	1	1	-1
transition	0	0	0	0	0	0	1	+1
U4-5 = 0	0	0	1	0	0			+3
	0	1	0	0	1	0	1	+5
	0	1	1	0	1	1	1	+7
	1	1	1	0	1	1	1	+7
	1	1	0	0	1	0	1	+5
	1	0	1	0	0	1	1	+3
Positive	1	0	0	0	0	0	1	+1
transition	0	0	0	1	1	1	1	-1
U4-1	0	0	1	1	1	0	1	-3
	0	1	0	1	0	1	1	-5
	0	1	1	1	0	0	1	-7
No transition U9-6 = 0	any			0	0	0	0	0

are identical, the following circuit description is applicable to either.

(1) The timing and automatic gain control card contains two functionally separate sections. The timing section accepts the b/t rate input from the bit sync buffer and provides two phases of one-half bit rate signals to operate the integrate and dump circuits. Included in the timing section are delay lines to provide bit rate quantizer signals delayed appropriately to compensate for propagation delays through the quantizing process (Timing is shown in fig. 2-19.) The automatic gain control (AGC) section examines the magnitude of the appropriate data in- tegrator output and develops the required drive voltage for the photo-resistor devices in each integrator.

(2) Bit rate clock is received from the bit sync buffer (P1-9) and is appliee through U7 which provides TTL to ECL conversion. U8 is an ECL 50-ohm line driver used to apply the clock signal to delay lines, DL1 and DL2, and U9. The noninverting output of Us-13 clocks flip-flop U9, pin 6. This flip- flop functions as a divide by 2 circuit to develop alternating phase integrator dump signal outputs at Pl-16 and Pl-14. Similarly, the inverted clock to U9-11 develops data integrator dump signals at pins Pl-10 and P1-13.

(3) The BR output from US-13 delayed through DL2 is used to compensate for propagation delays in the phase quantizer. The delayed signals from

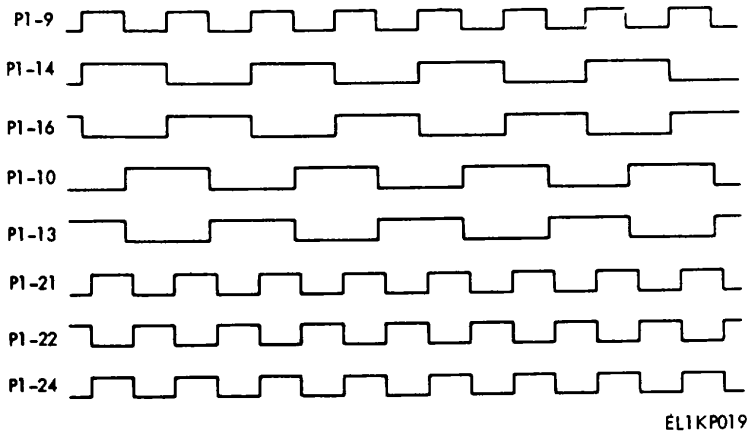


Figure 2-19. Timing and AGC control card, timing diagram.

U10-12 and U10-13 are then converted to TTL levels through U5 and U6. The ECL level output of U10 is routed via P1-21 to the phase quantizer. The delayed bit rate (opposite phase) for the data quantizer is taken from U8-12, delayed through DL1, and routed via U10 and P1-22 to the data quantizer.

(4) The AGC section of the timing and automatic gain control card receives the output of the data integrator (approximately 1.5 volts) and divides that signal by 4 across R10, R12, and the integrator output impedance. The input is then compared with a +300 millivolt reference developed across R1, R2, and R4 and a -300 millivolt reference developed across R17, R18, and R19. Outputs of comparators U1 are OR'ed and applied to the data input of flip-flop U3. Amplifier U4 and transistor Q1 convert the flip-flop output from ECL to TTL levels for application to summing amplifier AR1. Amplifier AR1 and transistor Q2 provide drive to the photo-resistors in both the data and phase integrators. As this AGC voltage increases, the resistance of the photo-resistors decreases and the integrator gain increases.

j. Loop Filter. The loop filter (A3A14) is identical to the transmit bit synchronizer loop filter (para 2-4 c).

k. D/A Converter. The D/A converter (A3A15) is identical to the transmit bit synchronizer D/A converter (para 2-4 d).

2-10. Receive Frequency Synthesizer

The operation of the receive frequency synthesizer, which is controlled by the I CHANNEL SYMBOL RATE switches, is identical to the transmit frequency synthesizer (para 2-5). A functional block diagram for the receive frequency synthesizer is shown in figure 2-20.

2-11. Decoder and Interface

a. General The decoder and interface circuits (fig.FO-45) perform four basic functions: select BPSK or QPSK data, interface with an external error correcting decoder, provide differential decoding, and derandomize the data stream. When the external error decoder is selected, the sign bit, MSB, and LSB of both I and Q channels plus bit rate clock are supplied to the decoder. Decoded data and clock are then returned from the decoder and are gated to the derandomizer circuits via the differential decoder. When the differential decoder switch is OFF, the data is simply clocked through the registers with no differential decoding. However, when the decoder switch is in the QPSK modes without external decoding, the differential decoder is always enabled The external error decoder can be bypassed in the BPSK mode with or without differential decoding. Outputs from the decoder switch are also routed to the phase and loss of lock detector and the D/A meter circuits. Decoded data and clock signals are applied to the derandomizer circuits. When the derandomizer logic is selected (RANDOMIZER RECEIVE switch is in ON position), the data is clocked through the derandomizer logic to reconstruct the original data traffic pattern. If the derandomizer logic is not selected, then the data is clocked through the derandomizer unaltered. When bit errors are present in the randomizer input data, the number of output errors are multiplied by the derandomizer feedback shift register. The feedback taps on the derandomizer and randomizer shift registers have been selected to provide a minimum error multiplication in the QPSK differential mode only. Data output of the derandomizer is reclocked to the output line drivers.

b. Decoder Switch (fig. FO-42). The decoder switch contains the input gating functions to receive the I, Q, and phase quantizer output from the bit synchronizer buffer. Also contained in the decoder switch is the switching logic required to select BPSK, QPSK, external error decoding, and differential decoding plus the necessary timing and clock circuits.

(1) From the bit sync buffer, the three outputs (sign bit, MSB, and LSB) from the I channel, Q channel, and phase quantizer, plus bit rate clock are loaded into D flip-flops U10 through U14 by the twice bit rate clock (P1-25). At the outputs of these flip- flops, the I channel bits are still offset from the phase and Q channel bits by one-half bit period. The outputs are applied directly to the appropriate inputs of the decoder interface, meter D/A, and phase and loss of lock detector cards. However, the gated bit rate clock (U10-5), the gated bit rate clock complement (U10-6), the I channel sign bit (U10-9), the Q channel sign bit (Ull-5), and twice bit rate clock (U5-2) signals are applied to the data and clock gating circuits (U7 and U3).

(2) When the external error decoder is enabled (P1 - 60 is grounded), the data and clock gates (U7 and U3) are disabled because U2 pins 8 and 11 are low. The gating signal to the decoder interface (P1-24) is high and the data complement and clock outputs of the decoder are received by the OR gates of U8 via P1-15 and P1-57. From the OR gate outputs (U8-6 and U8-8), the data and inverted clock signals are applied to the differential decoder inputs, U9-2 and U9-3. The differential decoder may be enabled (high at P1-49) or disabled (low at P1-49) through U2-6 since U2-5 is always high when the external error decoder is enabled.

(3) When the external error decoder is disabled (P1-60 is high), the data and clock signals must pass through U7 and U3. P1-14 is low whenever the BPSK mode has been selected and thus disables U7, U8-8 and U3-11. However, U2-8 is high and gates U3-3 and U3-6 are enabled. The I channel hard decision bit (EDECISIGN) from U10-9 is then routed

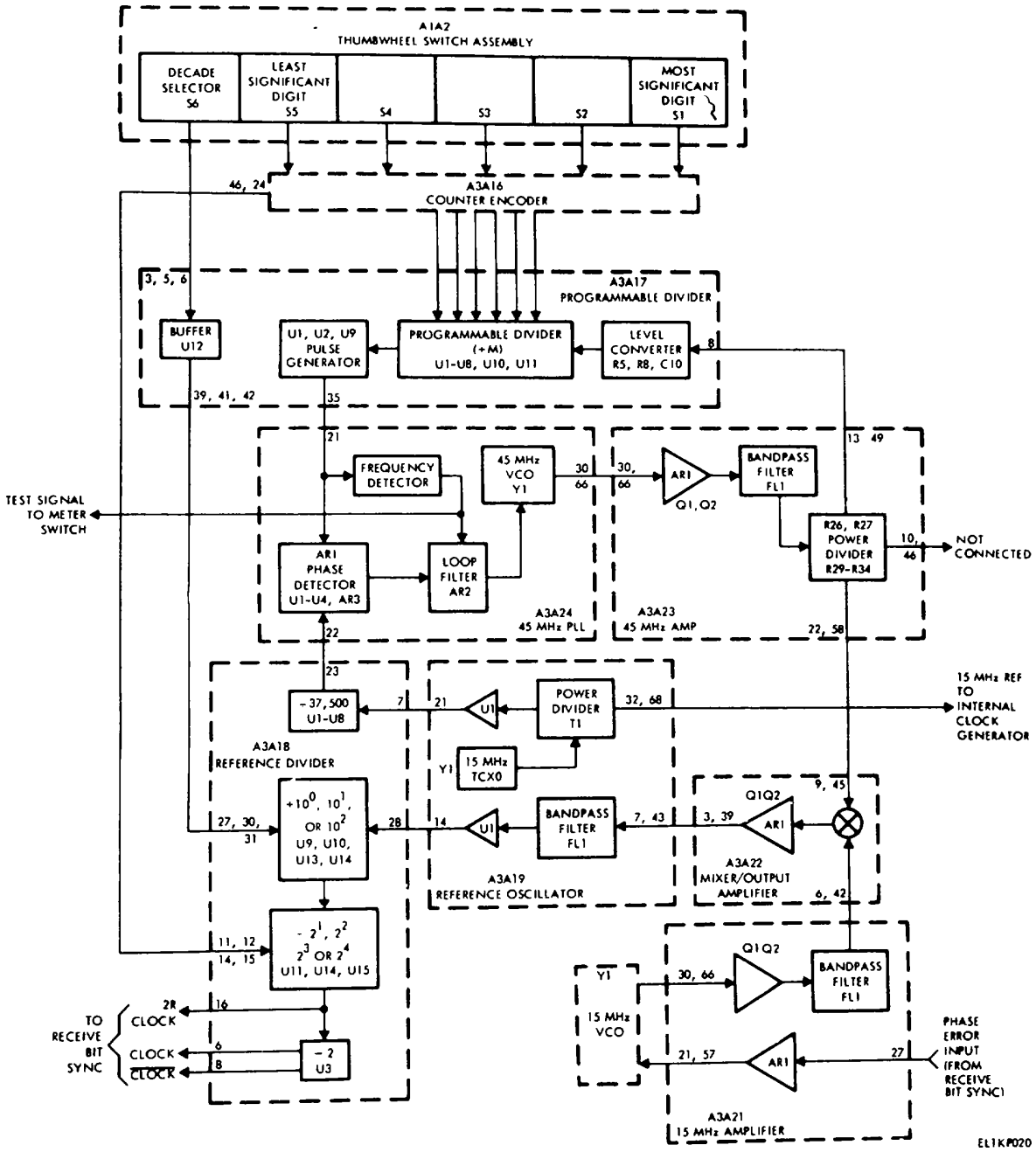


Figure 2-20. Receive frequency synthesizer, functional block diagram.

through U3-3 and U8-6 to the differential decoder input (U9-2). The inverted clock accompanying the I channel data from U10-6 is routed through U3-6 and U8-8 to the differential decoder input (U9-3).

(4) If the QPSK mode is selected (Pl-14 is high) and the external error decoder is disabled (P1-60 is high), U2-11 is high and U2-8 is low, thereby disabling U3-3 and U3-6. The I channel hard decision

data bit is applied to U7-4 and the Q channel hard decision data bit is applied to U7-10. U7 performs an AND function between these hard decision data bits and opposite phases of the clock signals from U10 pins 5 and 6 (refer to timing diagram, fig. 2-21). The two offset data channels from U9 pins 6 and 8 are then multiplexed into a single data stream at U8-6 and this single stream, at twice bit rate, is applied to the differential decoder. The clock from U5-1 (equal to the bit rate of the combined data stream) is gated through U3-11 and U8-8 to the input of the differential decoder.

(5) The differential decoder, which is composed of U3, U4, U9, and U6, operates in different ways depending upon the settings of the receive switches on the front panel. The possible combinations of the switch settings result in three different configurations for the differential decoder as indicated by table 2-22. When the differential decoder is operating in configuration 1, the decoder is disabled and the data bits are clocked through from U9-2 to U6-12. Differential decoding, based a comparison of the present bit (U9-5) and the second previous bit (U6-6), is performed if the decoder is in configuration 2. Configuration 3 results in differential decoding based upon a comparison of the present bit (U9-5) and the previous bit (U9-9). Configuration 2 is used whenever the modem is operating in the QPSK mode without external error decoding, regardless of the position of the differential decoder switch. The remaining differential decoder

Table 2-22. Differential Decoder Configurations.

Configuration	Error Modulation decoding	Deferential correcting switch	decode	U2-e	U6-1
1	BPSK	NONE	OFF	Low	Low
3	BPSK	NONE	DIFF	High	Low
1	BPSK	EXT	OFF	Low	Low
3	BPSK	EXT	DIFF	High	Low
2	QPSK	NONE	OFF	Low	High
2	QPSK	NONE	DIFF	Low	High
1	QPSK	EXT	OFF	Low	Low
3	, QPSK	EXT	DIFF	High	Low

requirements are satisfied by configuration 3 and are selected by the front panel switch.

(6) The differential decoder output (U4-6) is clocked through U6 and routed to the randomizer/derandomizer through P1-32. Both phases of the bit rate clock are applied to the output circuits through P1-58 and P1-59. A clock output is also provided to the randomizer/derandomizer through P1-58. A twice bit rate clock signal from the receive reference divider is applied through P1-46 to P1-9. is a 50-ohm driver with its output (pin 8) routed through P1-47 to the bit sync buffer.

c. Decoder Interface (fig. FO-18). The decoder interface card (A3A28) provides the necessary interface between the QPSK/BPSK modem and the external error correcting decoder. Circuits U1 through U5 are identical dual line drivers that convert logic inputs to differentials outputs. Line drivers U1, U3, and U4 accept TTL quantified data outputs from the decoder switch and provide differential outputs to the

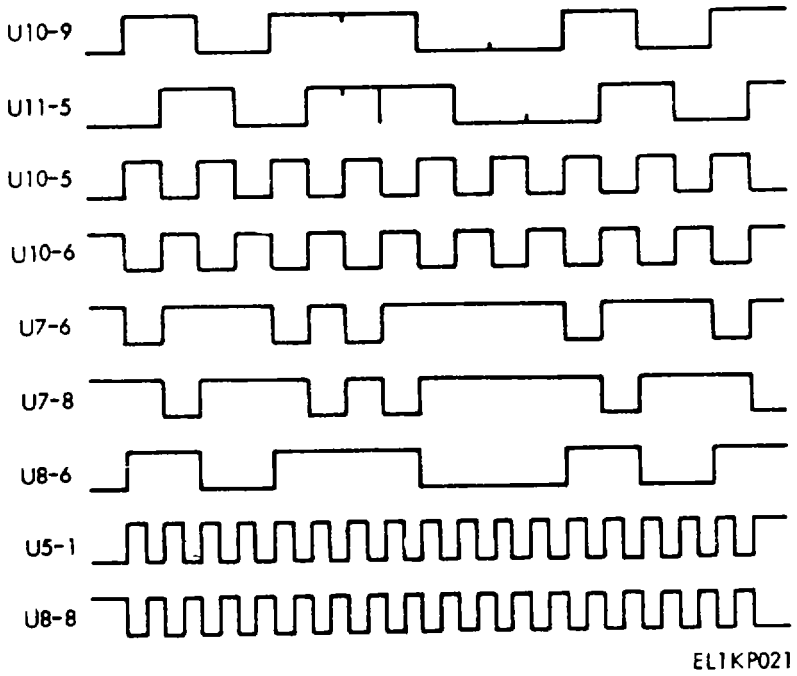


Figure 2-21. Timing diagram for QPSK gates and multiplexer.

decoder. Similarly, U5 translates the TTL clock outputs from the decoder switch into differential inputs for the decoder. The clock outputs can be inverted by switches S5 and S6. In all cases, a logic ONE is the off state of the drivers and a logic ZERO is the on state (fig. 2-12). A logic ONE is zero volts while a logic ZERO is between -70 and -135 millivolts. The drivers have a current sink of between 3.5 and 7 milliamperes, Line receivers U6 and U7 receive differential input signals, similar to those generated by line drivers U1 through U5, and produce TTL logic compatible outputs. The outputs switch when a differential input voltage of 25 millivolts is received. Line receivers U6 and U7 are enabled by a high on pin 6. Only U7 is used and U7-6 receives an enable signal from the decoder switch card via P1-62 when the error correcting decoder has been selected by the front panel switch. When a low is applied to pin 6, the receiver output is held high. U7 accepts the recovered data and accompanying clock from the decoder, converts the signals to TTL levels, and routes these signals to the decoder switch. S2 allows the received clock to be inverted.

d. Randomizer/Derandomizer (fig. FO-16). The derandomizer logic (A3A33), consisting of U4 through U13, is enabled when the input P1-44 is low. A logic ONE at P1-44 disables the derandomizer and allows the data input at P1 30 to be routed unaltered to output P1-29. The data output, however, is delayed by one bit time. When the randomizer logic is enabled, input data is routed directly to the shift register (U10 and Ull) and the modulo-2 sum of the ninth and eleventh stages of the shift register are added modulo-2 to the input data to produce the derandomized output. Binary counters U12 and U13 perform the same function in the derandomizer as binary counters U7 and U8 in the randomizer logic. Refer to paragraph 2-6 b for a description of this function.

2-12. Output Circuits

a. General. The output circuits generate the necessary output signal characteristics to provide the demodulated data and reconstructed clock to the digital user. A block diagram of the output circuits is shown in figure 2-22.

(1) The demodulated data and reconstructed clock are provided directly to the digital user via two identical line driver circuits on the standard line driver card. The standard data and clock outputs of this card provide 6-volt, peak-to-peak balanced signals into a balanced 75-ohm load The card also contains a dual line receiver to monitor the data and clock outputs and provides signals compatible with the internal test circuits. The alternate line driver provides an identical set of outputs for use by a second digital user, if required.

(2) The data output from the randomizer/derandomizer and the clock output of the decoder switch are also applied to an LOS/cable driver, which supplies bipolar NRZ output signals compatible with an interconnect facility LOS micro-wave link or an interconnect facility cable.

b. Line Drivers (fig. FO-46). The two line driver cards standard A3A31 and alternate A3A30) each contain two identical sections to convert logic level inputs to balanced outputs to interface with external equipment.

(1) The logic level inputs to the line drivers are applied through hex inverters of U1 to switching transistors that drive the differential amplifiers. Since the two driver circuits are identical, only the circuit associated with the P116 input is discussed. Transistor Q2 is biased such that when U1-4 is low, Q2 is on, the current through R4 provides base drive to Q1, which is a saturating switch. Since Q3 receives its base drive from Q1 collector, Q3 will be off. The current through R7, in this case will flow through R12 via CR6, causing Q5 to supply no base drive current to Q7. Since Q7 is off, Q6 will be on because of the base current received through R6, R8, and R14. The resulting output, with S1 in position 1, is P1-22 high, and P1-21 low. When U1-4 goes high, transistor Q4 and diode CR5 will back-bias diode CR6 and cause CR3 to conduct, reversing the states of all the remaining transistors and therefore the outputs.

(2) The amplifier outputs are routed through switches that permit polarity inversion to the output connectors. Each amplifier output is also connected to one section of line receiver U2. The line receivers reconvert the signals to logic level outputs for test purposes.

c. LOS/Cable Driver (fig. FO-47). The LOS/cable driver (A3A4) receives NRZ-L data from the randomizer/derandomizer and clock from the decoder switch. The LOS/cable driver develops bipolar NRZ outputs at +23, +10, or 0 dBm to drive cable loads of 50 ohms and 75 ohms unbalanced and 75 ohms balanced. A 75 ohm unbalanced output is also provided at power levels of -2, -12, or -22 dBm to drive an LOS microwave link. A link test output is also routed to the LOS/cable receiver and decoder.

(1) The input logic, U1 through U4, converts the NRZ-L date such that the output amplifiers develop bipolar NRZ data (fig. 2-23). The bipolar NRZ format is one in which ONE bits are represented by alternate positive and negative levels while ZERO bits are represented by ground levels. When the data input is high (logic ONE), the outputs from inverters of U1 steer flip-flops of U2 such that the input ONE is shifted into U2 (Q output pin 5) and U2 (Q output pin 9) is allowed to toggle to the opposite state Outputs of U3 then steer flip-flops of U4 to provide the appropriate positive or negative control inputs to the

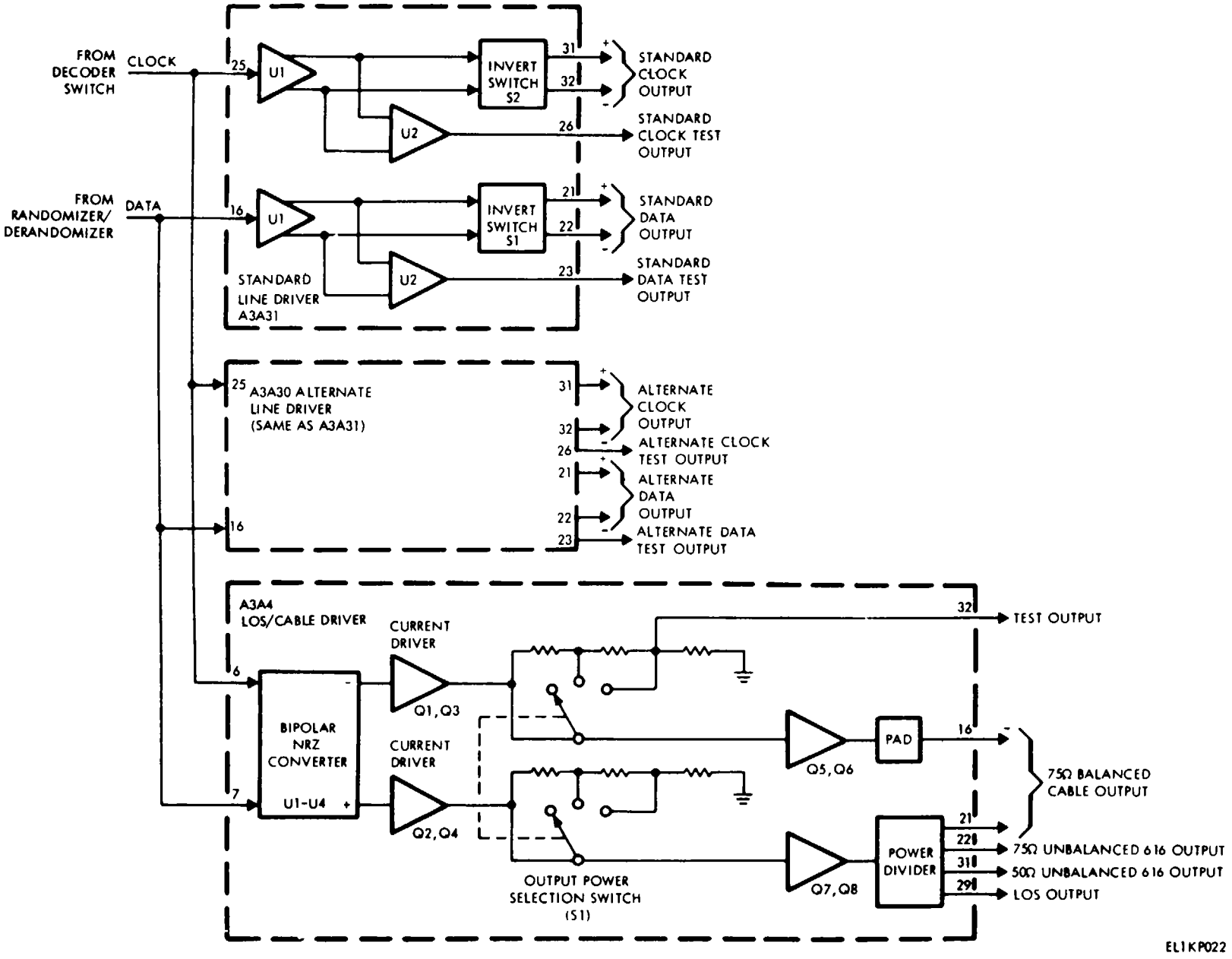


Figure 2-22. Output circuits, functional block diagram.

amplifiers. When the data input is low (logic ZERO), flip-flop U2 (Q output pin 5) is steered to a zero and both AND gates of U3 are inhibited. The resultant high outputs from AND gates of U3 steer the Q output pin 7 of flip-flop U4 high and the Q output pin 6 of flip-flop U4 low. Thus, an input logic ONE causes the states of U4-7 and U4-6 to be identical highs or lows depending on the state of U2, while an input ZERO forces U4-7 high and U4-6 low.

(2) Transistors Q1 and Q2, Q3 and Q4 form a complementary pair of differential current mode switches with OR'ed collectors which assume the states indicated in table 2-23. The output from the junction of Q2 and Q4 is either a positive or negative current, or ground when both transistors are off and the source current equals the sink current. The output from the junction of Q1 and Q8 is either a positive or negative current with the opposite polarity from the other current output (Q2 and Q4), or ground with both transistors are on. The voltage levels at the out1 RS -2G-282 puts of the current mode switches (which are equal and opposite), and thus the power outputs of the circuit are controlled by using switch S1 to change the load resistances. The link test output is taken directly from the attenuator outputs while the ICF data is applied to amplifier/line drivers Q5, Q6 and Q7, QS. The outputs of the line drivers then drive the ICF ' cable or LOS microwave link through the appropriate impedance matching resistors.

Table 2-23. Balanced Amplifier Drive.

U4-7	U4-e	Q1	Q2	Q3	Q4
Low	High	On	Off	On	Off
Low	Low	On	Off	Off	On
High	High	Off	On	On	Off

2-13. Internal Clock Generator

a. General The internal clock generator is shown in figure 2-24. The operation of the internal clock

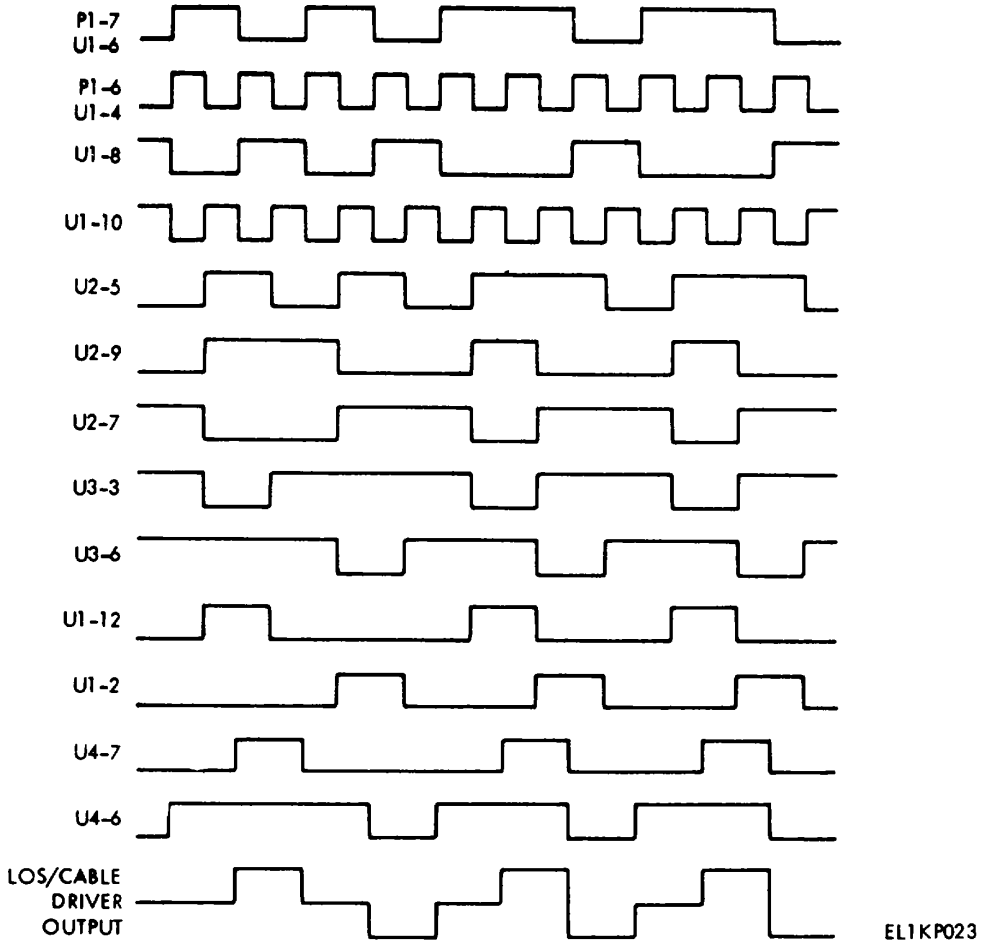


Figure 2-23. LOS/cable driver, timing diagram.

generator is similar to the equivalent sections of the transmit frequency synthesizer, discussed in paragraph 2-5. The stable clock card receives the programmable reference frequency and a stable 15-MHz reference signal from the transmit frequency synthesizer and provides a logic-compatible output of the difference frequency. This function is equivalent to the function of the mixer/output amplifier card along with the filter and level converter located on the reference oscillator card of the transmit synthesizer. The same reference divider is used, and the reference divider control inputs are connected in parallel with the control lines for the reference divider in the transmit frequency divider. The result, since a stable 15-MHz reference signal is used instead of the 15-MHz VCO output, is a clock signal at the selected INPUT DATA RATE. A line driver provides the clock signal to the digital user as a balanced output.

b. Stable Clock Circuit (fig. FO-48). The Internal clock output is the selected bit rate, unaffected by variations in the control voltage to the VCO. To implement this function, the output of the 15 MHz reference oscillator is mixed with the amplified output of the 45 ±10 MHz phase lock loop oscillator. The resultant 20to 40-MHz clock is amplified, filtered, and the down counted by decade and binary counters on an additional reference divider card.

(1) The 15-MHz input from the reference oscillator is received at the stable clock card (A8A89) via Pl-28 and applied across the attenuator formed by resistors R7, R11, and R12 to the input of mixer U1 The 45 -10 MHz Input from the 45-MHz amplifier is received via P1-11 and applied across the attenuator formed by R28 through R25 to the second Input of the mixer, The difference frequency, 20 to 40 MHs, is transformer-coupled to the Input of the three-tage RF amplifier formed by operational amplifier AR1 and transistors Q1 and Q2. This amplifier Is identical to the circuit used on the circuit used on the 45-MHz amplifier card and has a gain of approximately 40 to 56 dB as controlled by variable resistor R87.

(2) The output of transformer T2 is attenuated by R89, R41, and R42, and applied to low-pass filter FL1. The filter suppresses undesired mixer products and provides an output through attenuator R40, R48, and R44 to ECL to TTL converter U2. The resultant stable output between 20 and 40 MHz is a multiple of the selected bit rate and is appropriately counted down to the selected frequency through binary and decade counters of the reference divider.

c. The operation of the reference divider is discussed in paragraph 2-5d and the operation of the line driver is discussed in paragraph 2-12b.

2-14. Test and Monitor Functions

a. General The QPSK/BPSK modem contains a group of circuits which, in conjunction with various front panel indicators, provide a means of monitoring the operational status of the unit. The status monitoring capabilities along with the built-in test circuits provide a means of rapidly verifying operation or diagnosing a malfunction.

b. Fault and Statue Monitor Functions. The signal flow of the fault and status monitor functions is shown in figure FO-49.

(1) The front panel fault indications are developed from the following signals:

(a) The transmit bit detector a logic 0 output when in the transmit bit synchronizer, a loop filter overflow or underflow occurs (para 2-4b and para 2-4c).

(b) The 70-MHz output amplifier develops a logic 0 output when the modulator output signal drops below the required level (para 2-7 e).

(c) The coherent detector and sweep generator develops a logic 1 output when the phase lock loop In the rf demodulator is not locked (para 2-8h).

(d) The detector and AGC amplifier provides a logic 0 output when the AGC voltage indicates a loss of input signal to the rf demodulator (para 2-8h).

(e) The phase and loss of lock detector in the receive bit synchronizer provides a logic 0 output when the magnitude of the phase decisions (on the average) exceeds the magnitude of the data decisions (which indicates loss of lock) or when the AGC voltage indicates loss of bit synchronizer input signal (para 2-9h).

(f) The thermostat, which is positioned to monitor the temperature of the outlet air, provides a ground when ever the outlet air temperature exceeds 180*F.

(2) The presence of any fault indication except overtemperature causes the same result. Each fault indication sets a latch circuit on the alarm circuits card. Each latch output is applied to one of two OR gates. One OR gate is activated by either transmitter section fault signal and the other by any of the receiver section fault signals. Each OR gate output illuminates a front panel indicator showing which section developed the fault signal. Additionally, the presence of a fault Indication at either OR gate output causes the blinker generator and relay K1 (via driver U1) to be energized. Relay K1 provides one contact closure for remote fault status monitoring purposes, and a second contact closure which activates the audible alarm if enabled by the front panel ALARM Switch. The blinker generator output is gated with the latch outputs and the fault indicator signals to cause the appropriate front panel indicators to flash as long as the faults are present. If any of the faults are cleared after the appropriate latch circuits have been

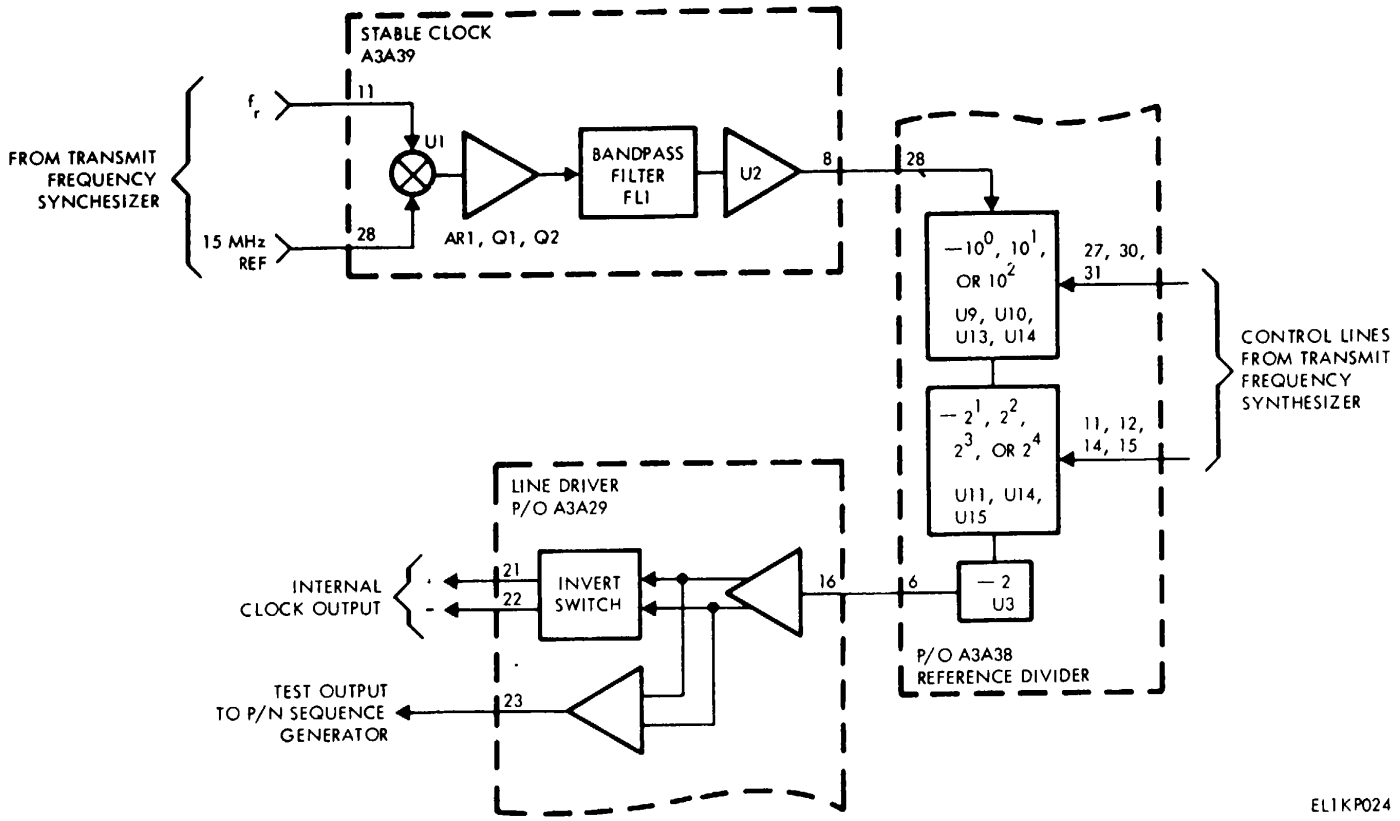


Figure 2-24. Internal clock generator, functional block diagram.

set, the gating networks provide steady ON indications at the front panel.

(3) The thermostat is connected directly to the associated indicator as well as the reset line and the audible alarm via a diode. In the event of a temperature fault, all fault indicators illuminate and the alarm sounds. In this case, none of the indications can be reset or disabled.

(4) All fault latches can be reset by momentarily holding the ALARM switch in RESET position. The RESET position also illuminates all fault indicators for lamp test purposes.

(5) The 70-MHz crystal oscillator card in the modulator provides a logic 0 output as long as the 70-MHz crystal oscillator is providing output power and the data input to the modulator is switching from state to state. A driver on the alarm circuits card illuminates the MODULATOR TEST indicator located on the front panel whenever a logic 0 is present.

(6) Driver circuits on the digital to analog meter card are connected to monitor the data and clock inputs to the error comparator The DATA and CLOCK indicators are located in the MONITOR section of the front panel Each 1 indicator is illuminated when its input is a logic 1 and extinguished when its input is a logic 0.

(7) The front panel meter is controlled by the MONITOR rotary switch.

(a) With the rotary switch in the OFF position, the meter is shorted.

(b) In the DC PWR position, the ±5V, -5V, + 15V and -15 V power supply outputs are applied to the meter through a resistive combiner network on the bit sync buffer card. The resistance associated with each voltage provides a total meter input current of 100 uA, which results in a one-half scale deflection when nominal voltages are present.

(c) The 45-MHz phase lock loop cards in the transmit and receive frequency synthesizers each contain circuits which provide a nominal 100 uA output current into the meter when the loop is locked. When the loop is out of lock, the deviation from 100 u A is proportional to the difference between the programmable divider output frequency and the 400 Hz reference frequency (para 2-5 e) These outputs are displayed on the meter when the MONITOR rotary switch is in the XMIT SYNTH and RCVR SYNTH positions.

(d) The AGC amplifier card in the RF demodulator provides a conditioned output which is displayed by the meter when the rotary switch is in the DEMOD AGC position (para 2-8 h(7)). The meter deflection is proportional to the input power (in dBm) with the 0 and full scale deflections representing the minimum and maximum allowable levels, respectively.

(e) In the DEMOD VCXO position, the control voltage to the VCXO on the phase locked loop amplifier and sweep circuit card of the RF demodulator is applied to the meter through an isolation amplifier. The amplifier gain is chosen so that full scale meter deflection is obtained for the wide sweep mode

(f) In the ERROR COUNT and SIG/NOISE positions of the rotary switch, the meter displays the output of the D/A converter on the digital to analog meter card. This indication is representative of the bit error rate and the signal-to-noise ratio.

(g) The bit sync buffer card in the receive bit synchronizer develops two conditioned outputs which are displayed by the meter when the rotary switch is in the BIT SYNC AGC I and Q positions. The meter deflection is proportioned to the AGC voltages in the I channel integrate and dump or the Q channel integrate and dump circuits of the receive bit synchronizer

(h) When the rotary switch is in the XMIT RATE and RCV RATE positions, biasing circuits on the test interface card provide an output to the meter which is proportional to the control voltage of the 15 MHz VCO in the transmit and receive frequency synthesizers. The frequency and control voltage of these VCO's is directly related to the transmit and receive clock rates.

(8) The error comparator receives data and clock inputs from various sections of the QPSK/BPSK modem as selected by the MODE, MONITOR rotary, and ERROR COUNT switches. The input clock drives a pseudo-random sequence generator identical to the one used to stimulate the test circuits The input sequence is compared to the internally generated sequence and an output pulse is developed each time the sequences differ. The internal pseudo-random sequence generator may be synchronized to the input sequence by momentarily placing the MONITOR AUTO/MANUAL switch in the MANUAL position. When the MONITOR switch is in the AUTO position, the synchronization circuit is controlled by two counters. The bit counter monitors the input clock and divides the rate by 256. The error counter is preset to a count of 64 at the beginning of each bit counter cycle, and downcounts each time an error is detected. If the error counter downcounts to 0 before the bit counter resets it to 64 on the next cycle, an output pulse is produced which resynchronizes the pseudo-random sequence generator.

(9) The digital to analog meter card produces an output current to the front panel meter based on the average input pulse rate A clock-loss detector circuit disables the input if a 1c3s of clock should occur. An additional circuit monitors the bit and error counters to limit the number of error pulses gated to the D/A converter, and thus limits the meter drive current at high error rates Input gating circuits are also present

to select the input for the D/A converter depending upon the position of the transmit and receive switches. The external error output signal is selected by U7 and US. Driver circuits for the DATA and CLOCK indicators are also contained on the D/A converter card.

c. Test Function The test function provides a means of providing an internally generated pseudorandom data sequence to the QPSK/BPSK modem transmitter input. The QPSK/BPSK modem receiver may then, with the test relay energized, be used to reconstruct the input sequence. The data signals at various points in the modem are monitored as selected by front panel switch settings to determine whether the proper sequence is present. A functional block diagram of the test circuits is shown in figure FO-50.

(1) The clock for the test function is taken from the internal stable clock generator through the divide by 2 and switching circuits of the encoder switch card. The internally generated stable clock is also provided to the digital user from the output of the line driver. During normal operation, the MODE switch is in the OPERATE position and the pseudo-random sequence generator is disabled.

(2) When the MODE switch is in the LINK position, the pseudo-random sequence generator, which generates two 2047 bit sequences (one I channel and one Q channel sequence) at the selected INPUT DATA RATE, is enabled. The digital user inputs to the input circuits are also disabled by the MODE switch and the internally generated sequence is applied to the transmit bit synchronizer through the input circuits when the TRANSMIT QPSK/BPSK switch is in the BPSK position. If the switch is in the QPSK position, both the I and Q channel outputs of the PN sequence generator are applied through the encoder switch in some of the LINK modes. As a result, the transmitter output is BPSK or QPSK modulated with internally generated sequences for link testing purposes.

(3) When the MODE switch is in the TEST position, the internal pseudo-random sequence generator is enabled and the appropriate sequence gates are enabled. Setting the MODE switch to the TEST position also accomplishes the following functions.

(a) The error comparator input is controlled by the ERROR COUNT switch.

(b) The test relay at the input to the RF demodulator is energized to apply a test output from the modulator instead of the IF input from the terminal to the demodulator input circuits.

(c) The relay on the LOS/cable receiver and decoder card is energized to disable the LOS/cable inputs and apply a test output from the LOS/cable driver to the bipolar NRZ decoder circuits (para 2-3).

(d) The level converters on the input interface and test interface cards are enabled.

(4) The data and clock inputs to the error comparator are selected according to the settings of the SOURCE, QPSK/BPSK, MONITOR rotary, and ERROR COUNT switches which control the switching functions of the PN sequence generator, test interface, and D/A meter cards. In the BPSK mode when the MONITOR rotary switch is in the SIG/NOISE position, the most significant soft data bit of the I channel and corresponding clock are selected for application to the error comparator. In the QPSK mode when the METER switch is in the SIG/NOISE position, both the I and Q channel most significant soft data bits are applied to the error comparator. When the MODE switch is in the TEST position and the MONITOR rotary switch is in the ERROR COUNT position, the error comparator inputs are selected by the ERROR COUNT switch.

(a) In position 0, the standard data and clock test outputs are selected as the input to the error comparator.

(b) In position 1, the I channel PN sequence generator output is selected as the error comparator input.

(c) In position 2, the output from the transmit bit synchronizer is selected as the error comparator inputs.

(d) In position 3, the relays on the data detector and driver cards of the RF demodulator are energized to apply compatible test outputs to the receive bit synchronizer. The I channel sign bit output from the decoder switch card and associated clock are selected as the comparator input.

(e) In position 4, the relays on the data detector and driver cards are again energized, but the Q channel sign bit from the decoder switch is applied to the comparator input.

(f) In position 5, the standard data and clock test outputs are selected as the input to the error comparator.

(g) In position 6, the alternate data and clock test outputs are applied to the error comparator.

(h) In position 7, the ICF test output from the input interface is selected as the comparator input.

(i) In position 8, the data output from the decoder switch is selected as the comparator input.

(j) In position 9, the error comparator input is again the data output of the decoder switch, but the clock signal is inverted.

(k) In position 10, the I channel MSB from the decoder switch card is selected as the error comparator input. In this case, the comparator input is compared to a sequence of all Zero's so that the error comparator produces an output pulse whenever the I channel MSB is a ONE. The MSB will be a ONE only when the integrator output fails to exceed the +0.6 volt level (para 2-9 d), thereby indicating a low

signal-to-noise ratio during the integration period.

(l) In position 11, the Q channel MSB from the decoder switch is selected for input to the comparator.

(m) In position 12, the phase channel MSB is applied to the error comparator input.

(n) In position 13, the I channel LSB is selected. The error comparator function is the same as for position 10 above. The meter reading for this position, in conjunction with the reading obtained when in position 10, gives a more accurate indication of the bit synchronizer operation based on the LSB value (para 2-9 d).

(o) In position 14, the Q channel LSB from the decoder switch is selected as the error comparator input.

(p) In position 15, the phase channel LSB is selected as the comparator input.

(5) The PN sequence generator card provides an output sync pulse to the front panel once during each cycle of the 2047 bit pattern. The data and clock outputs on the front panel are derived from the data and clock inputs from the test interface to the error comparator.

d. 11-Bit Pseudo-Random Sequence Generator (fig. FO-51)

(1) The pseudo-random sequence generator (A3A9) receives a clock input through gate U5 when P1-6 is high. P1-5 is connected externally to P1-45. P1-6 is low only when the MODE switch is in the OPERATE position, which disables the sequence generator. When the MODE switch is in LINK or TEST positions, the generator is enabled. The sequence -847-34/NAVELEX 0969 -LP169-5020/TO 31 R5 2G -282 generator consists of two 8-bit shift registers, U7 and U8, whose second and eleventh stages are exclusive OR'ed at Ull-6 (P1-14 is externally connected to P1-66), gated with the output of the zero-suppression gate network, U10, U12, and U13, and fed back to the shift register input. The zero-suppression circuit prevents the generator from being locked up with all zeros. If all gates receive all ZERO inputs, a ONE is clocked into the register. The resulting sequence has a period of 2047 bits. The output is clocked through flip-flop U9 to pin 11. A negative sync pulse is provided at the front panel SYNC connector by detecting state 11100000000 using NAND gate U14

(2) In conjunction with the data and clock selectors on the test interface card, U2 and U3 determine which test signal is applied to the error comparator input under control of the ERROR COUNT switch. The clock and data selectors, U2 and U3, respectively, are controlled by their A, B, and C inputs from OR gates IJ1 and U5, plus the strobe inputs from P1-53 and P1-61. The strobe inputs are HIGH during the ERROR COUNT settings of 0 through 7, thereby disabling U2 and U3. During the ERROR COUNT settings 8 through 15, the control inputs on pins 27, 62, 63, 30, 65, 28, and 64 of P1 (from the test interface card) determine the state of U2 and U3. Clock and data signals are applied to the selectors from various internal test points in the modem. The complement outputs are applied to the error comparator via P117 and P1-25 through the OR gates of U1 on the test interface card. The selected outputs are determined by the ERROR COUNT switch positions as shown in table 2-24.

Table 2-24. Test Switch Selections.

ERROR COUNT switch position	Pi -61 P1-53	Output at P1-17 from	Output at P1-25 from	Data
0-7	High	None	None	
8	Low	P1 - 16	P1-24	Decoder switch output
9	Low	P1-51	P1-59	Decoder switch output (clock inverted)
10	Low	P1-15	P1-z5	Decoder switch IMSB output
11	Low	P1-50	P1-58	Decoder switch Q MSB output
12	Low	P1-22	P1-18	Receive bit synchronizer AMSB output
13	Low	P1-57	P1-19	Decoder switch I LSB output
14	Low	P1-57	P1-20	Decoder switch Q LSB output
15	Low	P1-56	P1-21	Receive bit synchronizer OLSB output

(3) P1-49 is externally connected to P1-10 to allow flip-flop U9 to clock the Q channel PN sequence from the fifth stage of the PN generator. P1-5 is also externally connected to P1-42. The Q channel PN sequence is routed to the test interface card, pin 26, and to the encoder switch card, pin 25.

e. Test Interface (fig. FO-52). The test interface (A3A8) receives the control inputs from the ERROR COUNT switch and gates the appropriate test signal to the error comparator Driver circuits for the front panel outputs are also contained on this card. In addition,' a level converter for the Q channel PN sequence, a test relay driver, and meter input circuits are contained on the test interface card.

(1) Pins 20, 56, 19, and 54 receive the ERROR COUNT switch inputs to control data and clock selectors U4 and U3, respectively. When the ERROR COUNT switch is in positions 0 through 7, P1-54 is low and the A, B, and C inputs to the data and clock selector determine which test signals are applied to the error comparator through U1-11 and U1-3. The data and clock selectors on the PN sequence generator card are enabled for ERROR COUNT positions 8 through 15 and supply the inputs to the error comparator through P1-68 and P1-33. These inputs are also routed through U1-11 and U1-3 to the comparator. When the ERROR COUNT switch is in positions 8 through 15, U4 and U3 are disabled. U5 is a four line to ten line decoder used to convert the ERROR COUNT inputs to a format that is compatible with the control input to the data and clock selectors on the PN generator card. The outputs of U2 and U6 through U8 provide appropriate control signals to the error comparator and encoder switch cards during error count tests P1-14 goes low when the ERROR COUNT switch is in positions 10, 11, 13, and 14 to disable the sequence generator on the error comparator card. An external connection between P1-57 and P1-64 causes P1-27 to go low when the ERROR COUNT switch is in positions 3 and 4, thereby activating test relays on the data detector and driver cards of the RF demodulator. P1-22 is high when the ERROR COUNT switch is in positions 0 through 7 and disables the data and clock selectors on the PN generator card. Both the I and Q channel PN sequences are used to drive the RF modulator during QPSK self-test when the ERROR COUNT switch is in positions 8 through 15. In this condition, P1-23 is low. P1-15 controls the clock to the PN sequence generator and is low for ERROR COUNT switch positions 3 and 4 when in QPSK test.

(2) U9 and U10 are 50 ohm line drivers which supply output signals to the front panel connectors. The drivers of U9 provide a front panel output for the data and clock signals being applied to the error comparator input. Sync pulses from the PN sequence generator are provided to the front panel through R5-2G-282 U10-8. Similarly, error pulses from the error comparator output are routed through U10-6 for interface with an external counter.

(3) Whenever the source switch is in the test position, P1-63 is HIGH. This enables U1-6 to apply the Q channel PN sequence from the PN sequence generator card to the level converter circuits of Q1, Q2, and CR1 through CR4. Transistors Q1 and Q2 and ' diode bridge CR1 through CR4 develop a bipolar l1 volt test sequence through the Q channel data detector and driver card to the receive bit synchronizer. The circuit of R10, R11, and C4 provides filtering and level conversion between the control voltage to the 15 MHz VCXO of the transmit frequency synthesizer and the meter when the MONITOR rotary switch is in the XMIT RATE position. When the rotary switch is in the RCV RATE position, the circuit composed of R12, R13, and C5 provides filtering and level conversion between the 15 MHz VCXO control voltage in the receive frequency synthesizer and the meter.

f. Error Comparator (fig. FO-53). The error comparator (A3A10) receives data and clock from the selector circuits on the 11-bit pseudo-random sequence generator card. The comparator has two modes of operation; alpha measurement and error count.

(1) Shift registers U1 and U2, along with exclusive OR U8 and gates U9 and U10, make up the pseudo-random sequence generator. The eleventh stage of the shift register (P1-6) is applied to P1-68 by an external connection. Flip-flop U12 is cleared by a ground on P1-31 so that U8-5 is normally low. Data and clock are applied to pins 32 and 25. The input data from U8-6 is compared with sequence generator data at exclusive OR gate U8 and the results are applied to flip-flop U11-12. As long as the two data signals are identical, the output is low. If they are not the same, a high is generated which represents an error. The error signal at pin 51 is applied to the digital to analog meter card The error pulses are also gated with clock, inverted by U7, and applied through the digital to analog meter card and the test interface card to the front panel ERROR jack for external counting.

(2) When the ERROR COUNT switch is in one of the four alpha mode positions (settings 10, 11, 13, and 14), a low is applied to P1-42. The complement MSB and LSB soft decision data bits from the decoder interface are applied to pin 32 in these modes, in response to the ERROR COUNT switch setting. These inputs are high when an unreliable bit decision occurs. Exclusive OR gate US-1 has a constant low input because shift register U1 and U2 are held in the clear state by the low on pin 42. Any reliable decision results in a high at Ull-9.

(3) Binary counters U13 and U14 apply a reload input to down counters U5 and U6 for every 256 clock

pulses. A count equivalent to 64 counts is loaded by an externally connected high on pin 22. Pins 13, 43, 47, 12, 20, 19, 21, and 28 are externally grounded. Pin 29 is externally connected to pin 22. The count 256 output of U13 and U14, via P1-3, is applied to the D/A meter circuit. When the error signal is high at AND gate U9-13, clock pulses are gated through to downcount U5 and U6. If there are 64 errors within 256 clock pulses, an overflow signal is generated by U6-13. This pulse at pin 23 is applied to the D/A meter card. Manual/automatic resynchronization of the sequence generator is controlled by gates U9 and U10 which are enabled by a low at either pin 50 or pin 52. Pin 50 is low when the MONITOR switch is in the AUTO position. U10-5 is therefore enabled, allowing the overflow pulse, which is externally connected to P1-24, to clear shift register U3 and U4 (P1-14 is externally connected to P1-36). The resultant low at U4-13 causes gates U9 and U10 to load the input data into shift register Ul, U2. After 15 bits of input data have been loaded, U4-13 will go high again, since the shift register input is connected to a logic ONE, and the error comparator will revert back to normal operation. Placing the MONITOR switch in the MANUAL position places a ground on P1-52, which clear U3 and U4. When the switch is released, 15 bits of input data are loaded as described above.

g. Digital-to-Analog Meter (fig. FO-54). The digital-to-analog meter circuit (A3All) converts the digital error data to an analog signal which is applied to front panel MONITOR meter. In the condition of no error, pin 45 is low and OR gate U2-6 is high. Diodes CR1 and CR2 are forward-biased applying a voltage which back-biases CR3, and no current is applied to the meter from P1-9. An error causes pin 45 to go high. CR2 is then back-biased and CR3 and CR4 are forward-biased, causing meter current flow. Capacitor C1 filters the current flow. The resultant meter deflection is proportional to the number of errors. Full scale deflection equals 25 percent error rate (64 errors in 256 clock pulses).

(1) Limit flip-flop U1 prevents the meter from deflecting beyond full scale. U1 is preset by count 256 at pin 44, placing U1-9 high. When overflow condition occurs (greater than 64 errors in 256 pulses), a positive pulse at pin 7 clocks a low to U1. The low satisfies OR gate U2. The meter current flow is cut off until the next count 256 pulse.

(2) U3 through U5 and U9 provide a switching capability to regulate the input to the D/A converter circuit and to select the output to the front panel ERROR connector. When the MONITOR rotary switch is in the SIG/NOISE position, pin 65 is low and pin 63 is high. Gates U5-11, U5-3, and U9-11 are therefore disabled while U4-8, U9-3, and U9-6 are enabled. The outputs from the error comparator to pin 15, 60, and 28 are disabled. When in the QPSK 847-34/NAVELEX 0969-LP169-5020/TO 31R5-2G-282 mode, pin 62 and 13 are high while pin 26 is low. This allows both the I and Q channel MSB data bits to be multiplexed and applied to the D/A converter input (pins 61 and 45 are externally connected). When in the BPSK mode, pin 62 and 13 are low while pin 26, which is connected to pin 48, is high. This allows the I channel MSB to be applied through U4-6 to the D/A converter. This D/A converter input is also applied through U5-6 to the test interface and thence to the front panel error output.

(3) When the MONITOR rotary switch is in the BER position, pins 65 and 47 are high and pins 63 and 11 are low. The D/A converter input is processed through U5-11, U4-6, and pin 61 to the D/A converter (P1-45). The error pulses from the error comparator are also forwarded through U5-3, U5-6, and the driver on the test interface card to the front panel connector. The overflow signal from the error comparator is also forwarded through U9-11 to Ul-10 (pin 64 is externally connected to pin 44).

(4) Clock pulses at pin 12 trigger retriggerable one-shot U6, thus keeping its output high. If clock pulses are lost, the one-shot output returns to a low. The low satisfies OR gate U2, thus cutting off meter current flow.

(5) The selected data and clock at pins 46 and 10, respectively, are applied to inverters and drivers. The outputs drive the DATA 1 and 0 and the CLOCK 1 and 0 front panel indicators.

h. Alarm Circuits (fig. FO-55). The alarm circuits (A3A12) monitor the transmit and receive sections of the modem. In the event a fault occurs in the transmit power or bit synchronizer or the receive power, phase lock loop, or bit synchronizer, an alarm signal is generated. When a fault occurs, a high logic level is applied to the inverter of the appropriate latching circuit. The output from the latching circuit activates a monostable multivibrator which produces a square wave output to the corresponding fault indicator on the front panel. This output causes the normally off indicator to blink on and off at approximately three times per second. In addition to the blinking indication, an audible alarm sounds. When the fault has been remedied, the indicator remains on until the ALARM switch is momentarily switched to the RESET position (the RESET position also acts as a lamp test for the indicators). The SECTION indicators illuminate when a fault occurs and remain on until reset, but they do not blink. This card also contains the indicator driver, U8-8, for the TRANSMIT MONITOR indicator.

(1) The alarm circuits card contains six alarm detectors. One detector, made up of inverter U3-2, latch U2-3 and 11, NAD gate U4-3, OR gate U4-11, and indicator driver U5-10, is discussed. The RESET signal places a low at pin 52, latching U2-3 high. The low at pin 52 also places a low through CR1 to pin 50

to test the front panel indicator. The low at U4-12 satisfies OR gate U4, thus keeping the indicator off when the RESET is released. When the associated fault occurs, pin 32 goes high. This high, inverted by U3, sets latch U2-3 low and U2-11 high. The high also enables AND gate U4-2. U4-1 receives a square wave signal from the flasher circuit. When the flasher input is high, U4-8 is low, flashing the indicator off. When the flasher input is low, U4-3 is high and the indicator is on. The low at U6-1 causes a low at pin 22, thus turning the RECEIVE section fault indicator on. The high at U6-6 activates alarm relay driver U1 and relay K1 energizes, causing the audible alarm to sound. If the high (fault) input should go low, the circuit will remain latched, but the -low at U4-2 will disable the flasher input, keeping the indicator in the steady-on condition.

(2) The low of U7-8 also activates the flasher square wave generator, Ull, U12 and associated circuitry. One-shot, Ull, is initially triggered by this low. U11's Q output goes low, then returns high at the end of the one-shot operation. The return to high triggers one-shot, U12. The Q output of U12, in turn, retriggers Ull. This operation continues as long as the low at Ull-1 or -2 remains. The square wave output from Ull-8 is applied to AND gate U4-1 and the other fault circuits. The other alarm detect circuits operate the same although the circuits associated with P1-66, P1-31, P1-28, and P1-30 are activated by a low input.

CHAPTER 3
MAINTENANCE INSTRUCTIONS

Section I. INTRODUCTION

3-1. General

This chapter contains detailed procedures for maintenance of the QPSK/BPSK modem. Preventive maintenance procedures are used to insure that minor equipment degradations are not neglected until the equipment becomes inoperable. Modem troubleshooting is accomplished primarily through use of self-test procedures which isolate malfunctions to one or several cards, the replacement of which will clear the fault Modem alinement procedures provide a means of optimizing modem performance. The modem performance is periodically verified through the bit error rate measurement procedures provided herein.

3-2. Tools, Test Equipment, and Material Required for Maintenance

Material required for cleaning are lint-free cleaning cloths, a soft-bristle brush, and a cleaning compound/solvent. For general repairs, a standard electronic technician tool kit is required. Additionally, the required test equipment, or their equivalents, are listed in table 3-1 The required tools and materials are listed in table 3-2.

3-3. Preventive Maintenance

Preventive maintenance checks and services are performed by operator and organizational

Table 3-1. Test equipment Required.

Name	Part/model number	Manufacturer
Oscilloscope	485A	Tektronix
Digital Voltmeter	8000A-01	Fluke
Power Meter, With Thermistor Mount	ME-441/U, ME-7772/U	Hewlett-Packard
RF Power Meter	MV-828A	Milivac
Attenuator, Step	HP 356C	Hewlett-Packard
Attenuator, Step	HP 35D	Hewlett-Packard
Multimeter	ME-419	Simpson
Electronic Frequency Center, With Frequency Converter Plugin	AN/USM - 122A; AN/GRM-32D	Hewlett-Packard
Digital Communications Teat Set	TS-8642(V) I/G	Harris ESD
Error Rate Counter	TS-8641/G	Harris ESD
Modem Tat Set	TS-8580/G	

Table 3-2. Tools and Materials Required.

Name	Part/model number	Manufacturer
Tool Kit Electronic Equipment	TK-106/G	
Card Extender	SM-D-87735	Harris ESD
Card Extender (2 each)	SM-D-759649	Harris ESD
Card Puller, Single Card	17920	Protolab
Card Puller, Double Card	1428678	Protolab
RTV Rubber (as required)	8145RTV	Dow Corning

maintenance personnel Refer to TM 11-5820-847-12 for procedures

3-4. Operational Checks

The following procedure, when properly performed, does not interrupt digital traffic Do not disturb any control settings except as directed in the procedure In the sequence shown in table 3-3, set the front panel switch listed in the first column to each position listed in the second column. For each switch position, observe the indicator(s) listed in the third column, and verify proper operation as specified in the fourth column If the required indication is not obtained, perform the corrective action indicated In the final column Upon conclusion of the test, return the ALARM and MONITOR meter switches to their normal operating positions 1R5-2G-282

3-5. Cleaning

a Remove dust and loose dirt with a clean, soft lint free 0 clothe.

b Remove dust, dirt, and other foreign matter from all plugs and jacks with a soft-bristle brush WARNING
The fumes of trichloroethane are toxic Provide thorough ventilation whenever used. DO NOT USE NEAR OPEN FLAME.

Trichloroethane is not flammable, but exposure of its fumes to an open flame or hot metal forms a highly toxic phosgene gas.

c Remove grease, fungus, and ground-in dirt with a lint-free cloth dampened with cleaning material.

Table 3-3. Operational Checks.

Switch	Setting	Indicator	Required Indication	Corrective section
POWER	Illuminated	Replace lamp		
All MONITOR indicators	Illuminated	Replace lamp(s)		
ALARM RESET/OFF/ ON	Hold m RESET position indicators	ALL ALARMP and FAULT	Illuminated	Replace lamp(s)
Audible alarm	Tone	Troubleshoot modem		
ALARM RESET/OFF/ ON	Release to OFF	ALL ALARM and FAULT	Extinguished	Troubleshoot modem
		Audible alarm	No tone	Troubleshoot modem
MONITOR meter function	DC PWR	MONITOR meter	46 to 54	Troubleshoot modem
select switch	RCVR SYNTH	MONITOR meter	40 to 50	Troubleshoot modem
DEMOD AGC	MONITOR meter	0 to 100, no drift		Troubleshoot modem
DEMOD VCXO	MONITOR meter	35 to 65		Troubleshoot modem
SIG/NOISE	MONITOR meter	per site requirements		Troubleshoot modem

Section II. MODEM TROUBLESHOOTING

3-6. General

The maintenance personnel will, as required, perform the self-test procedure in this section as required to localize a fault. This procedure localizes a fault to one or more printed-circuit cards or plug-in subassemblies. Corrective action consist of interchanging those cards or subassemblies with possible faults with card or subassemblies known to be good Items are interchanged one at a time, in the order listed in each referenced corrective action table, until the fault is corrected. Additional information required to localize failures in the switches, blowers, indicators, and other items associated with the chassis and panels is also included.

CAUTION

The modem covers must be in place for proper air flow to ensure equipment cooling. If the cover(s) are removed for extended period (30 minutes or more), an external fan must be set up with air flow directly into the modem. Failure to observe this precaution will result in equipment damage.

3-7. Troubleshooting Procedure

a. Perform the self-test procedure in accordance with paragraph 3-8. The self-test procedure defines a series of operations with corresponding requirements for resultant indications. If, at any point in the self test procedure, the expected indication fails to occur, the appropriate corrective action is referenced.

b. Perform the corrective action in accordance with the portion of paragraph 3-9 that is referenced in the self-test procedure When the corrective action appears to have corrected the fault indication, confirm operability by repeating the entire self-test procedure. If the corrective actions given in paragraph 3-9 fail to correct the faulty indication,

refer to paragraph 3-10 to localize faults in the components that are not plug-in replaceable.

NOTE

Before any lengthy continuity tests are performed, it is recommended that the modem be returned to its original condition and the troubleshooting procedure be repeated to ensure that the malfunction indication did not result from operator error.

c. After successful conclusion of self-test procedures following a corrective action, perform the test procedure in accordance with paragraph 3-38 for only those data rates currently being used. If the test is successful, the modem may be returned to service immediately, if required. If the modem is not required in service immediately, the complete performance test procedure of paragraph 3-38 should be executed to ensure that the modem is operating within specifications.

NOTE

Although the self-test procedure will detect major failures, it is possible that the modem may be operating with degraded performance that will not cause a self-test failure indication. Therefore, the performance test (para 3-38), which will detect degraded performance, should be performed periodically and as soon after repair as possible.

3-8. Self-Test Procedure

CAUTION

Performing self-test on a modem while the system is operating interrupts digital user communications on both the transmit and receive links. If the self-test requires setting the TRANSMIT INPUT DATA RATE switches to any rate greater than the operational rate, the terminal output power for the carrier associated with the modem under test should be reduced.

a. If the modem is operating, initiate the test by changing the modem switch settings as required to correspond to table 3-4.

b. If modem is nonoperating, set the controls as follows and allow 30 minutes warmup, then change switch settings to correspond to table 3-4.

Control	Position
MODE	LINK
TRANSMIT ENCODER EXT/OFF	Normal operational setting.
TRANSMIT INPUT DATA RATE	Normal operational setting.
ALARM RESET/OFF/ON	OFF

c. Perform the self-test in accordance with table **3-5 and the following instructions:**

Table 3-4. Self-Test Initial Switch Setting.

Control section	Switch	Position
ALARM	RESET/OFF/ON	OFF.
MODE	OPERATE/LINK/TEST	TEST.
TRANSMIT	INPUT DATA RATE	Same as operational input data rate.
	QPSK/BPSK	Same as operational setting.
	ENCODER DIFF/OFF	DIFF.
	ENCODER EXT/OFF	OFF
RECEIVE	I CHANNEL SYMBOL RATE	Same as operational TRANSMIT INPUT DATA RATE for BPSK Same as one-half operational TRANSMIT INPUT DATA RATE for QPSK-
QPSK/BPSK		Same as operational setting of TRANSMIT QPSK/BPSK switch.
	DECODER DIFF/OFF	DIFF.
	DECODER EXT/OFF	DIFF.
MONITOR	Meter	DIFF.
	ERROR COUNT	0
	AUTO/MANUAL	AUTO.
Power	ON/off	ON.
Behind front panel	SOURCE	Same as operational setting.
	SWEEP NORMAL/WIDE	NORMAL.
	SWEEP FAST/NORMAL	NORMAL.
	SWEEP PARTAL/FU	FULL.
	RANDOMIZER TRANSMIT	OFF.
	RANDOMIZER RECEIVER	OFF.

Table 3-5. Self-Test Procedure.

(Control section) switch	Setting	Indicator	Normal indication	Crrective action
——	——	POWER.	Illuminated.	table 3–7.
(ALARM) RESET/OFF/ON.	Hold in RESET position.	All ALARM and FAULT indicators.	Illuminated.	table 3–8.
		Audible alarm.	Tone.	table 3–8.
(ALARM) RESET/OFF/ON.	Release to OFF.	Audible alarm.	No tone.	table 3–9.
		TEMPERATURE.	Extinguished.	table 3–9.
(MONITOR) meter.	DC PWR	Meter.	46 to 54.	table 3–10.
	XMIT SYNTH	Meter.	40 to 60.	table 3–11.
	RCVR SYNTH	Meter.	40 to 60.	table 3–12.
	DEMOD AGC	Meter.	72 to 92*	table 3–13.
	DEMOD VCXO	Meter.	40 to 60	table 3–14.
(MONITOR) meter switch ERROR COUNT.	0	*a.* Meter.	0	table 3–15.
		b ALL MONITOR indicators.	Illuminated.	table 3–15.
	1	Same as *a* and *b* above.	No change.	table 3–16.
	2	Same as *a* and *b* above.	No change.	table 3–17.
	3	Same as *a* and *b* above.	No change.	table 3–18.
	4	Same as *a* and *b* above.	No change.	table 3–19.
	5	*a.* Same as *a* and *b* above.	*a.* No change.	table 3–20.
		b TRANSMIT MODULATOR TEST indicator.	*b.* Illuminated.	
(MONITOR) meter switch ERROR COUNT— NOTE For positions 8 through 15 of the MONITOR ERROR COUNT test switch, the RECEIVE I CHANNEL SYMBOL RATE switch setting must equal the TRANSMIT INPUT DATA RATE switch setting	6	Same as *a* and *b* above.	No change.	table 3–21.
	7	Same as *a* and *b* above.	No change	table 3–22.
	8	Same as *a* and *b* above.	No change.	table 3–23.
	9	Same as *a* and *b* above	No change	table 3–24.
	10	*a.* Meter	*a.* < 2	table 3–23.
		b DATA 1	*b.* Off.	
		c. Remaining MONITOR indicators	*c.* Illuminated.	
	11	*a.* Meter.	*a.* < 2	table 3–24.
		b DATA 1.	*b* Off.	
		c. Remaining MONITOR indicators.	*c.* Illuminated.	
	12	*a.* Meter.	*a.* <2	table 3–25.
		b. All MONITOR indicators.	*b* Illuminated.	
	13	*a.* Meter	*a.* < 25	table 3–23.
		b. DATA 1.	*b.* Off	
		c. Remaining MONITOR indicators	*c.* Illuminated.	
	14	*a.* Meter	*a.* < 25	table 3–24.
		b DATA 1.	*b* Off.	
		c. Remaining MONITOR indicators.	*c.* Illuminated	
	15	*a.* Meter.	*a.* < 25	table 3–25
		b All MONITOR indicators.	*b* Illuminated.	
(MONITOR) meter switch.	SIG/NOISE	Meter	0.	table 3–26.
		ALL MONITOR indicators.	Illuminated	table 3–26.
(MONITOR) test.	BIT SYNC AGC I	Meter.	30 to 60	table 3–23.
	BIT SYNC AGC Q	Meter.	30 to 60.	table 3–24.
	XMIT RATE	Meter.	40 to 60.	table 3–27.
	RCV RATE	Meter.	40 to 60.	table 3–28.
(ALARM) RESET/OFF/ON.	RESET (momentary).	All ALARM and FAULT indicators.	Extinguished.	table 3–29.

*35 to 55 if S1 on the 70-MHz AGC amplifier card is in position 2 (0 to -55 dbm input power range).

NOTE

For positions 8 through 15 of the MONITOR ERROR COUNT test switch, the RECEIVE I CHANNEL SYMBOL RATE switch setting must equal the TRANSMIT INPUT DATA RATE switch setting.

(1) In the sequence shown in table 3-5, set each front panel switch indicated in the first column to the corresponding setting(s) indicated in the second column.

(2) For each switch setting, observe the indicator(s) listed in the third column, and verify the results required by the fourth column. A corrective action reference is contained in the final column.

(3) If the RANDOMIZER TRANSMIT and RECEIVE switches are used in the ON position (QPSK operation only) as an operational requirement, perform the self-test with these two switches OFF. Then repeat the procedure of table 3-5 with the RANDOMIZER TRANSMIT and RECEIVE switches in the ON position.

d. When the operational settings of the INPUT DATA RATE and QPSK/BPSK switches for the TRANSMIT control section are not compatible with the operational settings of the I CHANNEL SYMBOL RATE and QPSK/BPSK switches of the RECEIVE control section, the procedures of table 3-5 must be repeated. When necessary to repeat the test, the RECEIVE I CHANNEL SYMBOL RATE and QPSK/BPSK operational switch settings provide the basis for test switch settings. If the operational setting of the QPSK/BPSK switch in the RECEIVE control section is in BPSK, the repeated procedure is run with the TRANSMIT INPUT DATA RATE equal to the operational RECEIVE I CHANNEL SYMBOL RATE settings and the TRANSMIT QPSK/BPSK switch in the BPSK position. If the operational setting of the RECEIVE QPSK/BPSK switch is in QPSK, the repeated procedure is run with the TRANSMIT INPUT DATA RATE equal to twice the operational RECEIVE I CHANNEL SYMBOL RATE settings and the TRANSMIT QPSK/BPSK switch in the QPSK position. Thus, the transmit and receive sides of the modem are each tested under operational conditions.

NOTE

If both TRANSMIT ENCODER and RECEIVE DECODER EXT/OFF switches are operationally set to OFF, omit procedures of table 3-6.

e. If the RECEIVE DECODER EXT./OFF switch is operationally set to EXT, set both TRANSMIT ENCODER and RECEIVE DECODER EXT/OFF switches to the OFF position, set RECEIVE I CHANNEL SYMBOL RATE switches to operational positions, and set TRANSMIT INPUT DATA RATE switches to one-half the operational RECEIVE I CHANNEL SYMBOL RATE. Then perform the coder test in accordance with table 3-6.

f. If the TRANSMIT ENCODER EXT/OFF switch is operationally set to EXT, set both TRANSMIT and RECEIVE EXT/OFF switches to the OFF position, set TRANSMIT INPUT DATA RATE switches to operational positions, and set RECEIVE I CHANNEL SYMBOL RATE switches to twice the TRANSMIT INPUT DATA'RATE. Then perform (or repeat) the encoder test in accordance with table 3-6.

3-9. Corrective Actions.

The following corrective action procedure provides a means of isolating a failed subassembly and repairing the modem. Table 3-7 through 3-30 contain the fault isolation procedures to be used if a self-test failure is detected. Table 3-31 lists the alinement or adjustment procedures required after the replacement of certain subassemblies. Perform the fault isolation as follows: a, Perform self-test. If a fault occurs, proceed to the fault isolation procedure referenced in the self-test table. Perform any additional observations or tests required by the table and use this information to select the required corrective actions.

Table 3-6. Encode/Decoder Test Procedure.

(Control section) switch	Setting	Indicator	Normal Indication	Corrective action
(MONITOR) test	ERROR COUNT	--	--.	
(MONITOR) meter	ERROR COUNT	Meter	0	table 3-30
(ALARM)	RESET (momentary)	All MONITOR indicators	Illuminated	table 3-30
RESET/OFF/ON		ALL FAULT indicators	Extinguished	table 3-30

Table 3-7. Fault Isolation Procedure (POWER Indicator).

Symptom	Corrective action	Notes
POWER indicator extinguished	1 If other front panel indicators are illuminated, replace indicator lamp, DS15	Failed indicator lamp.
	2. Check fuse A1F1. Replace if necessary	
	3. Check ac line cord	
	4. Disconnect connector P1 from the power supply and again reset the switch to the ON position If power indicator is illuminated and fuse A1F1 is good, replace power supply assembly PS1* If indicator is extinguished, replace A1S12.	Failed power supply or switch
	5. Check chassis wiring, fans, and test relay Repair or replace if required	
One or more FAULT indicators extinguished.	1 If no FAULT indicators are illuminated, proceed to step 2. If other indicators are illuminated, perform *a* and *b* below.	
	a. Replace faulty indicator bulb.	
	b Replace A3A12.	Alarm circuits (SM−D−742033).
	2 Operate MONITOR meter switch to DC PWR position If meter reading is less than 46, or if all MONITOR lights are out, replace power supply PSI*	
	3 Check ALARM RESET switch, A1S1, and replace if required	RESET position.
No audible alarm.	Replace	
	a. A3A12	Alarm circuits (SM−D−742033).
	b. A1DS4	Audible alarm.

Table 3-8. Fault Isolation Procedure (ALARM RESET).

Symptom	Corrective action	Notes
One or more FAULT indicator extinguished	1 If no FAULT indicators are illuminated, proceed to step 2 If other indicators are illuminated, perform *a* and *b* below	
	a. Replace faulty indicator bulb.	
	b Replace A3A12.	Alarm circuits (SM−D−742033).
	2. Operate MONITOR meter switch to DC PWR position. If meter reading is less than 46, or if all MONITOR lights are out, replace power supply PS1*.	
	3 Check ALARM RESET switch, A1S1, and replace if required.	RESET position.
No audible alarm.	Replace	
	a. A3A12	Alarm circuits (SM−D−742033).
	b A1DS4	Audible alarm.

Table 3-9. Fault Isolation Procedure (ALARM REST OFF).

Symptom	Corrective action	Notes
Audible alarm tone or TEMPERATURE on.	Replace. a. A3A12 b Thermostat S1	Alarm circuits (SM−D−742033) Located on inside rear panel near blowers

Table 3-10. Fault Isolation Procedure (DC PWR).

Symptom	Corrective action	Notes
Meter indication out of limits	Replace· a. PS1* b A2A29 c A1M1	 Power supply B/S buffer (SM−D−877695) Meter.

Table 3-11. Fault Isolation Procedure (RCVR S YNTH).

Symptom	Corrective action	Notes
Meter indication not within limits (40 to 60), or is sweeping.	Replace a. A3A48 b A3A43 c A3A40 d A3A41 e. A3A42 f A3A47 g A1A1	Wait approximately 15 seconds for proper indication after each replacement 45 MHz PPL (SM−D−742113) Reference oscillator (SM−D−742129) Counter encoder (SM−D−742105) Program divider (SM−D−742109) Reference divider (SM−D−742133) 45 MHz amp (SM−D−742117) TRANSMIT INPUT DATA RATE thumb-wheel switches

Table 3-12. Fault Isolation Procedure (RCVR SYNTH)

Symptom	Corrective action	Notes
Meter indication not within limits (40 to 60), or is sweeping	Replace. a. A3A24 b A3A19 c A3A16 d. A3A17 e. A3A18 f A3A23 g A1A2	Wait approximately 15 seconds for proper indication after each replacement 45 MHz PLL (SM−D−742113). Reference oscillator (SM−D−742129). Counter encoder (SM−D−742105) Programmable divider (SM−D−742109) Reference divider (SM−D−742133) 45 MHz amp (SM−D−742117) RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches

Table 3-13. Fault Isolation Procedure (DEMOD A GC).

Symptom	Corrective action	Notes
Meter indication not within limits (35 to 55, or 72 to 92) (table 3−5).	1. If the TRANSMIT MODULATOR TEST indicator is extinguished, replace. a. A2A2 b A2A1 2 Momentarily reset the ALARM RESET/ OFF/ON switch. If the TRANSMIT PWR FAULT indicator illuminates, replace· a. A2A1 b A2A27 c. A2A26 d A2A2	 70 MHz oscillator (SM−D−731193). Data receiver and modulator (SM−D−877650) Data receiver and modulator (SM−D−877650) 70-MHz amplifier (SM−D−731189) Modulation filters (SM−D−731185) 70-MHz oscillator (SM−D−731193)

Table 3-13. Fault Isolation Procedure (DEMOD AGC)-Continued.

Symptom	Corrective action	Notes
Meter indication not within limits —Continued.	8. If the TRANSMIT MODULATOR TEST indicator is illuminated and the TRANSMIT PWR FAULT indicator is extinguished, replace:	Wait approximately 30 seconds for proper indication after each replacement.
	a. A3A32	Relay control (SM-D-877710).
	b. A2A16*	70-MHz GCA (SM-D-877675).
	c. A2A18*	Filters and distribution ampls (SM-D-877645).
	d. A2A20*	X2/X4 multiplier (SM-D-877660).
	e. A2A19*	Coherent detector and AGC loop ampl (SM-D-877665).
	f. A2A24*	PLL amplifier and sweep generator (SM-D-877670).)

Table 3-14. Fault Isolation Procedure (DEMOD VCXO).

Symptom	Corrective action	Notes
Meter indication not within limits (40 to 60), sweeping continuously, or at reset limits.	Replace:	Wait approximately 30 seconds for proper indication after each replacement.
	a. A2A22*	Ref X2/X4 multiplier (SM-D-877655).
	b. A2A24*	PLL ampl and sweep circuit (SM-D-877670).
	c A3A32	Relay control (SM-D-877710)
	d. A2A20*	X2/X4 multiplier (SM-D-877660).
	e. A2A47*	Acquisition control (SM-D-877685).
	f. A2A35	Quadrature detector (SM-D-877690).
	g. A2A19*	Coherent detector and AGC loop ampl (SM-D-877665).

Table 3-15. Fault Isolation Procedure (ERROR COUNT o).

Symptom	Corrective action	Notes
DATA 1 or 0 or CLOCK 1 or 0 extinguished or meter indication other than 0.	Resume the self-test procedure with test number 1.	

Table 3-16. Fault Isolation Procedure (ERROR COUNT 1).

Symptom	Corrective action	Notes
CLOCK 1 or 0 extinguished.	Replace:	
	a. A3A39*	Stable clock (SM-D-781201).
	b. A3A43	Reference oscillator (SM-D-742129).
	c. A3A33	Reference divider (SM-D-742133).
	d. A3A6	Encoder switch (SM-D-877730).
	e. A3A9	PN sequence generator (SM-D-742057).
	f. A3A8	Test interface (SM-D-877705).
	g. A3A11	D/A meter (SM-D-877725).
	h. CLOCK 1 or 0 indicator.	
DATE 1 or 0 extinguished.	Replace:	
	a. A3A9	PN sequence generator (SM-D-742057).
	b. A3A8	Test interface (SM-D-877705)
	c. A3A11	D/A meter (SM-D-877725).
	d. DATA 1 or 0 indicator.	
Meter indication other than 0.	Replace:	
	a. A3A9	PN sequence generator (SM-D-742057).
	b. A3A10	Error comparator (SM-D-742061).
	c. A3A11	D/A meter (SM-D-877725).
	d. A3A8	Test interface (SM-D-877705).
	e. A3A5	Input interface (SM-D-742037).

Table 3-17. Fault Isolation Procedure (ERROR COUNT 2).

Symptom	Corrective action	Notes
CLOCK 1 or 0 extinguished	Replace	
	a. A3A43	Reference oscillator (SM-D-742129)
	b A3A42	Reference divider (SM-D-742133)
	c A3A45	15-MHz ampl (SM-D-742121)
	d A3A46	Mixer/output ampl (SM-D-742125)
	e A3A35	Transmit bit detector (SM-D-742045)
	f A3A33	Randomizer/derandomizer (SM-D-877780)
	g Y2*	VCO (SM-A-731369-1)
DATA 1 or 0 extinguished.	Replace	
	a. A3A5**	Input interface (SM-D-742037)
	b A3A35	Transmit bit detector (SM-D-742045)
	c A3A33	Randomizer/derandomizer (SM-D-877780).
Meter indication other than 0.	1 Replace	
	a. A3A37	D/A converter (SM-D-731217)
	b. A3A36	Loop filter (SM-D-731221)
	c A3A35	Transmit bit detector (SM-D-742045)
	d. A3A43	Reference oscillator (SM-D-742129)
	e A3A42	Reference divider (SM-D-742133)
	f A3A45	15 MHz ampl (SM-D-742121)
	g A3A46	Mixer/output amp (SM-D-742125)
	h A3A33	Randomizer/derandomizer (SM-D-877780)
	i Y2*	VCO (SM-A-741369-1)
MODULATOR TEST extinguished	Replace:	
	a. A2A2*	70-MHz oscillator (SM-D-731193)
	b. A2A1*	Data receiver and modulator (SM-D-877650)
	c A3A6*	Encoder switch (SM-D-877730)
	d A3A27**	Encoder interface (SM-D-742049)
	e A3A12	Alarm circuits (SM-D-742033)
	f A1DS11	MODULATOR TEST indicator lamp

Table 3-18. Fault Isolation Procedure (ERROR COUNT 3).

Symptom	Corrective action	Notes
CLOCK 1 or 0 extinguished.	Replace:	
	a. A3A22*	Mixer/output ampl (SM-D-742125)
	b. A3A18	Reference divider (SM-D-742133)
	c. A3A21	15-MHz ampl (SM-D-742121)
	d. A3A7	Decoder switch (SM-D-877700)
	e A2A29	B/S buffer (SM-D-877695).
	f A3A8	Test interface (SM-D-877705)
	g A3A13	Phase and loss of lock detector (SM-D-731225/877926).
	h. A3A19	Reference oscillator (SM-D-742129)
	i. Y1*	VCO (SM-A-731369-1)
DATA 1 or 0 extinguished.	Replace	
	a. A2A8*	I channel data quantizer (SM-D-731213)
	b A2A10*	I channel data integrator (SM-D-731205)
	c A3A7	Decoder switch (SM-D-877700)
	d. A2A31*	Timing and AGC (SM-D-731229/877931
	e A2A12*	I channel data detector and driver (SM-D-731173)
	f A3A5**	Input interface (SM-D-742037)
	g A3A8	Test interface (SM-D-877705)
	h. A2A29	B/S buffer (SM-D-877695)
Meter indication other than 0.	Replace	
	a. A3A7	Decoder switch (SM-D-877700)
	b A313	Phase and loss of lock detector (SM-D-731225/877926).
	c. A3A15	D/A converter (SM-D-731217)
	d A3A14	Loop filter (SM-D-731221)

Table 3-18. Fault Isolation Procedure (ERROR COUNT 3) -- Continued.

Symptom	Corrective action	Notes
Meter indication other than 0 — Continued.	*e* A3A21	15 MHz ampl (SM−D−742121)
	f A2A29	B/S buffer (SM−D−877695)
	g A2A10*	I channel data integrator (SM−D−731205)
	h A2A6*	Phase integrator (SM−D−731205)
	i A2A8*	I channel quantizer (SM−D−731213)
	j A2A4*	Phase channel quantizer (SM−D−731213)
	k A2A9*	I channel data dump (SM−D−731209)
	l A2A5*	Phase channel dump (SM−D−731209)
	m A2A31*	Timing and AGC (SM−D−731229/877930).
	n Y2*	VCO (SM−A−731369−1)

Table 3-19. Fault Isolation Procedure (ERROR COUNT 4).

Symptom	Corrective action	Notes
CLOCK 1 or 0 extinguished	Replace	
	a. A3A7	Decoder switch (SM−D−877700)
DATA 1 or 0 extinguished	Replace	
	a. A2A32*	Q channel data quantizer (SM−D−731213)
	b A2A34*	Q channel data integrator (SM−D−731205)
	c A2A30*	Timing and AGC (SM−D−731229 /877930).
	d A3A8	Test interface (SM−D−877705)
	e A2A29	B/S buffer (SM−D−877695)
	f A3A7	Decoder switch (SM−D−877700)
	g A3A9	PN sequence generator (SM−D−742057)
	h A2A36	Q channel data detector and driver (SM−D−731173)
Meter indication other than 0	Replace	
	a A2A32*	Q channel data quantizer (SM−D−731213)
	b A2A34*	Q channel data integrator (SM−D−731205)
	c A2A33*	Q channel data dump (SM−D−731209)
	d A2A30*	Timing and AGC (SM−D−731229/877930).
	e A2A29	B/S buffer (SM−D−877695)
	f A3A7	Decoder switch (SM−D−877700)

Table 3-20. Fault Isolation Procedure (ERROR COUNT 5).

Symptom	Corrective action	Notes
CLOCK 1 or 0 extinguished	Replace	
	a. A3A31**	Standard line driver (SM−D−742053)
	b A3A7	Decoder switch (SM−D−877700)
	c A3A28	Decoder interface (SM−D−742049)
	d A3A33	Randomizer/derandomizer (SM−D−877780)
DATA 1 or 0 extinguished	1 IF MODULATOR TEST indicator is illuminated, go to 2 below If not, replace	After each card replacement, reset fault circuits using ALARM RESET/OFF/ON switch
	a A3A6*	Encoder switch (SM−D−877730)
	b A3A27	Encoder interface (SM−D−742049)
	c A2A1	Data modulator (SM−D−877650)
	d A3A33	Randomizer/derandomizer (SM−D−877780)
	2 Replace	
	a A3A31	Standard line driver (SM−D−742053)
	b A3A7	Decoder switch (SM−D−877700)
	c A3A28	Decoder interface (SM−D−742049)
	d A3A33	Randomizer/derandomizer (SM−D−8877780)
Meter indication other than 0	Replace	Allow 45 seconds for demodulator acquisition after each card replacement
	a. A2A12*	I channel data detector and driver (SM−D−731173)

Table 3-20. Fault Isolation Procedure (ERROR COUNT 5) - Continued.

Symptom	Corrective action	Notes
Meter indication other than 0 — Continued	*b* A2A36	Q channel data detector and driver (SM−D−731173)
	c. A2A14*	Phase adj and det driver (SM−D−877680)
	d A2A18*	Filters and distr ampl (SM−D−877645)
	e A2A16*	70-MHz GCA (SM−D−877675)
	f A3A32	Relay control (SM−D−877710)

Table 3-21. Fault Isolation Procedure (ERROR COUNT6).

Symptom	Corrective action	Notes
DATA 1 or 0 or CLOCK 1 or 0 extinguished or meter indication other than 0	Replace *a* A3A30**	Alternate line driver (SM−D−742053)

Table 3-22. Fault Isolation Procedures (ERROR COUNT 7).

Symptom	Corrective action	Notes
DATA 1 or 0 or CLOCK 1 or 0 extinguished or meter indication other than 0	Replace	
	a. A3A4**	LOS/cable driver (SM−D−742081)
	b A3A2*	LOS/cable receiver (SM−D−742089)
	c A3A5**	Input interface (SM−D−742037)

Table 3-23. Fault Isolation Procedure (ERROR COUNT 8 or 10 and BIT SYNC AGC I).

Symptom	Corrective action	Notes
Meter out of limit	Replace	
	a. A2A12*	I channel data detector and driver (SM−D−731173)
	b A2A8*	I channel data quantizer (SM−D−731213)
	c A2A9*	I channel data pump (SM−D−731209)
	d A2A10*	I channel data integrator (SM−D−731205).
	e. A2A31*	Timing and AGC (SM−D−731229/877930)
	f. A2A14*	Phase adj and det driver (SM−D−877680)
DATA 1 indicator illuminated or remaining indicator not illuminated	Replace	
	a. A2A29	B/S buffer (SM−D−877695)
	b A3A7	Decoder switch (SM−D−877700)
	c A3A9	PN sequence generator (SM−D−742057)
	d A3A11	D/A meter (SM−D−877725)

Table 3-24. Fault Isolation Procedure (ERROR COUNT9 or 11 and BITSYNC AGC Q).

Symptom	Corrective action	Notes
Meter reading out of limits	Replace	
	a. A2A32*	Q channel data quantizer (SM−D−731213)
	b A2A33*	Q channel data dump (SM−D−731209)
	c A2A34*	Q channel data integrator (SM−D−731205)
	d A2A30*	Timing and AGC (SM−D−731229/877930).
	e A2A36	Q channel data detector and driver (SM−D−731173)
	f A2A14*	Phase adj and det driver (SM−D−877680)

Table 3-24. Fault Isolation Procedure (ERROR CO UNT9 or 11 and BITSYNCAGC Q) - Continued.

Symptom	Corrective action	Notes
DATA 1 indicator illuminated or remaining indicator not illuminated	Replace	
	a A2A29	B/S buffer (SM-D-877695)
	b A3A7	Decoder switch (SM-D-877700)
	c A3A9	PN sequence generator (SM-D-742057)

Table 3-25. Fault Isolation Procedure (ERROR COUNT 12).

Symptom	Corrective action	Notes
Meter reading out of limits	Replace	
	a A2A4*	Phase quantizer (SM-D-731213).
	b A2A5*	Phase dump (SM-D-731209)
	c A2A6*	Phase integrator (SM-D-731205)
	d. A2A31*	Timing and AGC (SM-D-731229/877930).
DATA or CLOCK indicator extinguished	Replace.	
	a A2A29	B/S buffer (SM-D-877695)
	b A3A7	Decoder switch (SM-D-877700)
	c A3A9	PN sequence generator (SM-D-742057)

Table 3-26. Fault Isolation Procedure (SIG/NOISE).

Symptom	Corrective action	Notes
DATA 1 or 0 extinguished or meter other than 0	Replace.	
	a. A2A8*	I channel data quantizer (SM-D-731213)
	b A2A32*	Q channel data quantizer (SM-D-731213)
	c A2A10*	I channel data integrator (SM-D-731205)
	d A2A34*	Q channel data integrator (SM-D-731205)
	e A2A31*	Timing and AGC (SM-D-731229/877930).
	f A2A30*	Timing and AGC (SM-D-731229/877930).
	g A2A29	B/S buffer (SM-D-877695)
	h A3A7	Decoder switch (SM-D-877700).
	i. A3A11	D/A meter (SM-D-877725)

Table 3-27. Fault Isolation Procedure (XMITRA TE).

Symptom	Corrective action	Notes
Meter indication not within limits or any ALARM or FAULT light illuminated.	Replace	
	a A3A35	Transmit bit detector (SM-D-742045)
	b A3A36	Loop filter (SM-D-731221)
	c A3A37	D/A converter (SM-D-731217)

Table 3-27. Fault Isolation Procedure (XMITRA TE)-Continued.

Symptom	Corrective action	Notes
	d A3A45	15-MHz amplifier (SM−D−742121)
	e A3A46	Mixer/output amplifier (SM−D−742125)
	f A3A43	Reference oscillator (SM−D−742129)
	g A3A42	Reference divider (SM−D−742133)
	h Y2*	VCO, receive (SM−A−731369-1)

Table 3-28. Fault isolation Procedure (RCVRA TE).

Symptom	Corrective action	Notes
Meter indication not within limits	Replace	
	a. A3A13	Phase and loss of lock detector (SM−D−731225/877926).
	b A3A14	Loop filter (SM−D−731221)
	c A3A15	D/A converter (SM−D−731217)
	d. A3A21	15-MHz amplifier (SM−D−742121)
	e A3A22*	Mixer/output amplifier (SM−D−742125)
	f A3A19	Reference oscillator (SM−D−742129)
	g A3A18	Reference divider
	h Y1*	VCO, transmit (SM−A−731369−1)

Table 3-29. Fault Isolation Procedure (Monetary ALARM RESET).

Symptom	Corrective action	Notes
RECEIVE PWR FAULT illuminated or flashing	Replace	
	a. A2A19*	Coherent detector and AGC loop (SM−D−877665)
RECEIVE PH LOCK FAULT illuminated or flashing	Replace	
	a. A2A24*	PLL ampl and sweep generator (SM−D−877670)
	b A2A19*	Coherent detector and AGC loop (SM−D−877665)
RECEIVE BIT SYNC FAULT illuminated or flashing	Replace	
	a. A3A13	Phase and LOL detector (SM−D−731225/877926).

Table 3-30. Fault Isolation Procedure (Coder/Decoder Test).

Symptom	Corrective action	Notes
Any improper indication (external error coding)	Replace	
	a. A3A27**	Encoder interface (SM−D−742049)
	b A3A28**	Decoder interface (SM−D−742029)
	c A3A7	Decoder switch (SM−D−877700)

Table 3-31. Alinement and Adjustment Following Repair Action.

Subassembly	Full alinement procedure	Abbreviated alinemen procedure
A2AI (data receiver and modulator)	Perform the modulator output power adjustment (para 3-16) NOTE This adjustment may be postponed if the modem is required in service immediately	
A2A 2 (70-YH crystal oscillator)	Perform the modulator output power adjustment (para 3-16) NOTE This adjustment may be postponed if the modem is required in service immediately	
A2A4 (phase quantiuer)	Perform steps a b, bon through bv of the receive bit synchronizer alinement, paragraph 3-22 NOTE If the modem is required in service immediately, the above alinement may be postponed However, if the alinement is postponed, the on-line receive bit synchronizer alinement, paragraph 3-23, must be performed if the operational RECEIVE I CHANNEL SYMBOL RATE is 1 3 Mb/s or higher	
A.AS (phase dump circuit)	Perform steps a, b, am, ar through av, bc, bf through bh, and bm through cd of the receive bit synchronizer alinement paragraph 3-22 NOTE If the modem is required in service immediately, the above alinement may be postponed However, if the alinement is postponed, on-line receive bit synchronizer alinement, paragraph 3-23, must be performed if the operational RECEIVE I CHANNEL SYMBOL RATE is 1.3 Mb/s or higher	
A2A6 (phase integrator)	Perform steps a, b, am, ar through av, be, bf through bh, and bm through cd of the receive bit synchronizer alinement, paragraph 3-22 NOTE If the modem is required in service immediately, the above alinement may be postponed However, if the alinement is postponed, the on-line receive bit synchronizer alinement, paragraph 3-23, must be performed if the operational RECEIVE I CHANNEL SYMBOL RATE is 1.3 Mb/s or higher	Paragraph 3-26
A2A8 alinement, paragraph 3-22	Perform steps a, b, bm through bv of the receive bit synchronizer NOTE If the modem is required in service immediately, the above alinement may be postponed However, if the alinement is postponed, the on-line receive bit synchronizer alinement, paragraph 3-23, must be performed if the operational RECEIVE I CHANNEL SYMBOL RATE is 1 3 Mb/s or higher	
A2A9 (data dump circuit)	Perform steps a, b, bm, through bu of the receive bit synchronizer alinement, paragraph 3-22 NOTE If the modem is required in service immediately, the above alinement may be postponed However, if the alinement is postponed, the on-line receive bit synchronizer alinement, paragraph 3-23, must be performed if the operational RECEIVE I CHANNEL SYMBOL RATE is 1 3 Mb/s or higher	

Table 3-31. Alinement and Adjustment Following Repair Action--Continued.

Subassembly	Full alinement procedure	Abbreviated alinemen procedure
A2A10 (data integrator)	Perform steps a, b, am, through aq, be through be, and bm through cd of the receive bit synchronizer alinement, paragraph 3-22. NOTE If the modem is required In service immediately, the above alinement may be postponed. However, if the alinement is postponed, the on-line receive bit synchronizer alinement, paragraph 3-23, must be performed if the operational RECEIVE I CHANNEL SYMBOL RATE is 1 3 Mb/s or higher.	
A2A12 (data detector and driver)		Paragraph 3-28
A2A14 (phase compensatory/detector driver).	Perform the demodulator phase adjustment(para 3-21)	Paragraph 3-29.
A2A16 (70MHz gain control amplifier)	Perform the demodulator A GC level adjustment (para 3-17) NOTE These adjustments may be postponed if the modem is required in service immediately provided the AGC meter reading on the self-test following the repair is within the limits of the self-test.	Paragraph 3-30
A2A18 (filters and distribution amplifier).	Perform the demodulator phase adjustment (para 3-21)	Paragraph 3-29.
A2A19 (coherent detector and AGC loop amp).	Perform the demodulator AGC level adjustment (para 3-17) and then the demodulator acquisition threshold adjustment (para 3-19) NOTE If the modem is required for service immediately, perform the abbreviated demodulator AGC adjustment (para 3-27) and the abbreviated demodulator acquisition threshold adjustment (para 3-29), and then the Eb/No test (para 3-38) If the Eb/No test is within tolerance, return the modem to service; and then perform the demodulator AGC level adjustment (para 3-17) and the demodulator acquisition threshold adjustment (para 3-19) as soon as practicable If the Eb/No is not within tolerance, perform paragraphs 3-17 and 3-19 immedlately.	Paragraph 3-31.
A2A20 (X2/X4 multiplier)	Perform the demodulator AGC level adjustment (para 3-17) and then the post-multiplier AGC level adjustment (para 3-18)	Paragraph 3-32
A2A22 (reference oscillator and X2 multiplier)	Perform the demodulator phase adjustment procedure (para 3-21) NOTE This adjustment may be postponed if the modem is required in service immediately However, demodulator performance may be degraded	Paragraph 3-29.
A2A24 (PLL and sweep circuit)	a. If phase lock does not occur, perform paragraph 3-19 first and then 3-21 b. If phase lock does occur, perform paragraph 3-21 or abbreviated alinement (para 3-38).	Paragraph 3-33.
A2A26 (modulation filter).	Perform the modulator output power adjustment (para 3-16) NOTE This adjustment may be postponed if the modem is required in service immediately	
A2A27 (70-MHz output amplifier).	Perform the modulator output power adjustment (para 3-16) NOTE This adjustment may be postponed if the modem is required in service immediately	

Table 3-31. Alinement and Adjustment Following Repair Action--Continued.

Subassembly	Full alinement procedure	Abbreviated alinemen procedure
A2A30 (timing and AGC)	Perform steps a, b, f, through i, bq, br, bv, bi, by, bx, cc, and ed of th receive bit synchronizer alinement, paragraph 3-22 NOTE If the modem is required for service immediately, the above alinement may be shortened. To return to service, perform only steps a, b, and f through i of the receive bit synchronizer alinement, paragraph 3-22; and the on-line receive bit synchronizer alinenment, paragraph 3-28, if the operational RECEIVE I CHANNEL SYMBOL RATE is 1.3 Mb/s or higher. The complete alinement can be performed later.	Paragraph 3-34.
A2A31 (timing and AGC)	Perform steps a through e, ak and bm through cd of the receive bit synchronizer alinement, paragraph 3-22. NOTE If the modem is required for service immediately, the above alinement may be shortened. To return to serve, perform only steps a through e of the receive bit synchro niser alinement, paragraph	Paragraph 3-34.
line receive	bit synchronizer & alinement, paragraph 3-22, if the operational RECEIVE I CHANNEL SYMBOL RATE is 1.3 Mb/s or higher. The complete alinement can be performed later.	3-22, and the on-
A2A32 (data quantiser)	Perform stepsb, bin through bu of the receive bit synchronizer alinement, paragraph 3-22. NOTE If the modem is required in service immediately, the above alinement may be postponed. However, if the alinement is postponed, the on-line receive bit synhroniser alinement, paragraph 3-28, must be performed if the operational RECEIVE I CHANNEL SYMBOL RATE is 1.o Mb/s or higher.	
A2A34 (data integrator)	Perform steps a, b, am, ar through av, bc, bf th through bh, bq, br, ov, bw, by, b, cc, and Cd of the receive bit synchronizer alinement, paragraph 3-22. NOTE If the modem is required in service immediately, the above alinement may be postponed. However, if the alinement is postponed, the on-line receive bit synchroniser alinement, paragraph 3-28, must be performed if the operational RECEIVE I CHANNEL SYMBOL RATE is 1.3 Mb/s or higher.	Paragraph 3-28
AU2A (data detector and driver).		Paragraph 3-28
A2A47 (acquisition control).	Perform the AGC window adjustment, paragraph 3-20.	
A3A2 (LOS/cable receiver and decoder)	Perform the LOS/cable receiver alinement. See Operation and Organizational Maintenance Manual, TM 11-5820-847-12, chapter 2, circuit lineup paragraph.	
A8A6 (encoder switch)	Perform the coder switch timing alinement (para 3-24).	
A3A22 (receiver mixer/output amplifier)	Perform steps j through m and y of the receive frequency synthesizer alinement (para 3-15).	
A3A24 (receiver 45-MHz phase lock loop).	Perform the receive frequency synthesizer alinement (para 3-15).	
AA39S (stable clock)	Perform the stable dock adjustment (para 3-18)	Paragraph 3-36.
Y1 (oscillator).	Perform the oscillator adjustment (para 3-14 and 3-15).	
Y2 (oscillator)	Perform the oscillator adjustment (para 3-14 and 3-15).	

b. Perform the corrective actions in the sequence given, and monitor the unit to determine whether the corrective action clears the fault. For example, if the corrective action column lists several potentially faulty PC cards, replace the first card listed. If the fault indication status of the modem remains unchanged, return the original card to the modem, and then replace the second card on the list. Continue in this sequence until the fault is cleared.

c. When a corrective action is performed that apparently clears the faulty indication, confirm the repair by rerunning the self-test procedure (para 3-8).

d. The replacement of several cards of the modem requires that alinement or adjustment be performed. The specific procedures for alinement and adjustment of these cards (which are indicated by an asterisk (*) in table 3-6 corrective action column) are referenced from table 3-31. When alinement is required, proceed as follows:

(1) Rerun self-test.

(2) Perform Eb/No test at the operational data rate only (para 3-38). If error rate is within tolqrance (fig. 3-20), return the modem to service. If error rate Is not within tolerance (fig. 3-20), proceed to (8) below.

(3) Perform the abbreviated alinement procedure (if one exits), see table 3-31 for paragraph reference, Then perform the E_b/N_o test at the operational data 47-34/NAVELEX 0969-LP169-5020/TO 31 R5 -2G-282 rate. If the error rate is within tolerance, return to the self-test. If the error rate is not within tolerance, or if abbreviated alinement procedure does not exist, perform the full alinement, see table 3-31 for paragraph reference.

e. If any card that contains switches is replaced, the switches on the replacement card must be set properly to interface with the system. The cards that contain switches are indicated in the corrective action columns by double asterisks (**). Set the switches on the replacement cards the same as the switches on the card being removed.

f. For procedures to replace parts in the modem, refer to paragraph 3-37.

3-10. Chassis and Card File Fault Isolation

a. General This paragraph contains the fault isolation information for QPSK/BPSK modem components that are not plug-in replaceable.

b. Card Files. If the fault is not corrected by the substitution method of troubleshooting, continuity checks between connectors must be made. Refer to QPSK connection diagram, figure FO-56 and perform continuity tests in the suspect area.

c. Chassis Wiring. Continuity tests are made between external connector and points in the modem or between internal points within the modem. Refer to QPSK connection. diagram, figure FO-56, Table 3-32 gives a list and description of the connectors.

Table 3-32. QPS/BPSK Modem Connectors.

Designation	Type	Description
A1J01	External	ERROR test point.
A1JO2	External	SYNC test point.
A1JO0	External	DATA test point.
A1JO4	External	CLOCK test point.
A2J04	External	Ac power from the rack.
A2J05	External	Digital user interface with modem.
A2J06	External	Coder/decoder interface with modem.
A2ATL11	External	70-MHz output.
A2AlT21	External	70-MHz input.
A2E02	External	Static ground
A2E05	External	Single-point ground.
A2CP1	External	LOS input
A1P01/A4J01	Internal	Ac power.1
A1P02/A3J02	Internal	Connects coder/decoder to bottom card flies.
A1P08/A3J08	Internal	Connects standard inputs and outputs to bottom card files.
A1P04/A3J04	Internal	Connects RECEIVE I CHANNEL SYM-BOL RATE switch to bottom card files.
A1P05/A3J05	Internal	Connects TRANSMIT INPUT DATA RATE switch to bottom card files.
A1P05/A3J07	Internal	Connects front panel lights, switches, and meter to bottom card files.
A1P06/A2J02	Internal	Connects front panel lights and switches to top card files
A4P01/A2J07	Internal	Dc power to card files
A4P02/A3J09	Internal	Dc power to card files.
A1W01P1/A2J1	Internal	
A2W01P2/A3J6	Internal	Connects top and bottom card files

Table 3-32. QPS/BPSK Modem Connectors.

Designation	Type	Description
A1W02P1/A2J6	Internal	
A1W02P2/A3Jl1	Internal	
A1WO4POl/AlKl-eom	Internal (semi-rigid)	
A1W04PO2/A2W02JO1	Internal (semi-rigid)	
A1W05POl/A1K1-NC	Internal (semi-rigid)	
A1W05PO2/AlAT2J2	Internal (semi-rigid)	RF lines for internal 70- MHz distribution.
A1W06PO1/AlK1-NO	Internal (semi-rigid)	
A1W06P02/A2ATU1	Internal (semi-rigid)	
AlW07POl/A2WO4J1O	Internal (semi-rigid)	
AlW07P02/AlW08 J1	Internal (semi-rigid)	
A1WO8POl/A1ATLU2	Internal (semi-rigid)	
AlW09-1/A2WOl-1	Internal	Ground returns.
A1WO9-2/AEOS- B	Internal	Ground returns.
AlW10- 1/A3WO1-1	Internal	Ground returns.
A1W10-2/AlE0-6	Internal	Ground returns.
AlWllP01/A3J8	Internal	Oscillator cable.
AlWIIP02/AlY1J1	Internal	Oscillator cable.
A1WlPO/A1Y2J1	Internal	Oscillator cable.

d. Front and Rear Panel Components. Refer to paragraph 3-37 for defective parts replacement procedures.

(1) *Indicators. Test by replacing.* If replacement does not correct the problem, make voltage and continuity tests.

(2) *Switches.* Remove leads and make continuity tests with switch in different positions.

(3) *Blowers*. Test for 115 V ac between terminals E7 and E8. If voltage is present but blowers do not operate, replace blower assembly. If voltage is not present, make continuity tests to locate open circuit.

(4) *ALARM buzzer.* Test for +5 V dc at positive lead on buzzer. If +5 V dc is present, short negative lead to ground. If buzzer does not then operate, replace bazaar. If the buzzer operates, check associated wiring or replace alarm circuit card A3A12.

(5) *Thumbwheel switch subassembly.* Place the switch in each dial position and make continuity test from the common terminals to the output terminals (see table 3-33).

(6) *Front panel MONIMTOR meter.* Disconnect wires. With MONITOR meter switch in DC PWR position, verify continuity to ground at wire connected to terminal, and verify a voltage of 0.8 +0.1 volt dc at wire connected to + terminal. If readings are correct, replace meter.

Table 3-33. Thumbwheel Switch, Truth Table.

Switch S1					Switches S2 through S5				
Dial reading	Common X (●), Y(○) connected to terminal				Dial reading	Common X (●), Y(○) connected to terminal			
	1	2	3	4		1	2	3	4
1	○	○	○	●	0	●	○	○	●
2	●	●	●	○	1	○	○	○	●
3	○	●	●	○	2	●	●	●	○
4	●	○	●	○	3	○	●	●	○
5	○	○	●	○	4	●	○	●	○
6	●	●	○	○	5	○	○	●	○
7	○	●	○	○	6	●	●	○	○
8	●	○	○	○	7	○	●	○	○
9	○	○	○	○	8	●	○	○	○
					9	○	○	○	○

Switch S6		
Dial reading	Common A, B connected to terminal	
	A	B
KB/SXX.XXX	A0	B0
KB/SXXX.XX	A1	B1
MB/SX XXXX	A2	B2

Section III. MODEM ALINEMENT AND REPAIR

3-11. Adjustment and Alinement Procedures

a. The procedures required to adjust the modulator, demodulator, and receive bit synchronizer to obtain optimum performance are contained in this section

NOTE

Ensure that the RANDOMIZER TRAN SMIT and RECEIVE switches located behind the front panel are set to the OFF position when performing ahnement procedures.

b. Figure 3-1 shows the location of the pins on typical cards.

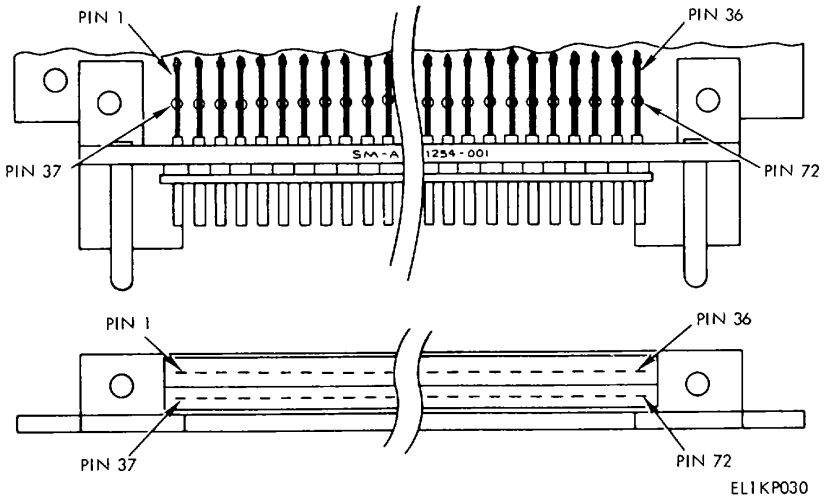


Figure 3-1. Typical card pin locations.

c. DATA RATE thumbwheel switch settings for the modem test set differ from those used on the QPSK/BPSK modem. When using the modem test set, refer to Operator's and Organizational Maintenance Manual for Test Set, Modem TS-3580/G (TM 11-6625-2772-12) for the corresponding settings on the modem test set.

CAUTION

Use only nonmetalic alinement tools. Never operate the QPSK/BPSK modem for more than 15 minutes with the cover removed unless external cooling air is applied to the power supply

3-12. Power Supply Adjustment

A digital voltmeter (DVM) is required for this adjustment. Use the DVM to motor the voltage test points on the bottom of the power supply. Ground of the DVM must be connected to the modem chassis Removal of the bottom cover is necessary, therefore, the blower adapter must be attached and running while making adjustments Ensure each power supply voltage is within hrmts as stated in table 3-34, if not, adjust as required The voltage adjustment controls are located on the bottom of the power supply and are clearly marked to indicate the voltage controlled by the adjusting control. It should be noted that if a voltage is adjusted to bring it within the stated limits, it may or may not affect other sections of the modem so as to require realinement of the particular section or card

Table 3-34. Power Supply Measurements

Voltage	*Limits*
+ 5 Vdc	+495to+505Vdc
-5Vdc	-4 95to-5 05Vdc
+15Vdc	+1498to+1502Vdc
-15Vdc	-1498to-1502Vdc

3-13. Stable Clock Adjustment

A frequency counter, an oscilloscope, a digital voltmeter, two card extenders (759649), and a card puller (7920) are required for this adjustment.

NOTE

If any adjustment fails to provide the specified result, the probable cause is a failure of the card being adjusted If the measurement is taken from a card other

than the one being adjusted, the next most probable cause is a failure of the card from which the measurement is taken.

a. Set the front panel MODE switch to TEST position.

b. Remove the transmit reference oscillator card, A3A43, and place it on a card extender. Also, remove the transmit 45 MHz amplifier card, A3A47, and place it on a card extender.

c. Before returning A3A43 and card extender to the modem, connect a frequency counter to pin 21 of the transmit reference oscillator card, A3A43. Return both cards and card extenders to the modem.

CAUTION

Remove the card from the card extender in order to remove the screw cap on oscillator Y 1

d. If required, adjust the 15 MHz TXCO, Y1, on the transmit reference oscillator card (fig. 3-2) for a frequency counter indication of 15 MH +2 Hz.

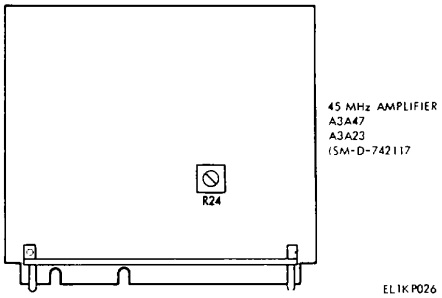


Figure 3-2. Reference oscillator adjustment locations

e. Set the front panel TRANSMIT INPUT DATA RATE thumbwheel switches to 9.9999 MB/S.

f. Connect an oscilloscope to monitor the signal amplitude at pin 22 of the transmit 45 MHz amplifier card, A3A47. Synchronize the oscilloscope internally.

g. While monitoring the amplitude at pin 22, change the TRANSMIT INPUT DATA RATE thumbwheel switches to 5 0000 MB/S.

h. Signal amplitude at pin 22 should be between 1 and 2 V p-p. As required, adjust R24 on the transmit 45 MHz amplfier card, A3A47 (fig. 3-3 to peak the signal amplitude as close to 2 V p-p as possible, at a data rate of 5.0000 MB/S. On some modems, it may be possible to obtain an amplitude greater than 2 V pp. On these modems, ensure that the signal is not adjusted for a value greater than 2 V p-p.

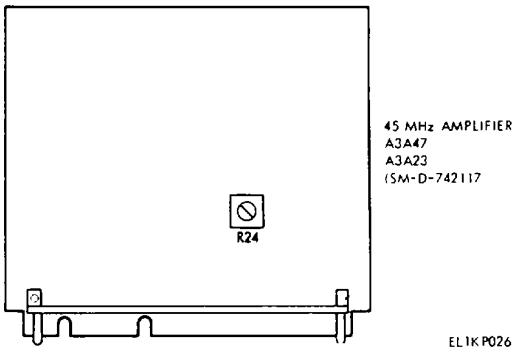


Figure 3-3. 45MHz amplifier adjustment location

i. Remove both card extenders. Return the circuit cards to their proper positions in the file. Place transmit 45 MHz phase lock loop card, A3A48, and the stable clock card, A3A39, on card extenders.

j. Connect an oscilloscope to monitor the waveform at pin 8 of the stable clock card, A3A39. Set TRANSMIT INPUT DATA RATE thumbwheel switches to 9.9999 MB/S.

k. As required, adjust R37 on the stable clock card, A3A39 (fig 3-4) to obtain the best possible symmetrical waveform.

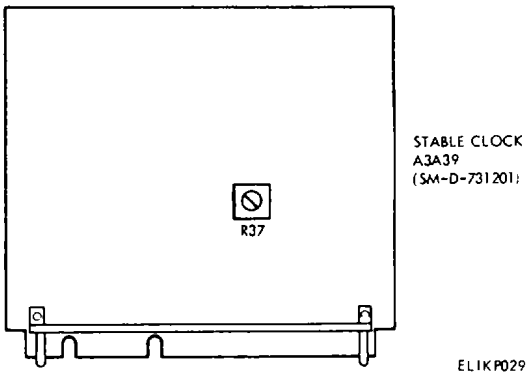


Figure 3-4. Stable clock adjustment location

l. Set TRANSMIT INPUT DATA RATE thumbwheel switches to 7.5000 MB/S.

m. Connect digital voltmeter to point A on the transmit 45 MHz phase lock loop card, A3A48, as shown in figure 3-5. If the required, adjust oscillator Y1 on A3A48 to obtain of 0O_0.1 V dc.

n. On the MONITOR section of the front panel, set the meter switch to the XMIT SYNTH position.

o. On the transmit 45 MHz phase lock loop card, A3A48, adjust R12 (fig. 3-5) to obtain a front panel MONITOR meter indication of 50+ 2.

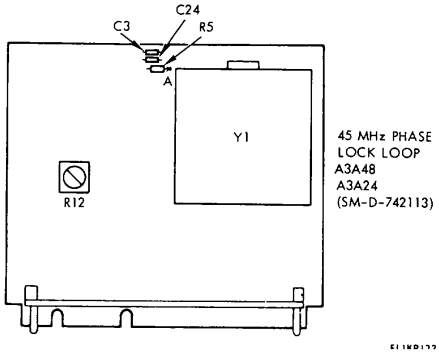


Figure 3-5. 45MHz phase lock loop adjustment

p. Remove the card extenders. Return the trans mit 45 MHz phase lock loop card, A3A48, and stable clock card, A3A39, to their proper position, in the card file.

q. Set the MONITOR ERROR COUNT thumb wheel switch to position 1 and monitor the front panel TEST OUTPUTS CLOCK output with E frequency counter. Exercise the TRANSMIT IN PUT DATA RATE switches through each position and verify that the counter indicates the selected frequency ± 1 least significant digit.

r. If the selected frequency cannot be obtained within a t 1 least significant digit, repeat the stable clock adjustment (a through o above.)

3-14. Transmit Frequency Synthesizer Alinement

A frequency counter, an oscilloscope, two card extenders (759649), and a card puller (7920 are required for this adjustment.

NOTE

If any adjustment fails to provide the specific result, the probable cause is a failure of the card being tested. If the measurement is taken from another card, the next most probable cause is a failure of the card from which the measurement is taken.

a. Set the front panel MODE switch to TEST position.

b. Place the transmit reference oscillator card, A3A43, and the mixer/output amplifier card, A3A46, on card extenders.

c. Set the TRANSMIT INPUT DATA RATE thumbwheel switches to 9.9999 MB/S.

d. Connect an oscilloscope to pin 14 on the transmit reference oscillator card, A3A43. Adjust R33 (fig. 3-6) on the mixer/output amplifier card, A3A46, to obtain the cleanest waveform possible. Oscilloscope must be triggered on internal source.

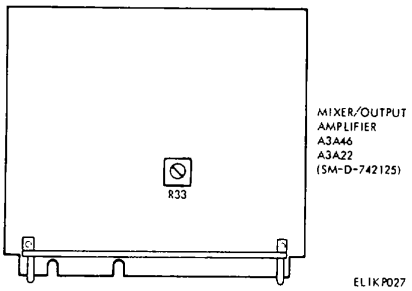


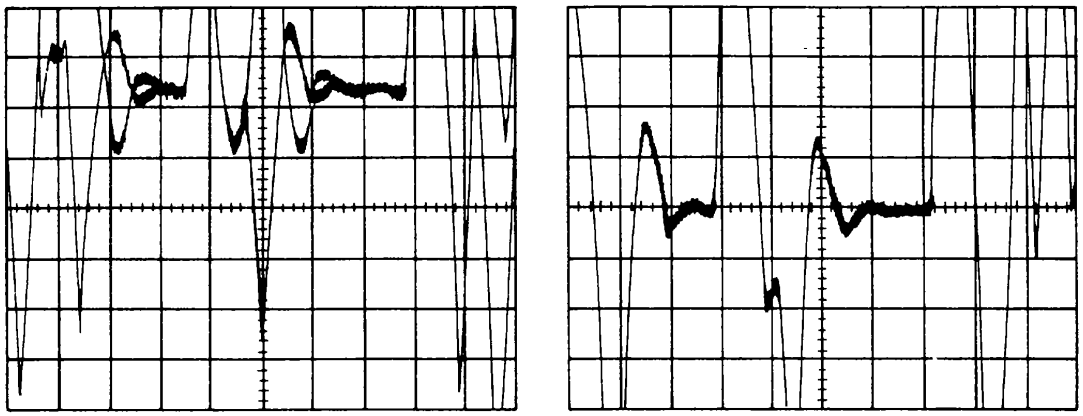
Figure 3-6. Mixer/output amplifier adjustment location

e. Set TRANSMIT INPUT DATA RATE thumbwheel switches to 5.0100 MB/S and observe the waveform. Readjust R33 on A3A46, if necessary, for cleanest waveform possible at both data rates (9.9999 MB/S and 5.0100 MB/S).

f. Remove card extenders. Return the transmit reference oscillator card, A3A43, and the transmit mixer/output amplifier card, A3A46, to the proper positions in the card file.

g. Place the transmit 15 MHz amplifier card, A3A45 on an extender.

h. Connect oscilloscope to pin 21 of the transmit 15 MHz amplifier, A3A45. Vertical coupling switch of oscilloscope must be in dc position, 20 MHz bandwidth (BW) and externally synchronized to front panel synchromzatlon jack. Adjust Y2 (fig. 3-22 or 3-22.1)as required to obtain a reading of 0 +0.05 V dc. Proper adjustment will give an oscilloscope presentation similar to that shown in figure 3-6.1 presentation B, whereas improper adjustment may be similar to presentation A.



PRESENTATION A PRESENTATION B

NOTE: Ground reference must be centered on scope to obtain proper readings
Vertical = lOO1mV per division Horizontal = 500ms per division

EL1 KP133

Figure 3-6.1. Transmit frequency synthesizer adjustment waveforms.

t. Remove the card extender and return the transmit 15 MHz amplifier card, A3A45, to its proper position In the card file. Return the oscilloscope from 20 MHz to the full bandwidth (BW) position

j. Upon completing this alinement, connect a frequency counter to the front panel TEST OUTPUTS CLOCK output and set the MONITOR ERROR COUNT thumbwheel switch to position 2 Exercise the TRANSMIT INPUT DATA RATE thumbwheel switches through each position and verify that the counter indicates the selected frequency + 1 least significant digit.

k. If the selected frequency cannot be obtained within a ± 1 least significant digit, repeat transmit frequency synthesizer alinement (a through j above).

3-15. Receive Frequency Synthesizer Alinement

A frequency counter, an oscilloscope, a digital voltmeter, two card extenders (759649), and a card puller (7920) are required for this adjustment.

NOTE

If an adjustment fails to provide the specified result, the probable cause is a failure of the card being adjusted. If the measurement is taken from another card, the next most probable cause is a failure of the card from which the measurement is taken.

a. Set the front panel MODE switch to the TEST position.

b. Place the receive reference oscillator card, A3A19, on a card extender. Also place the receive 45 MHz amplifier card, A3A23, on a card extender.

c. Set both the TRANSMIT QPSK/BPSK and the RECEIVE QPSK/BPSK switches to the BPSK positions

d. Set the MONITOR ERROR COUNT thumbwheel switch to position 3.

e. Set the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 9.9999 MB/S.

f. Connect a frequency counter to pin 21 of the receive reference oscillator, A3A19. As required, adjust the 15 MHz TCXO, Y1 on the receive reference oscillator card, A3A19 (fig. 3-2) for a frequency counter indication of 15 MHz +2 Hz.

g. Connect an oscilloscope to monitor the signal amplitude at pin 22 of the receiver 45 MHz amplifier card, A3A23 While monitoring the amplitude at pin 22, change the setting of both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 5 0000 MB/S.

h. The amplitude of the signal at pin 22 on the receiver 45 MHz amplifier card, A3A23, should be 2 +o 1 V p-p. If necessary, adjust R24 (fig. 3-3) to obtain the best indication as close to 2 V p-p as possible at pin 22.

i. Set TRANSMIT INPUT DATA RATE and RECEIVE I CHANNEL SYMBOL RATE thumb wheel switches to 9 9999 MB/S. Return the 45 MHz

amplifier card, A3A23, to the proper position in the card file, and place the mixer/output amplifier card, A3A22, on the card extender.

j. Connect an oscilloscope to monitor the signal at pin 14 on the receive reference oscillator, card A3A19.

k. Observe the signal on the oscilloscope, and adjust R33 (fig. 3-6) on the mixer/output amplifier card (A3A22) for the cleanest waveform possible. Oscilloscope must be triggered on internal source.

I. Set TRANSMIT INPUT DATA RATE and RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 5.0100 MB/S and observe the waveform. Adjust R33 on A3A22, if required, for the cleanest waveform possible at both data rates (9.9999 MB/S and 5 0100 MB/S).

m. Remove both card extenders. Return the circuit cards to their proper positions in the card file.

n. Place the receive 45 MHz phase lock loop card, A3A24, on a card extender

o. Set TRANSMIT INPUT DATA RATE and RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 7.5000 MB/S.

p. Connect digital voltmeter to exact point A on resistor on the receive 45 MHz phase lock loop card, A3A24, as shown in figure 3-5.

q. If required, adjust oscillator Y1 on A3A24 to obtain a reading of O +0.1 V dc.

r. On the monitor section of the front panel, set the meter switch to the RCVR SYNTH position.

s. On the receive 45 MHz phase lock loop card, A3A24, adjust R12 (fig. 3-5) to obtain a front panel MONITOR meter indication of 50 ± 2

t. Remove card extender Return the receive 45 MHz phase lock loop card, A3A24, to its proper position in the card file.

u. Place the receive 15 MHz amplifier card, A3A21, on the extender

v. Connect an oscilloscope to pin 21 of the receiver 15 MHz amplifier, A3A21 Channel of oscilloscope must be in dc position, 20 MHz BW, and externally synchronized to front panel synchronization jack. Adjust Y1 (fig. 3-22 or 3-22 1) as required to obtain a dc offset of 0 +0.05 V dc. Proper adjustment will give an oscilloscope presentation similar to that shown in presentation B, whereas improper adjustment may be similar to presentation A (fig. 3-6.1).

NOTE

Ground reference must be centered on oscilloscope to obtain proper readings.

w. Remove the card extender and return the receive 15 MHz amplifier, A3A21, to its proper position in the card file. Return oscilloscope from 20 MHz to the full bandwidth (BW LIMIT) position.

x. Connect a frequency counter to the TEST OUTPUTS CLOCK output on the front panel.

y. With the MONITOR ERROR COUNT thumbwheel switch in position 3, exercise both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches through each position at the same time and verify that the counter indicates the selected frequency + 1 least significant digit.

z. If the selected frequency cannot be obtained within a 71 least significant digit, repeat receive synthesizer alinement (a through y above).

3-16. Modulator Output Power Adjustment

A power meter (MV-828A), a card extender (759649), a card puller (7920), and a modem test set are required for this adjustment.

NOTE

If output power cannot be adjusted to +10.5 dBm, set the TRANSMIT INPUT DATA RATE thumbwheel switches to a different modulator data rate range (para 3-39) If the specified output is obtained at a different rate, the probable cause is a failure of the modulation filter card. A2A26, or the relay control card, A3A32. If the specified output cannot be obtained at another odulator data rate rarge, the probable cause is a failure of the 70 MHz output amplifier card, A2A27, the 70 MHz crystal oscillator card, A2A2, or the QPSK/BPSK data receiver and modulator card, A2A1.

a. Set the QPSK/BPSK modem switches to the normal operational settings. Connect modem transmitter output to input of modem test set at the IF patch rack. Put modem test set in CAL position and read power meter for 0 to - 1 dB.

b. If reading on modem test set is not > 10 dBM, remove the 70 MHz output amplifier card, A2A27, and install a card extender in the card slot. Install the 70 MHz output amplifier card, A2A27, in the card extender.

c. Adjust R28 on A2A27, figure 3-7, to obtain a reading of > 10 dBm on modem test set. Remove card extender and reinstall A2A27.

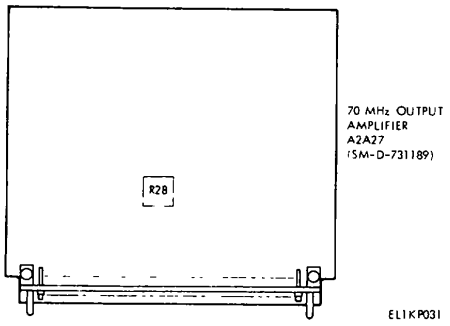


Figure 3-7. Modulator output power adjustment location

d. If this reading cannot be obtained, remove cable connected to AT1Jl on rear of modem and connect a power meter to AT1J1 connector at rear of modem to assure an output of +10.5 dBm +0.5 dB. If 10.5 dBm cannot be obtained, refer to note above for troubleshooting. If 10.5 dBm can be obtained, check entire cable path that connects modem output to modem test set input. If cable path checks out, modem test set may be cause of problem.

e. Remove card extender and reinstall A2A27.

3-17. Demodulator AGC Level Adjustment

Step attenuators HP 355C and HP 355D, and an rf power meter MV-828A are required for this adjustment.

a. Disconnect the external cables connected to ATlJ1 and AT2J1 on the rear panel.

b. Set the QPSK/BPSK modem front panel controls as shown in table 3-35 Set the POWER switch to the ON position.

c. Check the 70 MHz gain controlled amplifier card, A2A16, to determine the setting of switch S1 See positions of switch S1 (fig. 3-26). The remaining steps of this procedure list attenuator settings to be used if switch S1 is in position 1, followed by setting in parenthesis to be used if switch S1 is in position 2.

d. Connect AT1J1 to AT2J1 (on the rear panel) via series-connected HP 355C and HP 355D step attenuators set to provide a total attenuation of 85 dB _ (65 dB).

e. Connect the rf power meter (MV-828A) to TP8 on the X2/X4 multiplier card, A2A20 (A, fig. 3-8).

f. Monitor the rf power meter and adjust Rl18 on the coherent detector and AGC loop amplifier card, A2A19 (B, fig 3-8), to obtain a reading of -31 dBm O+0.2 dB.

Table 3-35. Initial Control Settings for AGC Level Adjustment

Control	Position
ALARM RESET/OFF/ON	OFF
MODE	LINK
TRANSMIT INPUT DATA RATE	16.000 K B/S
TRANSMIT QPSK/BPSK	BPSK
TRANSMIT ENCODER DIFF/OFF	DIFF
TRANSMIT ENCODER EXT/OFF	OFF
RECEIVE I CHANNEL SYM BOL RATE	16 000 K B/S
RECEIVE QPSK/BPSK	BPSK
RECEIVE DECODER DIFF/OFF	DIFF
RECEIVE DECODER EXT/OFF	OFF
MONITOR meter switch	DEMOD AGC
MONITOR ERROR COUNT	0
SWEEP CONTROL NORMAL/WIDE	NORMAL
SWEEP CONTROL FAST/NORMAL	NORMAL
SWEEP CONTROL PARTIAL/FULL	FULL
RANDOMIZER TRANSMIT	OFF
RANDOMIZER RECEIVE	OFF

NOTE

If the specified -31 dBm indication cannot be obtained by adjustment, the probable cause of failure is the 70 MHz gain control amplifier, A2A16, or the filters and distribution card, A2A18. However, the X2/X4 multipler, A2A20, the coherent detector and AGC loop amplifier and sweep circuit, A2A24, could also cause this failure. Refer to the unit fault isolation table 3-13

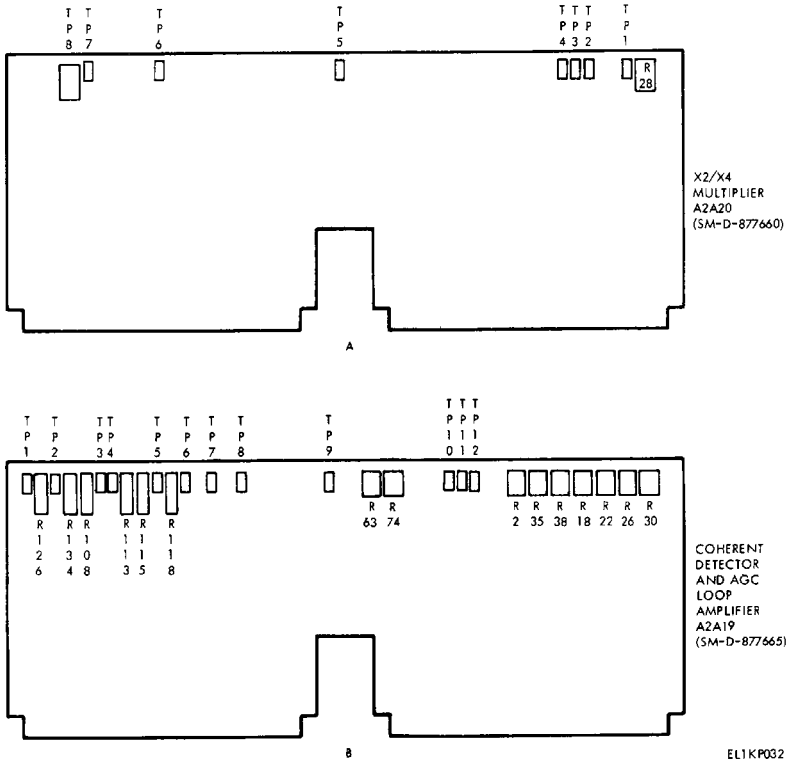


Figure 3-8. X2/X4 multiplier, and coherent detector and AGC loop amplifier, test points and adjustment location.

g. Disconnect the rf power meter from TP8 on the X2/X4 multiplier card, A2A20.

NOTE

If a specified MONITOR meter DEMOD AGC indication or a specified RECEIVE PWR FAULT indication cannot be obtained below, the probable cause is a failure of the coherent detector and AGC loop amplifier card, A2A19.

h. Monitor the front panel MONITOR meter and adjust R134 on the coherent detector and AGC loop amplifier card, A2A19 (B, fig. 3-8), to obtain a reading of 0.

i. Change settings of the two step attenuators to provide a total attenuation of 30 dB (10 dB).

j. Monitor the front panel MONITOR meter and adjust R108 on the coherent detector and AGC loop amplifier card, A2A19 (B, fig. 3-8), to obtain a MONITOR meter reading of 100.

k. Change the setting of the two step attenuators to provide a total attenuation of 87 dB (67 dB)

l. Observe the RECEIVE PWR FAULT indicator on the front panel and adjust R115 on the coherent detector and AGC loop amplifier card, A2A19 (B, fig. 3-8), until the RECEIVE PWR FAULT indicator just extinguishes.

m. Verify that the RECEIVE PWR FAULT indicator flashes when the total attenuation is changed to 92 dB (70 dB) and then extinguishes when the total attenuator setting is changed to 87 dB (68 dB). If not, repeat steps k and I above

n. Set the TRANSMIT INPUT DATA RATE and RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches on the QPSK/BPSK modem front panel for 2.5 MB/S Change attenuators for a total of 66 dB (46 dB).

o. Observe the RECEIVE PWR FAULT indicator on the front panel and adjust R113 on the coherent detector and AGC loop amplifier card, A2A19 (B, fig. 3-8), until the PWR FAULT indicator just extinguishes.

3-18. Post Multiplier AGC Level Adjustment

A digital voltmeter is required for this adjustment.

a. Set the QPSKIBPSK MODEM front panel controls as shown in table 3-36. Set the POWER switch to the ON position.

b. Connect the digital voltmeter to TP 1 on the quadrature detector card, A2A35 (fig. 3-9).

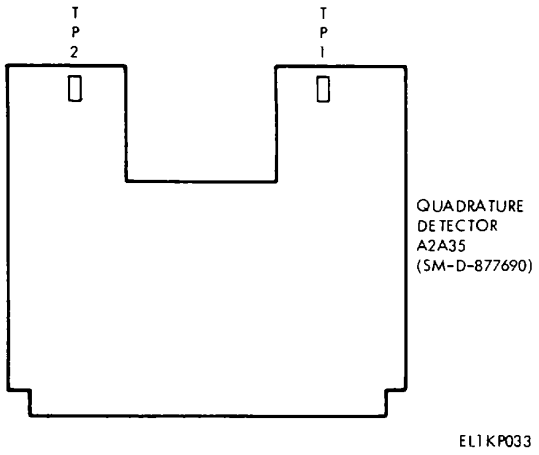


Figure 3-9. Quadrature detector, test point location.

Table 3-36. Initial Control Settings for Post Multiplier AGC Level Adjustment

Control	Position
ALARM RESET/OFF/ON	OFF
MODE	TEST
TRANSMIT INPUT DATA RATE	1 MB/S
TRANSMIT QPSK/BPSK	QPSK
TRANSMIT ENCODER DIFF/OFF	DIFF
TRANSMIT ENCODER EXT/OFF	OFF
RECEIVE I CHANNEL SYMBOL RATE	500 K B/S
RECEIVE QPSK/BPSK	QPSK
RECEIVE DECODER DIFF/OFF	DIFF
RECEIVE DECODER EXT/OFF	OFF
MONITOR meter switch	DEMOD VCXO
MONITOR ERROR COUNT	0
SWEEP CONTROL NORMAL/WIDE	NORMAL
SWEEP CONTROL FAST/NORMAL	NORMAL
SWEEP CONTROL PARTIAL FULL	FULL
RANDOMIZER TRANSMIT	OFF
RANDOMIZER RECEIVE	OFF

c. Monitor the voltmeter and adjust R28 on the X2/X4 multiplier card, A2A20 (A, fig. 3-8) to obtain a voltmeter reading of -0.922 +_0.025 V dc while the demodulator phase lock loop is locked.

NOTE

If the specified indication cannot be obtained, the probable cause is a failure of the X2/X4 multiplier card, A2A20, or the quadrature detector card, A2A35.

d. Disconnect the voltmeter

3-19. Demodulator Acquisition Threshold Adjustment

An oscilloscope, a modem test set, and a digital voltmeter are required for this adjustment.

NOTE

If the specified indication cannot be obtained, the probable cause is a failure of the phase lock loop amplifier and sweep circuit card, A2A24, or the coherent detector and AGC loop amplifier card, A2A19. The filters and distribution amplifier card, A2A18, and the relay control card, A3A32, could also cause thus problem. Refer to fault isolation table 3-14.

a. Set the modem front panel controls as shown in table 3-37.

b. Connect the modem test set output to the modem input (AT2J1) and modem test set input to the modem output (AT1J 1).

c. Adjust the modem test set for an Be/No of 1 dB at a data rate of 50 KB/S, and disconnect the input to the modem test set

d. Place channel 1 of oscilloscope to TP10 on A2A19 (B, fig 3-8) Switch channel 1 to 20 MHz BW.

e. Initiate full sweep (FULL SWEEP INITIATE may be pushed to establish first sweep cycle). At beginning of second sweep, as indicated by rise to approximately 60 on the front panel MONITOR meter, adjust R18 counterclockwise on A2A19, to obtain a false lock indication at TP10 of a voltage of more negative than - 10 volts on the oscilloscope.

Table 3-37. Initial Control Settings for Acquisition Threshold Adjustment

Control	Position
ALARM RESET/OFF/ON	OFF
MODE	LINK
TRANSMIT INPUT DATA RATE	50 K B/S
TRANSMIT QPSK/BPSK	QPSK
TRANSMIT ENCODER DIFF/OFF	DIFF
TRANSMIT ENCODER EXT/OFF	OFF
RECEIVE I CHANNEL SYMBOL RATE	25 K B/S
RECEIVE QPSK/BPSK	QPSK
RECEIVE DECODER DIFF/OFF	DIFF
RECEIVE DECODER EXT/OFF	OFF
MONITOR meter switch	DEMOD VCXO
MONITOR ERROR COUNT	0
SWEEP CONTROL NORMAL/WIDE	NORMAL
SWEEP CONTROL FAST/NORMAL	NORMAL
SWEEP CONTROL PARTIAL/FULL	FULL
RANDOMIZER TRANSMIT	OFF
RADOMIZER RECEIVE	OFF

f. Place channel 1 of oscilloscope of TP2 on A2A24 Adjust channel 1 for maximum sensitivity that will display a trace, and adjust R89 on A2A24 (fig 3-10) to assure voltage level does not drift. Monitor voltage level for minimum drift. Replace channel 1 of oscilloscope of TP10 of A2A19.

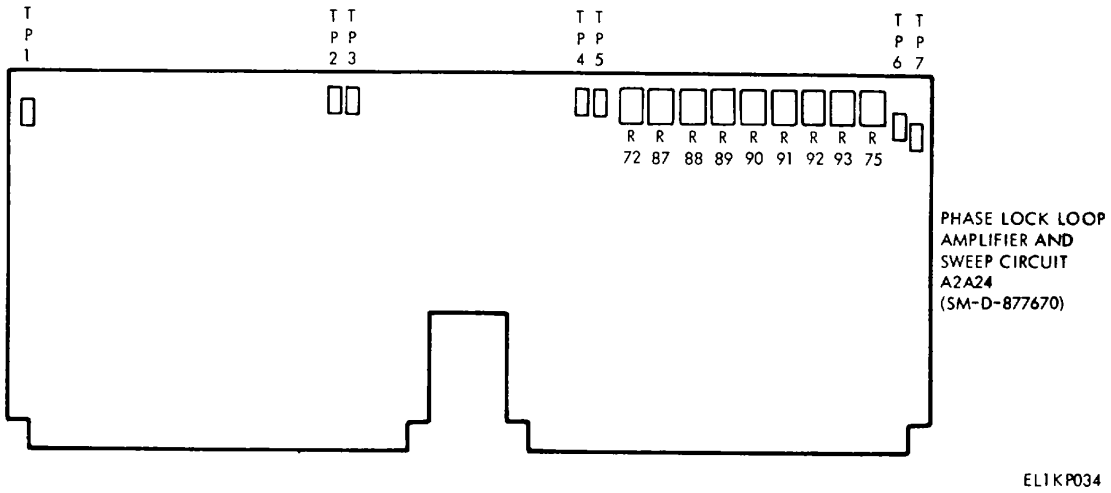


Figure 3-10. Phase lock loop amplifier and sweep circuit, test points and adjustment locations.

g. Connect the modem output (AT1J1) to the input of the modem test set.

h. Connect the digital voltmeter to TP11 on A2A19 Adjust R74 on A2A19 to obtain a reading of -0 6 +0.2 V dc

i. Remove digital voltmeter from TP11

j. Initiate hill sweep With the demodulator in the second sweep cycle, adjust R18 on the coherent detector and AGC loop amplifier card, A2A19 (B, fig. 3-8), to obtain an average reading of + 5 V dc at TP10, using the oscilloscope (modem should lock on second or fourth sweep) Lock state is voltage level more negative than + 10 volts

k. Change the TRANSMIT INPUT DATA RATE from 50 KB/S to 76 KB/S (QPSK) and RECEIVE I CHANNEL SYMBOL RATE from 25 KB/S to 38 KB/S

l. Readjust the signal-to-noise ratio at the demodulator input for an Eb/No of 1 dB at a data rate of 76 KB/S, QPSK.

m. Disconnect the input to the modem test set.

n. After the demodulator has begun Its second cot 1

sweep cycle as indicated by the front panel MONITOR meter, adjust R22 on the coherent detector and AGC loop amplifier card, A2A19 (B, fig. 3-8), to obtain a lock indication at TP10 (voltage more negative than -10 V dc) as monitored on the oscilloscope.

o. Adjust R88 on the PLL amplifier and sweep circuit card, A2A24 (fig. 3-10), to obtain minimum drift in the PLL (as In step f above).

p. Reinsert the signal carrier (by reconnecting the modem test set) at a level so that the resulting Eb/No is 1 dB.

q. With the demodulator in the second sweep cycle, adjust R 22 on the coherent detector and AGC loop amplifier card, A2A19 (B, fig. 3-8). to obtain an average oscilloscope reading of 2.5 V dc at TP10 (modem should lock up on second or fourth sweep, voltage more negative than - 10 V).

r. Change the TRANSMIT INPUT DATA RATE from 76 KB/S to 150 KB/S (QPSK) and RECEIVE I CHANNEL SYMBOL RATE from 38 KB/S to 75 KB/S.

s. Readjust the signal-to-noise ratio at the demodulator input for an Eb/No of 1 dB of a data rate of 150 KB/S, QPSK

t. Disconnect the input to the modem test set.

u. After the demodulator has begun its second sweep cycle, adjust R26 on the coherent detector and AGC loop amplifier card, A2A19 (B, fig 3-8)., to obtain a lock indication at TP10 (voltage more negative than -10 V) as monitored by the oscilloscope.

v. Adjust R87 on the PLL amplifier and sweep circuit card, A2A24 (fig 3-10) to obtain minimum drift in the PLL (as in step for this procedure).

w. Reinsert the carrier signal (by reconnecting the modem test set) at a level so that the resulting Eb/No is 1 dB.

x. With the demodulator in second sweep cycle, adjust R26 on A2A19 (B, fig. 3-8) to obtain an average reading of 2 5 V on the oscilloscope, at TP10 (modem should lock up on second or fourth sweep, voltage more negative than - I O V)

y. Change the TRANSMIT INPUT DATA RATE from 150 KB/S to 300 KB/S and RECEIVE I CHANNEL SYMBOL RATE from 75 KB/S to 150 KB/S.

z. Readjust the signal-to-noise ratio at the demodulator input for an Eb/No of 1 dB at a data rate of 300 KB/S, QPSK.

aa. Disconnect the input to the modem test set.

ab. After the demodulator has begun its second sweep cycle, adjust R30 on A2A19 (B, fig. 3-8), to obtain a lock indication at TP10, (voltage more negative than -10 V) as monitored by the oscilloscope.

ac. Adjust R90 on A2A24 (fig. 3-10) to obtain minimum offset in the PLL (as in step f of this procedure)

ad. Reinsert the carrier signal (by reconnecting the test set) at a level so that the resulting Eb/No is 1 dB.

ae. With the demodulator in the second sweep cycle, adjust R30 on A2A19 (B, fig. 3-8) to obtain an average reading a TTP10 of 2.5 V, az monitored on the oscilloscope (modem should lock upon the second or fourth sweep with a voltage more negative than - 10 V)

af. Change the TRANSMIT INPUT DATA RATE from 300 KB/S to 1 26 MB/S and RECEIVE I CHANNEL SYMBOL RATE from 150 KB/S to 630 KB/S.

ag. Readjust the signal-to-noise ratio at the demodulator input for an Eb/No of 1 dB at a data rate of 1 26 MB/S, QPSK.

ah. Disconnect the input to the modem test set. at After the demodulator has begun its second sweep cycle, adjust R35 on A2A19 (B, fig 3-8) to obtain a lock indication at TP10, as monitored by the oscilloscope (voltage more negative than -10 V).

aj. Adjust R92 on A2A24 (fig. 3-10) to obtain minimum drift in the PLL (as in step f of this procedure)

ak. Reinsert the carrier signal (by reconnecting the test set) at a level so that the resulting Eb/No will be 1 dB.

al. With the demodulator in the second sweep cycle, adjust R35 on A2A19 (B, fig. 3-8) to obtain an average reading, at TP10, of 2 5V, as monitored on the oscilloscope (modem should lock up on the second or fourth sweep with a voltage more negative than -10 V).

am. Change the TRANSMIT INPUT DATA RATE from 1 26 MB/S to 5 MB/S and RECEIVE I CHANNEL SYMBOL RATE from 630 KB/S to 2.5 MB/S

an. Readjust the signal-to-noise ratio at the demodulator input for an Eb/No of 1 dB at a data rate of 5 MB/S, QPSK.

ao. Disconnect the input to the test set

ap. After the demodulator has begun its second sweep cycle, adjust R38 on A2A19 (B, fig 3-8) to obtain a lock indication at TP10 (voltage more negative than -10 V) as monitored by the oscilloscope.

aq. Adjust R91 on A2A24 (fig. 3-10) to obtain minimum drift in the PLL (as in step f.

ar. Reinsert the carrier signal (by reconnecting the test set) at a level so that the resulting Eb/No will be 1 dB

as. With the demodulator in the second sweep

cycle, adjust R38 on A2A19 (B, fig 3-8) to obtain an average reading, at TP10, of 2 5 V, as monitored on the oscilloscope. Modem should lock up on the second or fourth sweep with a voltage more negative than -10 V. (At 5 MB/S, the average level may be near zero).

at. Change the TRANSMIT INPUT DATA RATE from 5 MB/S to 16 KB/S and RECEIVE I CHANNEL SYMBOL RATE from 2.5 MB/S to 16 KB/S Change from QPSK to BPSK operation In the TRANSMIT and RECEIVE sections of the front panel.

au. Readjust the signal-to-noise ratio at the demodulator input for an Eb/No of 1 dB at a data rate of 16 KB/S, BPSK

av. Disconnect the Input to the modem test set

aw After the demodulator has begun its second sweep cycle, adjust R2 on A2A19 (B, fig 3-8) to obtain a minimum voltage at TP10, as monitored by the oscilloscope

ax. Adjust R93 on A2A24 (fig. 3-10) to obtain minimum offset in the PLL as determined by minimum MONITOR meter movement

ay. Reinsert the carrier signal (by reconnecting the test set) at a level so that the resulting Eb/No will be O dB.

az. With the demodulator in the second sweep cycle, adjust R2 on A2A19 (B, fig 3-8) to obtain an average reading at TP10 of +1 25 V dc, as monitored on the oscilloscope (modem should lock up on the second or fourth sweep, voltage average around -5 V)

ba. Disconnect the oscilloscope from TP10

3-20. Deleted

Figure 3-11 deleted

3-21. Demodulator Phase Adjustment

An oscilloscope, an error rate counter, and a modem test set are required for this adjustment

NOTE

If the specified indication cannot be obtained, the probable cause Is a failure of the phase adjust and detector driver card, A2A14

a. Terminate the 70 MHz modem output into the modem test set input at the IF patch rack

b. Set the modem controls as shown in table 3-39. Set the POWER switch to ON

Table 3-39. Initial Control Settings for Receive Bit Synchronizer Adjustment

Control	Setting
ALARM RESET/OFF/ON	OFF
MODE	TEST
TRANSMIT INPUT DATA RATE	9 9999 MB/S
TRANSMIT QPSK/BPSK	QPSK
TRANSMIT ENCODER DIFF OFF	DIFF
TRANSMIT ENCODER EXT/OFF	OFF
RECEIVE I CHANNEL SYMBOL RATE	9 9999 MB/S
RECEIVE QPSK/BPSK	QPSK
RECEIVE DECODER DIFF/OFF	DIFF
RECEIVE DECODER EXT/OFF	OFF
MONITOR switch	ERROR COUNT
MONITOR ERROR COUNT switch	8
SWEEP CONTROL NORMAL WIDE	NORMAL
SWEEP CONTROL FAST/NORMAL	FAST
SWEEP CONTROL PARTIAL/FULL	FULL
RANDOMIZER TRANSMIT	OFF
RANDOMIZER RECEIVE	OFF

c. Monitor TP1 on A2A10 (fig 3-14) with channel 1 of an oscilloscope and monitor TP1 on A2A34 (fig 3-14) with channel 2 of an oscilloscope Synchronize the oscilloscope externally using the modem TEST OUTPUTS SYNC connector on the front panel

NOTE

Verify that channel 2 of the oscilloscope is not in the inverted mode.

d. After demodulator acquisition, adjust R8 on A2A14 (fig 3-12) until the waveform on channel 1 is a stable data sequence composed of just two levels (misadjustment will result In three or more discrete levels)

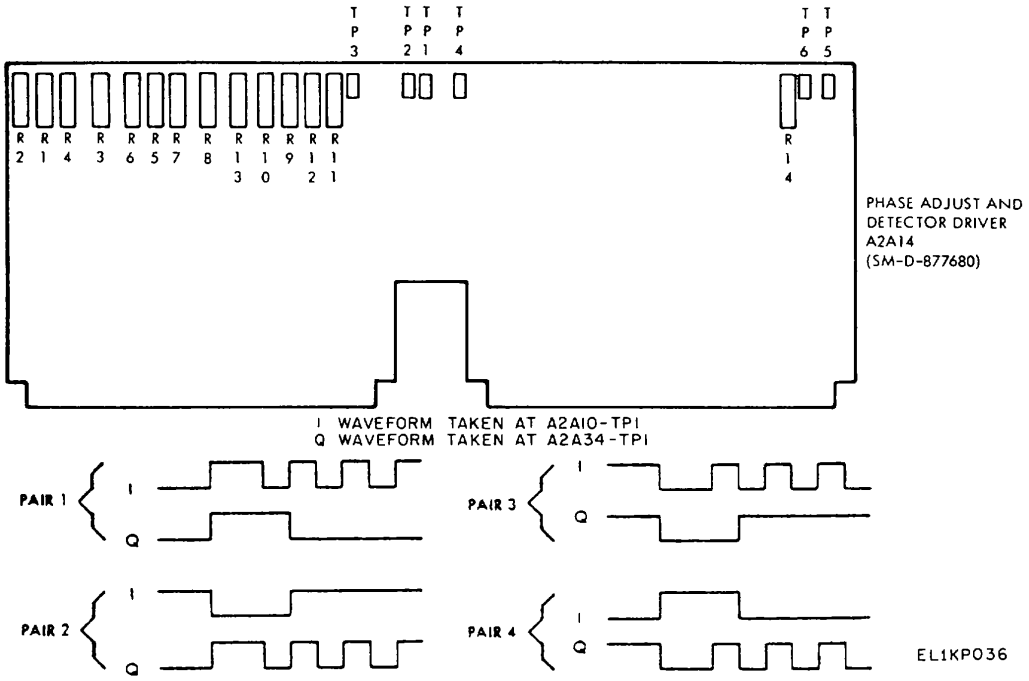


Figure 3-12. Phase adjust and detector driver, test points, adjustment locations and waveforms.

e. Compare the data waveform present on channel 1 of the oscilloscope with the I channel waveforms of the four waveform pairs (fig. 3-12) Determine which of the four waveform pairs (fig. 3-12) contains the I channel waveform displayed on channel 1 of the oscilloscope. For proper adjustment, the data waveform of the Q channel must be part of the same waveform pair as the I channel waveform. Therefore, adjust R14 on A2A14 until the data waveform on channel 2 of the oscilloscope is identical to the corresponding Q channel data waveform (fig. 3-12)

NOTE

Achieving one of the waveform pairs as in figure 3-12 is extremely important for proper operation with the external coder.

f. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 2.4999 MB/S

g. Adjust R10 on A2A14 until the waveforms on both oscilloscope channels are stable data sequences (d above).

h. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 629.99 KB/S.

i. Adjust R6 on A2A14 until the waveforms on both oscilloscope channels are stable data sequences (d above)

j. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 149.99 KB/S

k. Adjust R4 on A2A14 until the waveforms on both oscilloscope channels are stable data sequences (d above)

l. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 74.999 KB/S.

m. Adjust R2 on A2A14 until the waveforms on both oscilloscope channels are stable data sequences (d above).

n. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 37.999 KB/S.

o. Adjust R12 on A2A14 until the waveforms on both oscilloscope channels are stable data sequences (d above).

p. Change both the TRANSMIT and RECEIVE QPSK/BPSK switches to the BPSK position Set MONITOR ERROR COUNT thumbwheel to 0.

q. Adjust R11 on A2A14 until the data sequence at TP1 on A2A34 (Channel 2 of oscilloscope) is nulled

r. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 74.999 KB/S

s. Adjust R1 on A2A14 until the data sequence on channel 2 of the oscilloscope is nulled.

t. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 149.99 KB/S.

u. Adjust R3 on A2A14 until the data sequence on channel 2 of the oscilloscope is nulled.

v. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel siwtches to 249 99 KB/S.

w. Adjust R13 on A2A14 until the data sequence on channel 2 of the oscilloscope is nulled

x. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 629 99 KB/S

y. Adjust R5 on A2A14 until the data sequence on channel 2 of the oscilloscope is nulled

z. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 2 4999 MB/S

aa. Adjust R9 on A2A14 until the data sequence on channel 2 of the oscilloscope is nulled.

ab. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 9.9999 MB/S.

ac. Adjust R7 on A2A14 until the data sequence on channel 2 of the oscilloscope is nulled.

ad Set the TRANSMIT section to QPSK at
9 9999 MB/S, and RECEIVE section to QPSK at
4.9999 MB/S, both uncoded

ae. Set MODE switch to LINK.

af. Set modem test set for Eb/No = 11 5 dB

ag. Connect modem test set output to modem input (AT2J 1)

ah. Connect modem TEST OUTPUTS ERROR and CLOCK outputs to error rate counter ERROR and CLOCK inputs, respectively.

ai. Refer to figure 3-16 If bit error rate (BER) is within tolerance, return modem to service, if not, proceed to paragraph 3-22 (Error rate counter must be terminated in 50 ohms)

3-22. Receive Bit Synchronizer Alinement

An oscilloscope, a modem test set, a digital voltmeter (DVM), an rf power meter (MW-828A), an error rate counter, two card extenders (759649), and a card puller (7920) are required for this adjustment.

a. Terminate the 70 MHz modem output into the modem test set input at the IF patch rack

b. Set the QPSK/BPSK modem front panel controls as shown m table 3-39. Set the POWER switch to the ON position.

c. Place A2A31 on card extender

d. Use DVM to monitor point A (pin 12 of U1 on fig. 3-13) and adjust R19 for -O 4 +0.05 V dc.

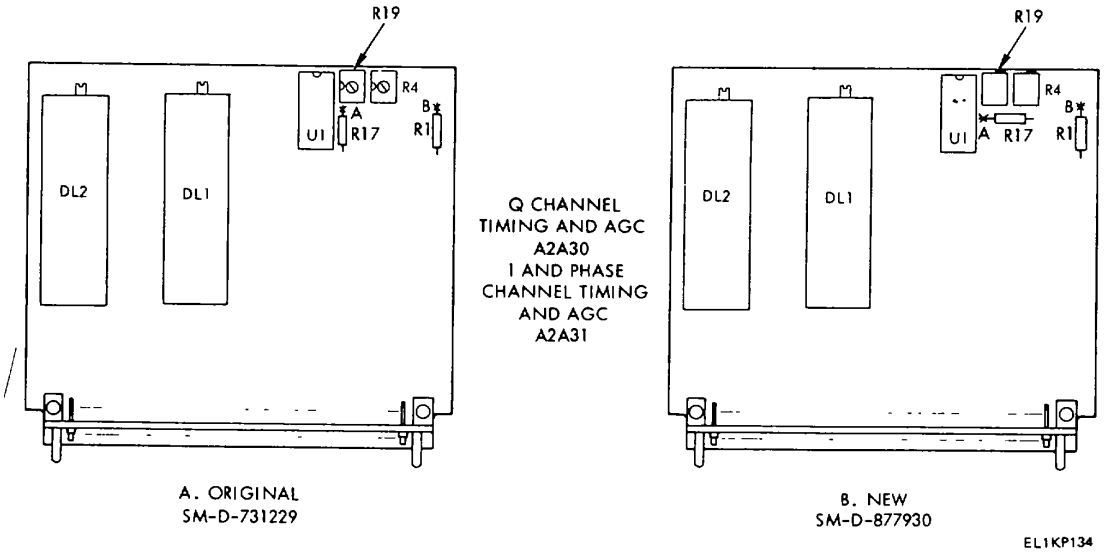


Figure 3-13. Timing and AGC, test points and adjustment locations.

e. Use DVM to monitor point B (pin 5 of U1 of fig. 3-13) and adjust R4 for +0.4 +0.05 V dc.

f. Return A2A31 to card file, place A2A30 on card extender.

g. Use DVM to monitor point A (fig. 3-13) and adjust R19 for -0.4 +0.05 V dc.

h. Use DVM to monitor point B (fig. 3-13) and adjust R4 for +0 4 +0.05 V dc.

i. Return A2A30 to the card file.

j. On A2A31 adjust delay linens DL1 and DL2 controls fully counter clockwise (fig. 3-13).

k. On A2A30 adjust delay line DL1 control fully counterclockwise (fig. 3-13).

l. Place A2A12 on a card extender. Monitor TP1 of A2A10 with oscilloscope. Alternately adjust C4 and C6 on A2A12 (fig. 3-25) to obtain best square waveform. Return A2A12 to card file.

m. Place A2A36 on a card extender. Monitor TP1 of A2A34 with oscilloscope. Alternately adjust C4 and C6 on A2A36 to obtain best square waveform. Return A2A36 to card file.

n. Set the both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 1.2000 MB/S.

o. Place the I channel integrator card, A2A10, on a card extender.

p. Use a digital voltmeter to monitor point B on figure 3-14, and adjust R31 on A2A10 to read 0 +10 mV dc.

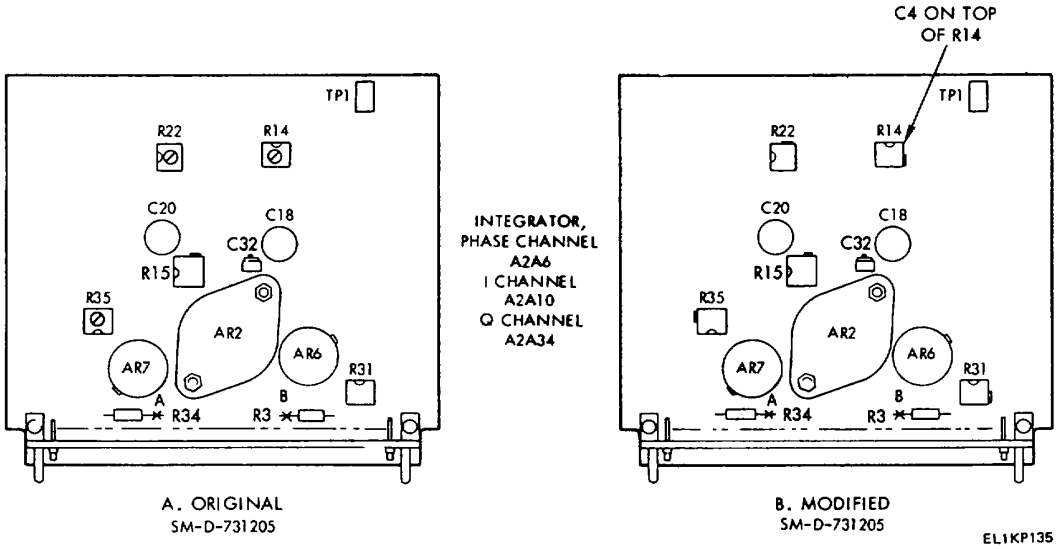


Figure 3-14. Integrator, test points and adjustment locations

q. Use a digital voltmeter to monitor point A (fig. 3-14) and adjust R35 on A2A10 to read 0 +10 mV dc.

r. Monitor pin 21 of A2A10 with one channel of the oscilloscope. Adjust R14 and R22 of A2A10 (fig. 3-14) to maximize the amplitude of the waveform peaks. The two resistors, R14 and R22, will each control the magnitude of alternate waveform peaks. Then, adjust the resistor controlling the largest peaks so as to reduce the amplitude until they equal the amplitude of the peaks controlled by the other resistor.

s. Return A2A10 to the card file and place A2A6 on a card extender.

t. Use a digital voltmeter to monitor point B (fig. 3-14) and adjust R31 on A2A6 to read 0 +10 mV dc.

u. Use a digital voltmeter to monitor point A (fig. 3-14) and adjust R35 on A2A6 to read 0 +10 mV dc.

v. Use a digital voltmeter to monitor TP1 (or point A) on A2A4 (fig. 3-15) and, if necessary, adjust R15 on A2A6 to reduce the dc offset to 0 +20 mV dc. If this level cannot be obtained, readjust R31 on A2A6 to reduce the dc voltage offset to 0 + 20 mV dc.

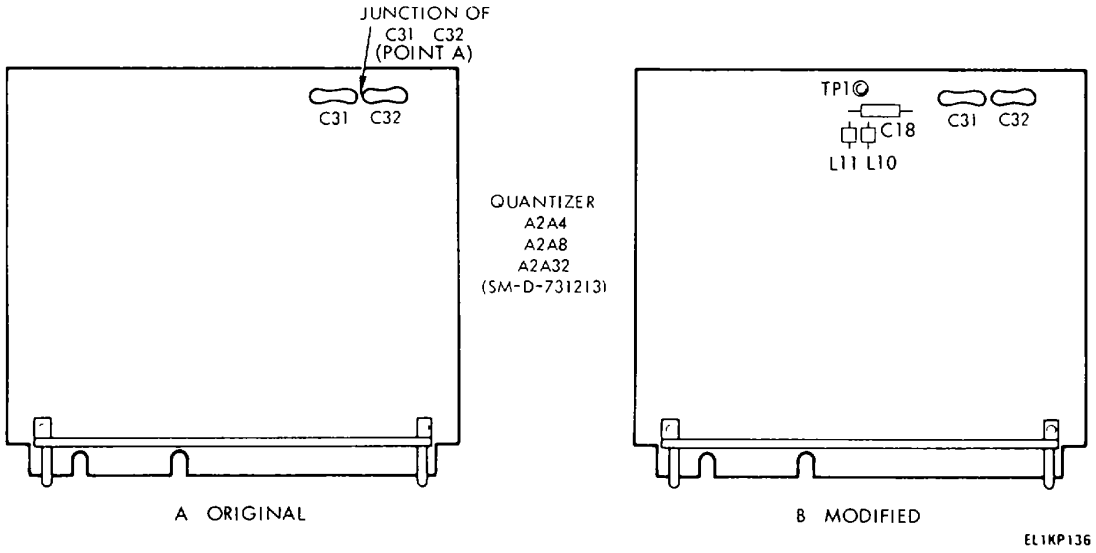


Figure 3-15. Quantizer, test points and adjustment locations.

w. Monitor pin 21 of A2A6 with one channel of the oscilloscope Adjust R14 and R22 of A2A6 (fig 3-14) to maximize the amplitude of the waveform peaks The two resistors, R14 and R22, will each control the magnitude of the alternate waveform peaks Then, adjust the resistor controlling the largest peaks to reduce their amplitude until they equal the amplitude of the peaks controlled by the other resistor.

x. Return A2A6 to the card file and place A2A34 on a card extender.

y. Use a DVM to monitor point B on card B (fig 3-14) and adjust R31 on A2A34 to read 0 +10 mV dc.

z. Use a DVM to monitor point A on figure 3-14 and adjust R35 on A2A34 to read 0 + 10 mV dc.

aa. Use a DVM to monitor TP1 or point A on A2A32 (fig. 3-15) and, if necessary, adjust R15 on A2A34 to reduce the dc offset to 0 +20 mV dc. If this level cannot be obtained, readjust R31 on A2A34 to reduce the dc voltage offset to 0 + 20 mV dc.

ab. Monitor pin 21 of A2A34 with one channel of an oscilloscope Adjust R14 and R22 of A2A34 (fig 3-14) to maximize the amplitude of the waveform peaks. The two resistors, R14 and R22, will each control the magnitude of alternate waveform peaks. Then, readjust the resistor controlling the largest peaks to reduce their amplitude until they equal the amplitude of the peaks controlled by the other resistor.

ac. Return A2A34 to the card file.

ad. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 9 9999 MB/S.

ae. Place A2A10 on a card extender Monitor pin 21 of A2A10 with an oscilloscope Adjust C18 and C20 of A2A10 (fig 3-14) to maximize the amplitude of the waveform peaks. The two capacitors, C18 and C20, will each control the magnitude of alternate waveform peaks Then, readjust the capacitor controlling the largest peaks to reduce their amplitude until they equal the amplitude of the peaks controlled by the other capacitor.

af. While continuing to monitor pin 21 of A2A10, adjust C32 on A2A10 (fig 3-14) to minimize the distance shown by the arrow in figure 3-15.1

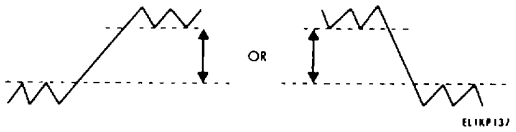


Figure 3-15.1. Falter bandwidth adjustment waveforms

ag. Return A2A10 to the card file and place A2A6 on a card extender.

ah. While monitoring pin 21 of A2A6 with an oscilloscope, adjust C18 and C20 of A2A6 (fig. 3-14) to maximize the amplitude of the waveform peaks. The two capacitors, C18 and C20, will each control the amplitude of alternate waveform peaks. Then, reduce the amplitude of the largest peaks until all the peaks have equal amplitude.

ae. Set MONITOR ERROR COUNT thumbwheel switch to position 15, adjust C32 on A2A6 (fig. 3-14) for minimum deflection on front panel MONITOR meter

aj. Return A2A6 to the card file and place A2A34 on a card extender

ak. While monitoring pin 21 of A2A34 with an oscilloscope, adjust C18 and C20 of A2A34 (fig. 3-14) to maximize the amplitude of the waveform peaks. The two capacitors, C18 and C20, will each control the amplitude of alternate waveform peaks Then, reduce the amplitude of the largest peaks until all the peaks have equal amplitude.

al. While continuing to monitor pin 21 of A2A34, adjust C32 on A2A34 (fig 3-14) to minimize the distance along the arrow, as shown in figure 3-15.1. am Return A2A34 to the card file. am Set the modem test set for a data rate of 20 MB/S at an Eb/No= 11 5 dB and connect to modem.

ao. Place the MONITOR ERROR COUNT thumbwheel switch to position 8. Place modem in link mode.

ap. Connect rf power meter (MV-828A) to the TEST OUTPUTS ERROR jack on the front panel of the modem.

aq. On A2A31 (fig 3-13) alternately adjust delay lines DL1 and DL2 for minimum reading (microvolts) on the rf power meter.

ar. Place the MONITOR ERROR COUNT thumbwheel switch to position 9.

as. On A2A30 (fig. 3-13) adjust DL1 for a minimum reading (microvolts) on the rf power meter.

at. Disconnect the rf power meter and connect the error rate counter to the ERROR and CLOCK TEST OUTPUTS on the modem front panel.

au. Place the MONITOR ERROR COUNT thumbwheel switch to position 8.

av. Connect the error rate counter (properly terminated in 50 ohms) to the modem test jacks and note the I channel bit error rate as indicated by the ERROR COUNTER on the error rate counter.

aw. Change the MONITOR ERROR COUNT thumbwheel switch to position 9 and note the Q channel bit error rate as indicated by ERROR COUNTER on the error rate counter.

ax. Compare the measured results of the previous two steps with the theoretical bit error rate performance curves of figure 3-16. Using the curves, determine how close to theoretical curve the modem is operating and note this number for both the I and Q channels

ay. Change the MONITOR ERROR COUNT thumbwheel switch to position 10 in order to monitor the I channel MSB

az. Note the rate at which I channel MSB errors are occuring as displayed by the ERROR COUNTER on the error rate counter. Compare the measured result with the theoretical MSB error rate performance curve of figure 3-16. Determine how close to the theoretical curve the MSB error rate reading is. The MSB performance degradation and the 1 channel bit error rate performance degradation, as determined in step ax above, should be the same distance from their respective theory curves within 0.5 dB of each other If this is true, continue to step ba. If it is not true, place the timing and AGC card, A2A31 on a card extender (not necessary if A2A31 is new configuration, SM-D-877930) and adjust R4 and R19 of A2A31 (fig. 3-13) by equal amounts until the MSB performance degradation is equal to the bit error rate performance degradation +0 5 dB. If A2A31 is on a card extender, return it to the card file.

ba. Change the MONITOR ERROR COUNT thumbwheel switch to position 11 in order to monitor the Q channel MSB.

bb. Note the Q channel MSB error rate as displayed by the ERROR COUNTER on the error rate counter. Compare the measured results with the theoretical MSB error rate performance curve of figure 3-16 Determine how close to the theoretical curve the MSB error rate reading is. This MSB performance degradation and the Q channel bit error rate performance degradation, as determined in step ax above, should be within 0 5 dB of each other at Eb/No = 11.5 dB. If this is true, the alinement is complete. If it is not, place the timing and AGC card A2A30 on a card extender (not necessary if A2A30 is new configuration, SM-D-877930) and adjust R4 and R19 of A2A30 (fig 3-13) by equal amounts until the MSB performance degradation is equal to the bit error rate performance degradation +0.5 dB If A2A30 is on a card extender, return it to the card file

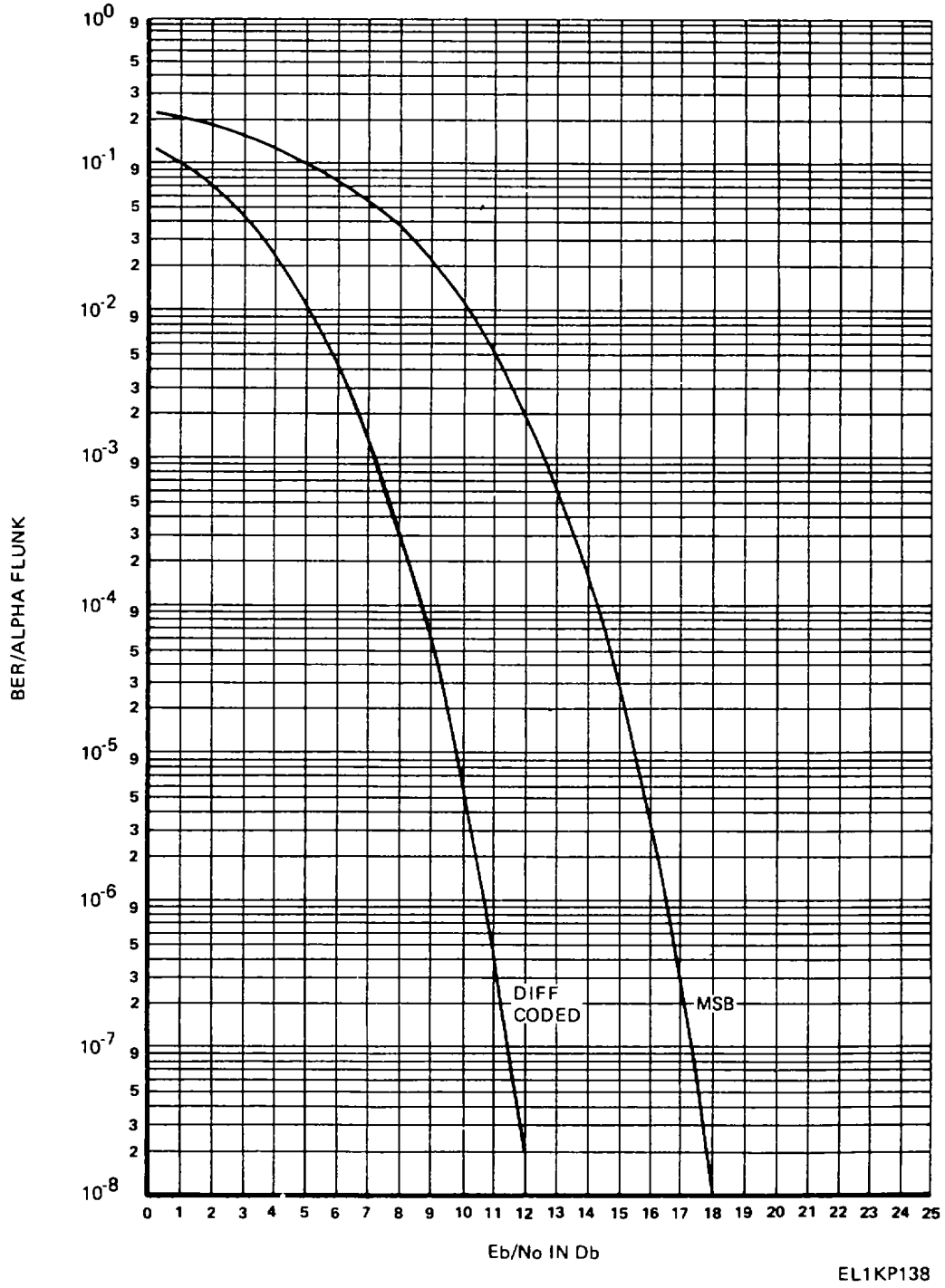


Figure 3-16. Modem theoretical performance curves

3-23. Deleted.

3-24. Encoder Switch Timing Alinement

A card extender (759649), a card puller (7920), and an oscilloscope are required for this adjustment.

a. Set front panel switches as shown In table 3-39.

CAUTION

Encoder switch A3A6 may be damaged if removed or reinstalled with power on.

b. Turn power OFF. Place the encoder switch card, A3A6, on a card extender.

c. Turn power ON. Monitor pin 12 of the encoder switch card A3A6 (fig. 3-17) with an oscilloscope

NOTE

The oscilloscope probe requires the use of a short ground clip terminating on the nearest ground to the test point under observation.

d Adjust C1 (fig. 3-17) on the encoder switch card, A3A6, to produce a dc clock signal at pin 12 (as monitored by the oscilloscope) for a clean symmetrical waveform (fig 3-17.1).

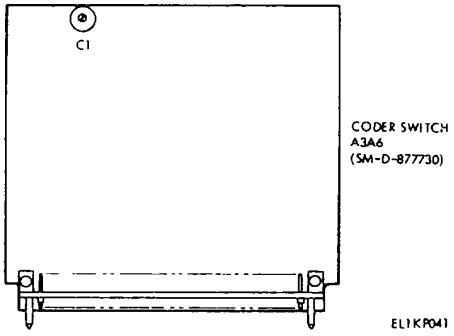


Figure 3-17. Encoder switch, test points and adjustment locations.

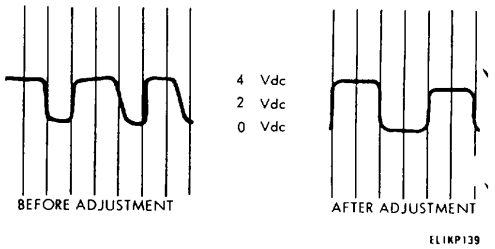


Figure 3-17.1. Encoder switch timing alinement, dc clock waveforms

CAUTION

Encoder switch A3A6 may be damaged if removed or reinstalled with power on.

e. Turn power OFF Remove card extender and return encoder switch to card file A3A6.

3-25. Receive Bit Synchronizer Alarm Threshold Alinement

A modem test set is required for this alinement

a. Set front panel switches as shown in table 3-39 Set POWER switch to ON position.

b. Connect modem output (AT1J1) to modem test set input and modem input (AT2J1) to modem test set output. Using the modem test set, adjust the signal-to-noise ratio at the demodulator input for an Eb/No of 1 dB at a data rate of 9 9999 MB/S

c. Adjust R9 (fig. 3-18) on the phase and loss of lock detector card, A3A13, until the RECEIVE BIT SYNC FAULT lamp on the front panel just extinguishes.

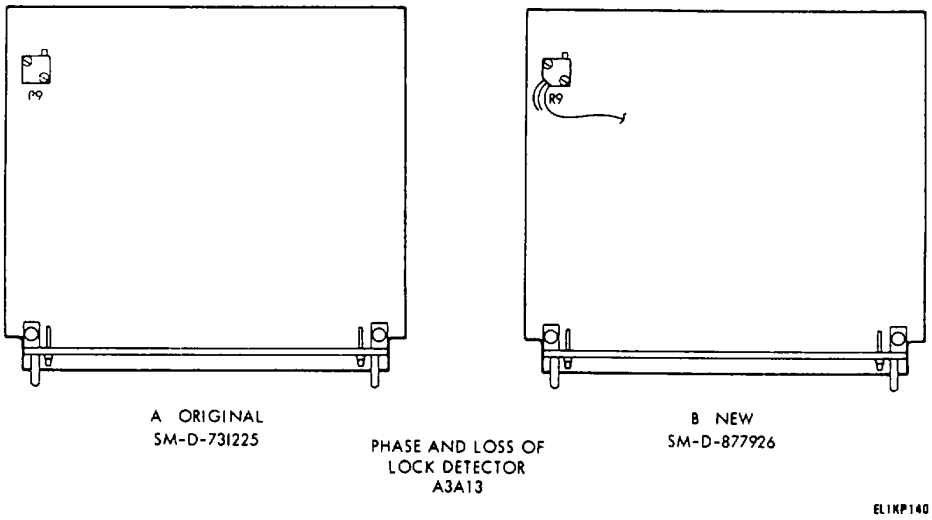


Figure 3-18. Phase and loss of lock detector, adjustment locations.

d. Reduce the Eb/No to 0 dB. Verify that the RECEIVE BIT SYNC FAULT lamp on the front panel is flashing.

3-26. Phase Control Integrator A2A6, Abbreviated Alinement

a. Disconnect the external cables from ATIJ1 and AT2J1 (located on rear panel).

b. Set the modem controls as shown in table 3-39 except set the TRANSMIT INPUT DATA RATE to 1 2 MB/S Set the POWER switch to ON.

c. Place A2A6 on a card extender.

d. While using an oscilloscope to monitor pin 11 of AR6 on A2A6 (fig 3-14), adjust R31 on A2A6 as required to reduce the dc voltage offset at AR6-11 to 0 ± 10 mV dc

e. While using an oscilloscope to monitor pin 11 of AR7 on A2A6 (fig. 3-14), adjust R35 on A2A6 as required to reduce the dc voltage offset at AR7-11 to O +10mV dc

f. Monitor the junction between C31 and C32 on A2A4 (fig. 3-15) with an oscilloscope and, if necessary, adjust R15 on A2A6 to reduce the dc offset to 0 +mV dc. If this level cannot be obtained, readjust R31 on A2A6 slightly to reduce the dc voltage offset to 0 ± 20 mV dc.

NOTE

If the normal operating frequency is above 1 2 Mb/s, perform the following. If operating below 1 2 Mb/s, perform steps w, x, and y below.

g Monitor pin 21 of A2A6 (fig. 3-1) with one channel of the oscilloscope. Adjust R14 and R22 of A2A6 (fig 3-14) to maximize the amplitude of the waveform peaks The two resistors, R14 and R22, will each control the magnitude of alternate waveform peaks. Then, adjust the resistor controlling the largest peaks to reduce their amplitude until they equal the amplitude of the peaks controlled by the other resistor.

h. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 9 9999 MB/S.

i. Place A2A10 on a card extender. Monitor pin 21 of A2A10 (fig 3-1) with an oscilloscope. Adjust C18 and C20 of A2A10 (fig. 3-14) to maximize the amplitude of the waveform peaks; the two capacitors, C18 and C20, will each control the magnitude of alternate waveform peaks. Then, readjust the capacitor controlling the largest peaks to reduce their amplitude until they equal the amplitude of the peaks controlled by the other capacitor

j. While continuing to monitor pin 21 of A2A10, adjust C32 on A2A10 (fig 3-14) to minimize the amplitude of the waveform between adjacent peaks

k. Return A2A10 to the card file and place A2A6 on a card extender.

l. While monitoring pin 21 of A2A6 with an oscilloscope, adjust C18 and C20 of A2A6 (fig 3-14) to maximize the amplitude of the waveform peaks The two capacitors, C18 and C20, will each control the amplitude of alternate waveform peaks. Then readjust the capacitor controlling the largest peaks to reduce their amplitude until they equal the amplitude of the peaks controlled by the other capacitor

m. While continuing to monitor pin 21 of A2A6, adjust C32 on A2A6 (fig 3-14) to minimize the amplitude of the waveform between adjacent peaks

n. Set the MONITOR ERROR COUNT thumbwheel switch to position 12 in order to monitor the phase channel MSB on the front panel MONITOR meter.

o. On the timing and AGC card, A2A31, adjust the phase delay line, DL2, (fig. 3-13) until the MONITOR meter reading goes to zero.

p. Set the MONITOR ERROR COUNT thumbwheel switch to position 13 in order to monitor the I channel LSB on the front panel MONITOR meter.

q. On the timing and AGC card, A2A31, adjust the data delay (DL1) line (fig. 3-13) until the MONITOR meter reading is at a minimum (should read less than 10 when adjustment is complete).

r. Set the MONITOR ERROR COUNT thumbwheel switch to position 14 In order to monitor the Q channel LSB on the front panel MONITOR meter

s. On the second timing and AGC card, A2A30, adjust the data delay line, DL1, (fig. 3-13) until the MONITOR meter reading is at a minimum (should read less than 10 when adjustment is complete).

t. Set the MONITOR ERROR COUNT thumbwheel switch to position 15 in order to monitor the phase channel LSB on the MONITOR meter

u. On the first timing and AGC card, A2A31, slowly adjust the phase delay line, DL2 (fig. 3-13), slightly to minimize the meter reading. (Reading should be less than 25)

v. Return the MONITOR ERROR COUNT thumbwheel switch to positions 12 through 14 and finally to 15 again (steps n through t above). Adjust the appropriate delay line to minimize the MONITOR meter readings if not within limits and continue with next step

NOTE

Due to the interdependence of the I, Q, and phase channels of the receive bit synchronizer, some interaction will be noted between the adjustments of the three delay lines.

w. Set the modem TRANSMIT INPUT DATA RATE switches to the operating frequency.

x. Set the modem MONITOR meter switch to ERROR COUNT, and the thumbwheel switches to 0

y. Connect the Modem Test Set TS-3580/G to the modem (modem test set INPUT and OUTPUT connectors to modem AT1J1 and AT2J1, respectively) Perform the Eb/No test at the operating frequency and at the operational signal-to-noise level. Compare the measured error rate with the theoretical bit error rate of figure 3-20, the measured bit error rate shall be no greater than the maximum allowable bit error rate shown in figure 3-20 If the error rate is within tolerance, return the modem to service If the error rate is not within tolerance, perform the complete receive bit synchronizer alinement (para 3-22).

3-27. Phase Control Integrator A2A10, Abbreviated Alinement

a. Disconnect the external cables from ATIJ1 and AT2J 1 (located on rear panel).

b. Set the modem controls as shown in table 3-39 except set the TRANSMIT INPUT DATA RATE to 1 2 MB/S Set the POWER switch to ON

c. Place the I channel integrator card, A2A10, on a card extender.

d. While using an oscilloscope to monitor pin 11 of AR6 on A2A10 (fig. 3-14), adjust R31 on A2A10 as required to reduce the dc voltage offset at AR6-11 to O + 10 mV dc.

e. While using an oscilloscope to monitor pin 11 of AR7 on A2A10 (fig 3-14), adjust R35 on A2A10 as required to reduce the dc voltage offset at AR7-11 to 0 + 10 mV dc.

f. Monitor pin 21 of A2A10 with one channel of the oscilloscope Adjust R14 and R22 of A2A10 (fig. 3-14) to maximize the amplitude of the waveform peaks. The two resistors, R14 and R22, will each control the magnitude of alternate waveform peaks Then, adjust the resistor controlling the largest peaks so as to reduce their amplitude until they equal the amplitude of the peaks controlled by the other resistor

g. Monitor the junction between C31 and C32 on A2A4 (fig. 3-15) with an oscilloscope and, if necessary adjust R15 on A2A6 to reduce the dc offset to 0 +20 mV dc If this level cannot be obtained, readjust R31 on A2A10 slightly to reduce the dc voltage offset to 0 ± 20 mV dc.

NOTE

If operating below 1.2Mb/s, perform steps r, s, and t below. If operating above 1.2 Mb/s, perform the following

h. Set both the TRANSMIT INPUT DATA RATE and the RECEIVE I CHANNEL SYMBOL RATE thumbwheel switches to 9 9999 MB/S.

i. Place A2A10 on a card extender. Monitor pin 21 of A2A10 with an oscilloscope Adjust C18 and C20 of A2A10 (fig 3-14) to maximize the amplitude of the waveform peaks. The two capacitors, C18 and C20, will each control the magnitude of alternate waveform peaks. Then, readjust the capacitor controlling the largest peaks to reduce their amplitude until they equal the amplitude of the peaks controlled by the other capacitor

j. While continuing to monitor pin 21 of A2A10, adjust C32 on A2A10O (fig. 3-14) to minimize the amplitude of the waveform between adjacent peaks.

k. Set the MONITOR ERROR COUNT thumbwheel switch to position 12 in order to monitor the phase channel MSB on the front panel MONITOR meter

l. On the timing and AGC card, A2A31, adjust the phase delay line, DL2, (fig. 3-13) until the MONITOR meter reading goes to zero.

m. Set the MONITOR ERROR COUNT thumbwheel switch to position 13 in order to monitor the I channel LSB on the front panel MONITOR meter.

n. On the timing and AGC card, A2A31, adjust the data delay (DL1) line (fig 3-13) until the MONITOR meter reading is at a minimum (should read less than 10 when adjustment is complete)

o. Set the MONITOR ERROR COUNT thumbwheel switch to position 14 in order to monitor the Q channel LSB on the front panel MONITOR meter.

p. On the second timing and AGC card, A2A30, adjust the data delay line, DL1 (fig. 3-13) until the MONITOR meter reading is at a minimum (should read less than 10 when adjustment is complete)

q. Return the MONITOR ERROR COUNT thumbwheel switch to positions 12 through 14 and finally to 15 again (steps k through p above). Adjust the appropriate delay line to minimize the MONITOR meter readings if not within limits and continue with next step.

NOTE

Due to the interdependence of the I, Q, and phase channels of the receive bit synchronizer, some interaction will be noted between the adjustments of the three delay lines.

r. Set the modem TRANSMIT INPUT DATA RATE switches to the operating frequency.

s. Set the modem MONITOR meter switch to ERROR COUNT, and the thumbwheel switches to 0.,

t. Connect the Modem Test Set TS-8580/G to the modem (modem test set INPUT and OUTPUT connector to modem AT1J1 and AT2J1, respectively). Perform the Eb/No test at the operating frequency and at the operational signal-to-noise level. Compare the measured error rate with the theoretical bit error rate of figure 3-20. If the error rate is within tolerance, return the modem to service. If the error rate is not within tolerance, perform the complete receive bit synchronizer alinement (para 3-22).

3-28. Data Detector and Driver (A2A12/ A2A26) Abbreviated Alinement

a. Disconnect the external cables connected to AT1J1 and AT2J1 (on the rear panel).

b. Set the QPSK/BPSK modem front panel controls as shown in table 3-38. Set the POWER switch to the ON position.

c. Using the Modem Test Set TS-3580/G, adjust the signal-to-noise ratio at the demodulator input for an Eb/No of 5 dB at a data rate of 9.9999 Mb/s, QPSK.

d. Alternately adjust CA4 and C6 on the data detector and driver card, A2A12 (fig. 3-25), to obtain minimum front panel MONITOR meter deflection. (For more accurate adjustment, connect frequency counter to front panel TEST OUTPUTS ERROR connector and adjust for minimum error count.)

e. Set the modem MONITOR meter switch to ERROR COUNT, and the thumbwheel switches to 8.

f. Connect the Modem Test Set TS-3580/G to the modem (modem test set INPUT and OUTPUT connectors to modem ATlJ1 and AT2J1, respectively). Perform the Eb/No at 19.999 Mb/s and at 7 dB. Compare the measured error rate with the theoretical bit error rate of figure 3-20; the measured bit error rate shall be no greater than the maximum allowable bit error rate shown in figure 3-20. If the error rate is within tolerance, return the modem to service. If the error rate is not within tolerance, perform the complete receive bit synchronizer alinement (para 3-22).

3-29. Phase Adjust and Detector Driver (A2A14 Abbreviated Alinement

a. When replacing the phase adjust and detector driver card, A2A14, with a new card, it may be necessary to adjust the new card in order to determine if the problem has been corrected. This determination can be made by adjusting only those resistor(s) concerned with the specific data rate being used. The following table indicates which resistor or resistors must be adjusted for each data rate range and mode. See figure 3-12 for resistor locations.

I CHANNEL SYMBOL RATE

Mode	switch setting range	Adjust A2A14 resistor(s)
BPSK	16.000 KB/S to 87.999 KB/S	R11
BPSK	88.000 KB/S to 74.999 KB/S	R1
BPSK	75.000 KB/S to 149.99 KB/S	R3
BPSK	150.00 KB/S to 249.99 KB/S	R13
BPSK	250.00 KB/S to 629.99 KB/S	R5
BPSK	630.00 KB/S to 2.4999 MB/S	R9
BPSK	2.5000 MB/S to 9.9999 MB/S	R7
QPSK	25.000 KB/S to 87.999 KB/S	R12 and R14
QPSK	88.000 KB/S to 74.999 KB/S	R2 and R14
QPSK	75.000 KB/S to 149.99 KB/S	R4 and R14
QPSK	150.00 KB/S to 629.99 KB/S	R6 and R14
QPSK	630.00 KB/S to 2.4999 MB/S	R10 and R14
QPSK	2.5000 MB/S to 9.9999 MB/S	R8 and R14

b. To perform the necessary adjustment(s) follow these instructions:

(1) Disconnect the external cables from AT1J1 and AT2J1 (located on rear panel).

(2) Set the modem controls as shown in table 3-39. Set the POWER switch to ON.

(3) After the new phase adjust the detector driver card has been placed into location A2A14, monitor the I channel integrator input (TP1 on A2A10, fig. 3-14) with channel one of an oscilloscope and monitor the Q channel integrator input (TPI on A2A34, fig. 3-14) with channel 2 of an oscilloscope. Synchronize the oscilloscope externally using the sync output on the modem front panel.

(4) If the modem is in the BPSK mode, perform step (a) below and proceed to step (6) below. If the modem is in the QPSK mode, perform step (b) below and proceed to step (5) below.

(a) Adjust the resistor that corresponds to the present BPSK data rate for maximum signal amplitude on channel 1 of oscilloscope.

(b) Adjust the first resistor listed for the cor-

responding data rate until the waveform on channel 1 is a stable data sequence composed of just two levels (misadjustment will result in an oscilloscope display containing three or four discrete levels).

NOTE

If the desired adjustment cannot be accomplished, the original phase adjust and detector driver card, A2A14, was not the faulty card. Therefore, remove the new card, A2A14, and return the original card to location A2A14. Resume the card replacement sequence.

(5) For QPSK operation, also adjust the second resistor listed until the waveform on channel 2 is a stable data sequence composed of just two levels.

NOTE

It may be necessary to readjust both resistors several times to achieve the desired waveforms.

(6) Set the modem TRANSMIT INPUT DATA RATE switches to the operating frequency.

(7) Set the modem MONITOR meter switch to ERROR COUNT, and the thumbwheel switches to 0.

(8) Connect the Modem Test Set TS-3580/G to the modem (modem test set INPUT and OUTPUT connectors to modem ATiJ1 and AT2J1, respectively). Perform the Eb/No test at the operating frequency and at the operational signal-to-noise level Compare the measured error rate with the theoretical bit error rate of figure 3-20; the measured bit error rate shall be no greater than the maximum allowable bit error rate shown in figure 3-20. If the error rate is within tolerance, return the modem to service. If the error rate is not within tolerance, perform the complete receive bit synchronizer alinement (para 3-22).

3-30. 70 MHz, Gain Control Amplifier A2A1 6, Abbreviated Alinement

a. Disconnect the external cables connected to AT1J1 and AT2J1 on the rear panel.

b. Set the QPSK/BPSK modem front panel controls as shown in table 3-35 except set the TRANSMIT INPUT DATA RATE to the operating frequency. Set the POWER switch to the ON position.

c. Connect the RF power meter (MV-828A) to TP8 on the X2/X4 multiplier card, A2A20 (A, fig. 3-8). d Monitor the RF power meter and adjust R118 on the coherent detector and AGC loop amplifier card, A2A19 (B, fig. 3-8), to obtain a reading of -31 dBm ±0.2 dB.

NOTE

If the specified -31 dBm indication cannot be obtained by adjustment, the probable cause of failure is the 70 MHz gain control amplifier, A2A16, or the filters and distribution amplifier card, A2A18 However, the X2/X4 multiplier, A2A20, the coherent detector and AGC loop amplifier, A2A19, the phase lock loop amplifier and sweep circuit, A2A24, could also cause this failure. Refer to fault isolation table 3-13.

e. Disconnect the RF power meter from TP8 on the X2/X4 multiplier card, A2A20

NOTE

If a specified MONITOR meter DEMOD AGC indication or a specified RECEIVE PWR FAULT indication cannot be obtained below, the probable cause is a failure of the coherent detector and AGC loop amplifier card, A2A19.

f. Set the modem MONITOR meter switch to the DEMOD VCXO position If the modem receive bit synchronizer acquires phase lock (RECEIVE PH LOCK FAULT not flashing), perform steps g, h, and i below. If the modem receive bit synchronizer does not acquire phase lock, perform the abbreviated demodulator phase alinement (A2A14, para. 3-29).

g. Set the modem TRANSMIT INPUT DATA RATE switches to the operating frequency.

h. Set the modem MONITOR meter switch to ERROR COUNT, and the thumbwheel switches to 0.

i. Connect the Modem Test Set TS-3580/G to the modem (modem test set INPUT and OUTPUT connectors to modem AT1Jl and AT2J1, respectively). Perform the Eb/No test at the operating frequency and at the operational signal-to-noise level. Compare the measured error rate with the theoretical bit error rate of figure 3-20; the measured bit error rate shall be no greater than the maximum allowable bit error rate shown in figure 3-20. If the error rate is within tolerance, return the modem to service If the error rate is not within tolerance, perform the complete receive bit synchronizer alinement (para 3-22).

3-31. Coherent Detector and AGC Loop Amplifier (A2A19), Abbreviated Alinement

a. Disconnect the external cables connected to AT1J1 and AT2J1 on the rear panel. Set MODE switch to LINK.

b. Connect ATIJ1 to AT2J1 (on the rear panel) via an HP 355C step attenuator and an HP 355D step attenuator set to provide a total attenuation of 85 dB (65 dB).

c. Connect the RF power meter (MV-828A) to TP8 on the X2/X4 multiplier card, A2A20 (A, fig. 3-8)

d. Monitor the RF power meter and adjust R118 on

the coherent detector and AGC loop amplifier card, A2A19 (B, fig. 3-8), to obtain a reading of -31 dBm +0.2 dB.

NOTE

If the specified -31 dBm indication cannot be obtained by adjustment, the probable cause of failure is the 70 MHz gain control amplifier, A2A16, or the filters and distribution amplifier card, A2A18. However, the X2/X4 multiplier, A2A20, the coherent detector and AGC loop amplifier, A2A19, the phase lock loop amplifier and sweep circuit, A2A24, could also cause this failure. Refer to fault isolation table 3-13.

e. Connect the DVM to TP1 of A2A35 (fig. 3-9).

f. Set the modem MONITOR switch to DEMOD AGC

g. Allow modem to acquire phase lock.

h Adjust R28 on A2A20 (A, fig. 3-8) for 922 +20mV dc.

i. Adjust R134 on A2A19 (B, fig. 3-8) for modem meter reading of 0.

j. Set the attenuators for a total attenuation of 30 dB.

k. Adjust R108 on A2A19 (B, fig. 3-8) for a modem MONITOR meter reading of 100.

NOTE

If the modem TRANSMIT PWR FAULT lamp flashes, adjust R113 and R115 on A2A19 (B, fig. 3-8) fully clockwise.

l. Disconnect the attenuators. Connect the Modem Test Set TS-3580/G to the modem (modem test set INPUT and OUTPUT to modem ATlJ1l and AT2J1, respectively). Set modem MODE switch to LINK and TRANSMIT INPUT DATA RATE to operating rate. Set the modem test set for 11 dB. If the modem receive bit synchronizer acquires phase lock, perform step u below. If the modem receive bit synchronizer does not acquire phase lock, perform steps m, n, o, above and u below.

m. Connect the oscilloscope channel 1 to TP10 of A2A19 (B, fig. 3-8). Connect the oscilloscope channel 2 to TP2 of A2A24 (fig. 3-10).

n. Set the modem MONITOR meter switch to the DEMOD VCXO position.

o. Adjust the appropriate potentiometer (see table below) on A2A19 (B, fig. 3-8) for a reading of -5 V dc (or more negative) on channel 1 of the oscilloscope.

Mode	TRANSMIT INPUT DATA RATE switch setting		Adjust resistor	
			A2A19	A2A24
BPSK	16 000 KB/S	37 999 KB/S	R22	R93
QPSK	38 000 KB/S	74 999 KB/S	R18	R89
QPSK	75 000 KB/S	149.99 KB/S	R22	R88
QPSK	150 00 KB/S	249 99 KB/S	R26	R87
QPSK	250 00 KB/S	629 99 KB/S	R30	R90
QPSK	630 00 KB/S	2 4999 MB/S	R35	R92
QPSK	2 500 MB/S	9 9999 MB/S	R38	R91

p. During the second sweep, observe channel 2 of the oscilloscope for a drift of the dc level. If drifting occurs, adjust the appropriate potentiometer on A2A24 (see table in step o above) (fig. 3-10) for minimum drift. FULL SWEEP INITIATE may be used to reinitiate the sweep cycle.

q. Remove the test set input to the modem.

r. On A2A19 (B, fig. 3-8), adjust the appropriate potentiometer (see table in step o above) for an average reading of approximately +5V dc on channel 1 of the oscilloscope.

s. Set the modem TRANSMIT INPUT DATA RATE switches to the operating frequency.

t. Set the modem MONITOR meter switch to ERROR COUNT, and the thumbwheel switches to 0

u. Connect the Modem Test Set TS-3580/G to the modem (modem test set INPUT and OUTPUT connectors to modem ATlJ1 and AT2J1, respectively). Perform the E b No test at the operating frequency and at the operational signal-to-noise level. Compare the measured error rate with the theoretical bit error rate of figure 3-20; the measured bit error rate shall be no greater than the maximum allowable bit error rate shown in figure 3-20. If the error rate is within tolerance, return the modem to service. If the error rate is not within tolerance, perform the complete receive bit synchronizer alinement (para 3-22).

3-32. X2/X4 Multiplier (A2A20), Abbreviated Alinement

a. Perform the adjustment of A2A14 (para 3-29)

b. Connect the DVM to TPI on A2A35 (fig. 3-9).

c. Adjust R28 on A2A20 (A, fig. 3-8) for a dvm reading of 922 ±20 mV dc.

d. Set the modem TRANSMIT INPUT DATA RATE switches to the operating frequency.

e. Set the modem MONITOR meter switch to ERROR COUNT, and the thumbwheel switch to 0.

f. Connect the Modem Test Set TS-3580/G to the modem (modem test set INPUT and OUTPUT connectors to modem AT1Jl and AT2J1, respectively). Perform the Eb/No test at the operating frequency and at the operational signal-to-noise level. Compare the measured error rate with the theoretical bit error rate of figure 3-20, the measured bit error rate shall be no greater than the maximum allowable bit error rate shown in figure 3-20. If the error rate is within tolerance, return the modem to service. If the error rate is not within tolerance, perform the complete receive bit synchronizer alinement (para 3-22).

3-33. Phase Lock Loop Amplifier and Sweep Circuit (A2A24), Abbreviated Alinement

a. Set the modem MODE switch to LEIK.

b. Set up equipment for Eb/No test of 3 dB, at the operational rate Connect the Modem Test Set TS-3580/G to the modem (test set INPUT and

OUTPUT connectors to AT1J1 and AT2J1, respectively).

c. Set the modem TRANSMIT INPUT DATA RATE switches to the operational data rate.

d. Connect the oscilloscope channel 1 to TP10 of A2A19 (B, fig. 3-8). Connect the oscilloscope channel 2 to TP2 of A2A24 (fig. 3-10).

e. Set the modem MONITOR meter switch to the DEMOD VCXO position.

f. Remove the input to the modem, from the test set.

g. Adjust the appropriate potentiometer (see table below) on A2A19 (B, fig. 3-8) for a reading of -5 V dc (or more negative) on channel 1 of the oscilloscope, while modem is in the second sweep.

Mode	TRANSMIT INPUT DATA RATE switch setting		Adjust resistor	
			A2A19	A2A24
BPSK	16 000 KB/S	37 999 KB/S	R2	R93
QPSK	50.000 KB/S	74 999 KB/S	R18	R89
QPSK	75.000 KB/S	149.99 KB/S	R22	R88
QPSK	150 00 KB/S	299 99 KB/S	R26	R87
QPSK	300 00 KB/S	1 2599 MB/S	R30	R90
QPSK	1.2600 MB/S	4.9999 MB/S	R35	R92
QPSK	5.0000 MB/S	9 9999 MB/S	R38	R91

h. During the second sweep, observe channel 2 of the oscilloscope for a drift of the dc level. If drifting occurs, adjust the appropriate potentiometer on A2A24 (see table in step g above) (fig. 3-10) for minimum drift. FULL SWEEP INITIATE may be used to reinitiate the sweep cycle.

i. On A2A19 (B, fig 3-8), adjust the appropriate potentiometer (see table in step g above) for an average reading of approximately +5 V dc (+2.5 V dc if in BPSK mode) on channel 1 of the oscilloscope.

j. Set the modem MONITOR meter switch to ERROR COUNT, and the thumbwheel switches to 0.

k. With the Modem Test Set TS-3580/G connected to the modem (modem test set INPUT and OUTPUT connectors to modem ATIJ1 and AT2J1, respectively, perform the Eb/No test at the operating frequency and at the operational signal-to-noise level Compare the measured error rate with the theoretical bit error rate of figure 3-20; the measured bit error rate shall be no greater than the maximum allowable bit error rate shown in figure 3-20. If the error rate is within tolerance, return the modem to service. If the error rate is not within tolerance, perform the complete receive bit synchronizer alinement (para 3-22)

3-34. Timing and AGC (A2A30, A2A31), Abbreviated Alinement

NOTE

The following adjustments are required only if the modem is operating at 1 MB/S or higher 3-44

a. Turn DL1 and DL2 fully counterclockwise.

b. Connect the oscilloscope lead to the top of R1 (junction of R1 and U5-1) on A2A30/A2A31 (fig. 3-13).

c. Adjust A2A30/A2A31 R4 (fig. 3-13) for 400 + 100 mV dc as read on the oscilloscope.

d. Move the oscilloscope lead from R1 to top of A2A30/A2A31-R18 (junction R18 and U1-12) fig. 3-13).

e. Adjust A2A30/A2A31-R19 for 400 +100 mV dc as read on the oscilloscope.

f. Set the modem MODE switch to LINK.

g. Connect the Modem Test Set TS-3580/G to the modem (modem test set INPUT and OUTPUT connectors to modem AT1Jl and AT2J1, respectively). Perform the Eb/No test at the operating frequency and at 11 dB. Compare the measured error rate with the theoretical bit error rate of figure 3-30; the measured bit error rate shall be no greater than the maximum allowable bit error rate shown in figure 3-20.

h. Set the modem MONITOR switch to ERROR COUNT and thumbwheel switch to 0.

i. Adjust A2A30/A2A31-DL1 for a minimum reading on the modem MONITOR meter.

j. Connect the Modem Test Set TS-3580/G to the modem (modem test set INPUT and OUTPUT connectors to modem AT1Jl and AT2J1, respectively. Perform the E /N test at the operating frequency and at the operational signal-to-noise level. Compare the ' measured error rate with the theoretical bit error rate of figure 3-20; the measured bit error rate shall be shown in figure 3-20. If the error rate is within tolerance, return the modem to service If the error rate is not within tolerance, perform the complete receive bit synchronizer alinement (para. 3-22)

3-35. Phase Control Integrator A2A34, Abbreviated Alinement

a. Disconnect the external cables from AT1J1 and AT2J1 (located on rear panel).

b. Set the modem controls as shown in table 3-39 except set TRANSMIT INPUT DATA RATE to 1.2 MB/S Set the POWER switch to ON.

c. Place A2A34 on a card extender.

d. While using an oscilloscope to monitor pin 11 of AR6 on A2A34 (fig. 3-14), adjust R31 on A2A34 as required to reduce the dc voltage offset at AR611 to 0 ± 10 mV dc

e. While using an oscilloscope to monitor pin 11 of AR7 on A2A34 (fig. 3-14), adjust R35 on A2A34 as required to reduce the dc voltage offset at AR7-11 to 0 ± 10 mV de.

f. Monitor the junction between C31 and C32 on A2A4 (fig 3-15) with an oscilloscope and, if necessary, adjust R15 on A2A34 to reduce the dc offset to 0 + 20 mV dc. If this level cannot be ob-

tained, readjust R31 on A2A34 slightly to reduce the dc voltage offset to 0 + 20 mV dc

g. Monitor pin 21 of A2A34 with one channel of the oscilloscope. Adjust R14 and R22 of A2A34 (fig. 3-14) to maximize the amplitude of the waveform peaks The two resistors, R14 and R22, will each control the magnitude of alternate waveform peaks. Then, adjust the resistor controlling the largest peaks to reduce their amplitude until they equal the amplitude of the peaks controlled by the other resistor.

NOTE

If operating below 1.2 MB/S, perform steps 1, m, and n below. If operating above 1.2 MB/S, perform the following.

h. While monitoring pin 21 of A2A34 with an oscilloscope, adjust C18 and C20 of A2A34 (fig. 3-14) to maximize the amplitude of the waveform peaks The two capacitors, C18 and C20, will each control the amplitude of alternate waveform peaks Then, readjust the capacitor controlling the largest peaks to reduce their amplitude until they equal the amplitude of the peaks controlled by the other capacitor.

i. While continuing to monitor pin 21 of A2A34, adjust C32 on A2A34 (fig. 3-14) to minimize the amplitude of the waveform between adjacent peaks

j. Set the MONITOR ERROR COUNT thumbwheel switch to position 14 in order to monitor the Q channel LSB on the front panel MONITOR meter.

k. On the second timing and AGC card, A2A30, adjust the data delay line, DL1 (fig. 3-13) until the MONITOR meter reading is at a minimum (should read less than 10 when adjustment is complete)

l. Set the modem TRANSMIT INPUT DATA RATE switches to the operating frequency

m. Set the modem MONITOR meter switch to ERROR COUNT, and the thumbwheel switches to 0

n. Connect the Modem Test Set TS-3580/G to the modem (modem test set INPUT and OUTPUT connectors to modem ATlJ1 and AT2J1, respectively) Perform the Eb/No test at the operating frequency and at the operational signal-to-noise level. Compare the measured error rate with the theoretical bit error rate of figure 3-20, the measured bit error rate shall be no greater than the maximum allowable bit error rate shown in figure 3-20. If the error rate is within tolerance, return the modem to service. If the error rate is not within tolerance, perform the complete receive bit synchronizer alinement (para. 3-22).

3-36. Stable Clock (A3A39), Abbreviated Alinement

a. Set the modem MODE switch to TEST

b. Place A3A39 on a card extender

c. Connect the oscilloscope lead to pin 8 of A3A39-U2 (fig 3-4)

d. Adjust A3A39-R37 for 600 ±20 mV dc (as read on the oscilloscope).

e. Connect the counter to the modem TEST OUTPUT CLOCK connector on the front panel

f. Set the modem MONITOR switch to ERROR COUNT and the thumbwheel switch to 1 The counter should indicate the frequency as set on TRANSMIT INPUT DATA RATE switches (+1 count) If the frequency reading is within limits, return the modem to operation. If not, perform the complete stable clock adjustment (para 3-13).

3-37. Removal and Replacement Procedures

NOTE

After removing and replacing any of the following parts, cover all solder connections, that are at a potential of 115 V ac, with Dow Corning 3145 RTV rubber compound.

a. Indicators Remove retaining nut and extract indicator by pulling straight out. Replace with like item

b Power Indicator Unscrew the jewel lens, remove the neon lamp, and install replacement lamp

c. Toggle Switches. Remove the leads to the switch with a screwdriver Remove the retaining nut Withdraw the switch and replace with a like replacement

d. Rotary Switches Unsolder the leads to the switch. Remove the knob with an allen wrench Remove the retaining nut and withdraw the switch Install replacement switch. Cover solder connections of the MODE switch with compound, Dow Corning 3145 RTV.

e. Thumbwheel Switch Subassembly (A1A1 or A1A2) Disconnect the cable connector Remove the four screws from the front panel. Remove the subassembly from the back of the front panel. Install replacement subassembly

f. Alarm Buzzer Remove the leads with a screwdriver. Remove the retaining nut. Remove the buzzer and install replacement buzzer

g. MONITOR Meter Tag leads and remove by removing securing nuts Remove the four nuts that hold the meter In place Install replacement meter and reconnect leads.

h. Oscillators. Disconnect cable connector Remove screws holding oscillator and retaining bracket in place Remove assembly and install replacement oscillator

i. Power Supply

(1) With modem top cover removed, disconnect the ac power cable connector A1P1 from A1PS1J1 and

the dc connector AIPSlP1 from A2J7 on the top file (fig. 3-22). Remove four phillips head screws (A, fig. 3-19). With the modem bottom cover removed, disconnect dc connector A1PSlP2 from A3J9 on the bottom file. Remove two lower phillips head screws from each side near bottom of the modem (B, fig. 3-19). Extract power supply with attached mounting brackets from bottom of modem.

(2) To replace the power supply, attach mounting brackets to replacement power supply and reverse the procedures of (1) above. Leave screws untightened and ensure that the mounting brackets are flush with the bottom sides of the modem; then tighten screws.

j. Printed Circuit Cards. Use card puller, type Protolab 7920 or 423678, to extract printed circuit cards. Attach card puller to card and squeeze the extracting lever. To replace the card, aline the connector properly and press the card into place.

k. Printed Circuit Card File. Remove the screws which hold the file in place. Remove all cable connectors. Lift out the card file.

l. Blowers. Remove the 115 V ac cover from the rear of the modem chassis. Tag and unsolder the leads. Remove the four screws which hold the fan assembly in place. Remove the fan and install replacement
blower. Reconnect leads.

Section IV. PERFORMANCE TEST PROCEDURES

3-38. Performance Testing

a. General. The procedures of this section provide a means of evaluating the bit error rate performance of the QPSK/BPSK modem under various conditions. In the event of a test failure or marginal indication, refer to performance failure analysis, paragraph 3-39.

b. Test Procedure

(1) Set front panel controls as shown in table 3-40.

(2) Connect the Modem Test Set TS-3580/G to the modem 70 MHz interface connectors, AT1Jl and AT2J1

(3) Connect the TS-3641/G (Harris Model 7002), TS-3642(V)1/G (Harris Model 7003), or the frequency counter to TEST OUTPUTS ERROR connector on the modem front panel to measure the error rate.

(4) Using the Modem Test Set TS-3580/G, measure the bit error rate for Eb/No settings of 3, 5, 7, 9, and 11 5 dB. Verify that the measured results are within the limits shown on figure 3-20.

EST PROCEDURES

NOTE

If time permits, also perform noise tests at RECEIVE I CHANNEL SYMBOL RATES within the following ranges;
1) 25 000 KB/S to 37.999 KB/S,
2) 38.000 KB/S to 74.999 KB/S,
3) 75.000 KB/S to 149.99 KB/S,
4) 150.000 KB/S to 629.99 KB/S,
5) 630.00 KB/S to 2.4999 MB/S,
6) 2.5000 MB/S to 4.9999 MB/S
This action tests the modem performance within each of the six QPSK demodulator rate ranges. Similarly, the modem performance for the BPSK mode can be tested by performing noise tests at RECEIVE I CHANNEL SYMBOL RATES within the following ranges:
1) 16.000 KB/S to 37.999 KB/S,
2) 38.000 KB/S to 74.999 KB/S,
3) 75 000 KB/S to 149.99 KB/S,
4) 150.00 KB/S to 249.99 KB/S,
5) 250.00 KB/S to 629.99 KB/S,
6) 630.00 KB/S to 2.4999 MB/S,
7) 2.5000 MB/S to 9.9999 MB/S.

Table 3-40. Initial Control Settings for Performance Testing

Control	Position
ALARM RESET/OFF/ON	OFF
MODE	LINK
TRANSMIT INPUT DATA RATE	Same as operational RECEIVE I CHANNEL SYMBOL RATE for BPSK Twice operational I RECEIVE CHANNEL SYMBOL RATE for QPSK
TRANSMIT QPSK/BPSK	Same as operational setting of RECEIVE QPSK/BPSK switch
TRANSMIT ENCODER DIFF/OFF	DIFF
TRANSMIT ENCODER EXT/OFF	OFF
RECEIVE I CHANNEL SYMBOL RATE	Same as operational setting
RECEIVE QPSK/BPSK	Same as operational setting
RECEIVE DECODER DIFF/OFF	DIFF
RECEIVE DECODER EXT/OFF	OFF
MONITOR meter switch	ERROR COUNT
MONITOR ERROR COUNT	0
RANDOMIZER TRANSMIT	OFF
RANDOMIZER RECEIVE	OFF

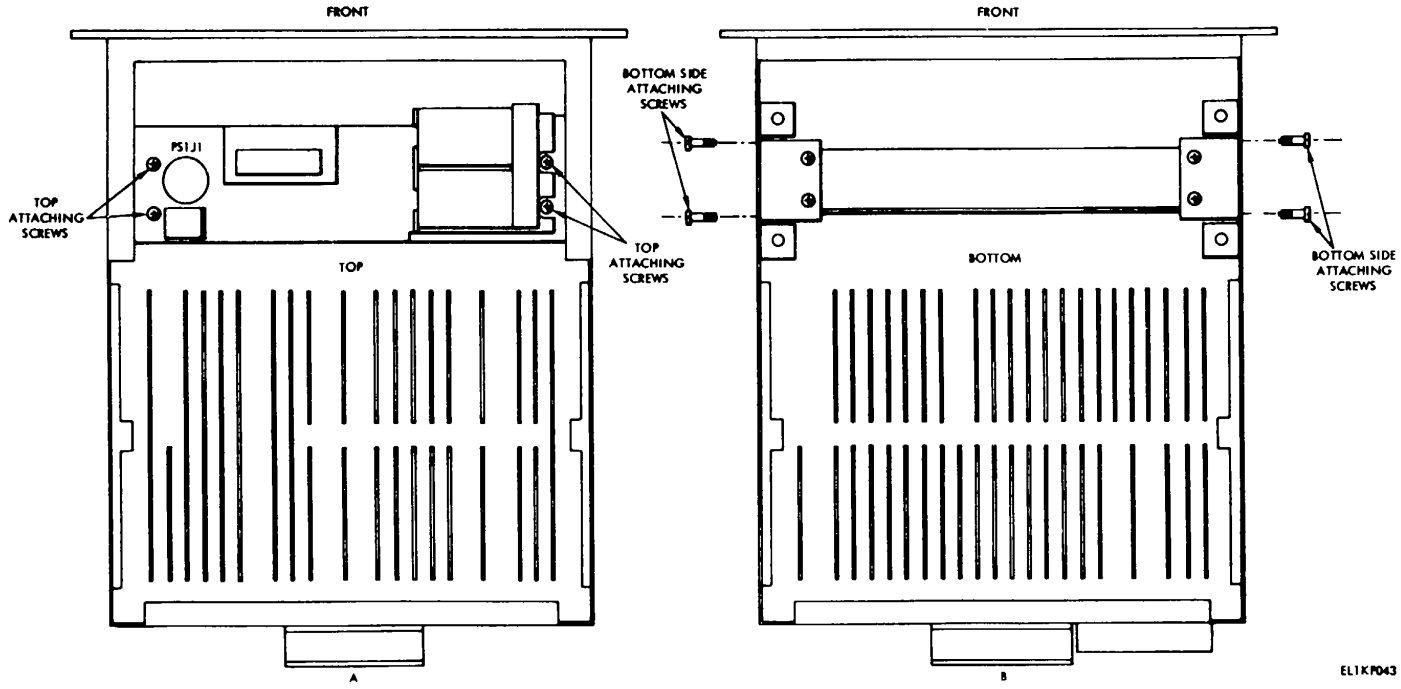


Figure 3-19. Power supply removal and replacement

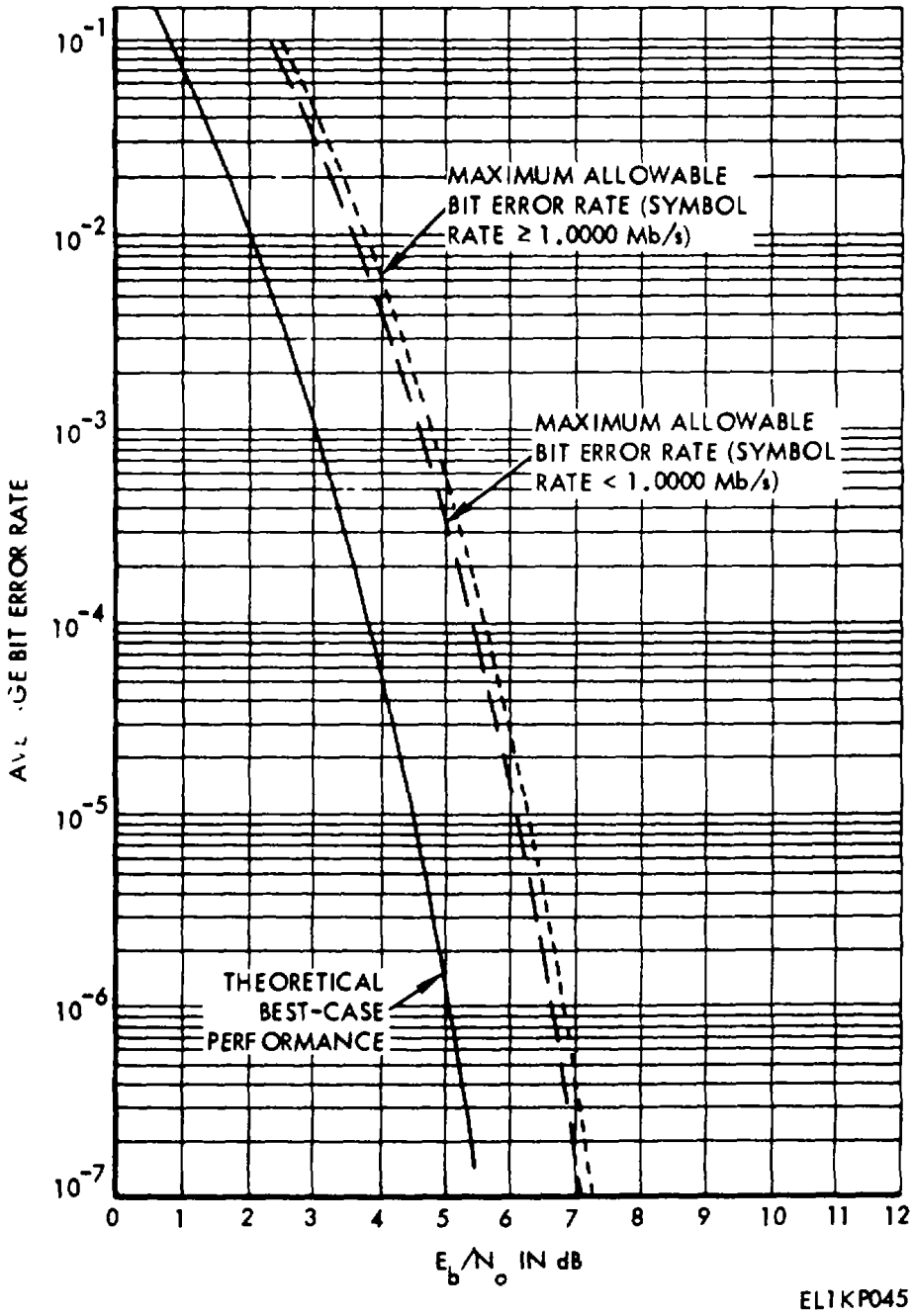


Figure 3-20. QPSK/BPSK modem bit error rate performance for differential coding and no error-correcting coding.

(5) If receive error coding is used in normal operation, the modem performance with coding can also be tested using the noise test procedure (step (4) above). To accomplish this, the TRANSMIT and RECEIVE EXT/OFF switches must both be placed in the EXT position. The TRANSMIT INPUT DATA RATE switches must also be changed to account for the coder processing. This means that when the modem is in the BPSK mode, the TRANSMIT INPUT DATA RATE setting will be half of the RECEIVE I CHANNEL SYMBOL RATE setting. If the modem is in the QPSK mode, the TRANSMIT INPUT DATA RATE setting will equal the RECEIVE I CHANNEL SYMBOL RATE setting. The procedure then is to measure the bit error rate for E_b/No settings of 8, 4, and 5.5 dB. Verify that the measured results are within the limits shown on figure 3-21.

(6) Although normal modem operation in the

QPSK mode may require the use of the randomizer circuits, the actual bit error rate performance of the modem is measured with the RANDOMIZER TRANSMIT and RECEIVE switches in the OFF position, as specified in table 3-40. When these switches are on during a noise test, the indicated bit error rate is two times the true bit error rate. Therefore, the RANDOMIZER TRANSMIT and RECEIVE switches are maintained in the OFF position when verifying that the modem is operating within performance limits. After verification of performance in accordance with step (4) or (5) above, the two switches may be placed in the ON position and the noise test procedure repeated for the expected increase in indicated error rate.

3-39. Performance Failure Analysis

a. General. Failure to attain the required bit error rate performance requires that additional checks and analysis be made to determine the cause of failure. Some of the functional areas within the modem are rate sensitive; i.e., different circuits are used at various data rates Therefore, the range of data rates for which the modem performance is degraded may provide an indication of the probable functional area that is causing the failure Tables 3-41, 3-42, and 3-43 list the data rate breakpoints associated with the frequency synthesizers, modulator, and demodulator, respectively. In many cases, adjustment or alinement of the functional area causing performance degradation is sufficient to restore proper

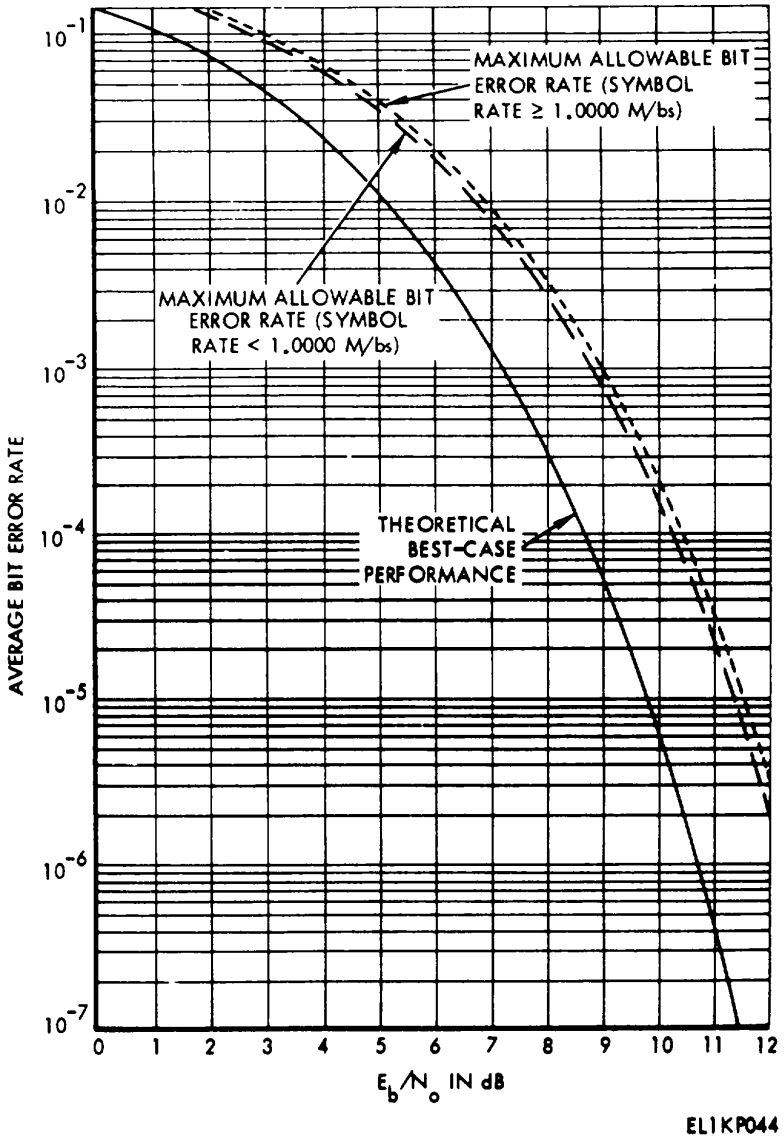


Figure 3-21. QPSK/BPSK modem bit error rate performance for differential coding and external (KY-801/GSC (Viterbi) soft decision, K = 7) error-correccting

performance. Therefore, appropriate adjustment procedures are referenced for many failure symptoms. Each adjustment procedure is prefaced with a note that indicates the probable malfunctioning subassembly if specified adjustments cannot be accomplished. Subparagraphs b through g below provide a narrative description of the checks and analysis to be made. Trouble symptoms, probable causes for failure, and recommended corrective action are summarized in table 3-44. Replacement of _ certain cards requires the checking of the alinement, refer to table 3-31 for the alinement paragraph references.

Table 3-41. Frequency Synthesizer Rate Breakpoints

Range	Transmit Input Data Rate and Receive I Channel Symbol Rate thumbwheel switch setting
1	16.000 KB/S to 24 999 KB/S
2	25.000 KB/S to 49 999 KB/S
3	50 000 KB/S to 99 999 KB/S
4	100 00 KB/S to 124 99 KB/S
5	125 00 KB/S to 249 99 KB/S
6	250.00 KB/S to 499 99 KB/S
7	500.00 KB/S to 999 99 KB/S
8	1 0000 MB/S to 1 2499 MB/S
9	1 2500 MB/S to 2.499 MB/S
10	2 5000 MB/S to 4 9999 MB/S
11	5 0000 MB/S to 9 9999 MB/S

Table 3-42. Modulator Data Rate Breakpoints

Conditions	Transmit Input Data Rate thumbwheel switch setting
BPSK (without EXT coding)	16.000 KB/S to 999 99 KB/S
	1 0000 MB/S to 2 4999 MB/S
	2 5000 MB/S to 9 9999 MB/S
BPSK (with EXT coding)	16 000 KB/S to 499 99 KB/S
	500 00 KB/S to 1 2499 MB/S
	1 2500 MB/S to 4 9999 MB/S
QPSK (without EXT coding)	50 000 KB/S to 1 2499 MB/S
	1 2500 MB/S to 4 9999 MB/S
	5 0000 MB/S to 9 9999 MB/S
QPSK (with EXT coding)	50 000 KB/S to 499 99 KB/S
	500 00 KB/S to 2 4999 MB/S
	2 5000 MB/S to 9 9999 MB/S

Table 3-43. Demodulator and Receive Bit Synchronizer Rate Breakpoints

Functional Area	BPSK RECEIVE I CHANNEL SYMBOL RATE breakpoints	QPSK RECEIVE I CHANNEL SYMBOL RATE breakpoints
Demodulator	16 000 KB/S to 37 999 KB/S	25 000 KB/S to 37 999 KB/S
	38 000 KB/S to 74 999 KB/S	38.000 KB/S to 74 999 KB/S
	75 000 KB/S to 149 99 KB/S	75 000 KB/S to 149 99 KB/S
	150 00 KB/S to 249 99 KB/S	150 00 KB/S to 629 99 KB/S
	250 00 KB/S to 629 99 KB/S	630 00 KB/S to 2 4999 MB/S
	630 00 KB/S to 2 4999 MB/S	2 5000 MB/S to 9 9999 MB/S
	2 5000 MB/S to 9.9999 MB/S	
Receive bit synchronizer	16 000 KB/S to 159 99 KB/S	25 000 KB/S to 159 99 KB/S
	160.00 KB/S to 1 2799 MB/S	160 00 KB/S to 1 2799 MB/S
	1 2800 MB/S to 9.9999 MB/S	1.2800 MB/S to 9 9999 MB/S

Table 3-44. Performance Test Failure Symptoms, Probable Causes, and Corrective Actions

Symptom	Probable cause of failure	Corrective action
1 Performance is within tolerance in one or more demodulator rate ranges but is out of tolerance in others	*a.* Demodulator phase controls not properly adjusted	*a* Perform applicable portions of the demodulator phase adjustment (para 3−21)
	b Card failure	*b* Replace card(s) in the following order A2A14 A2A18 A3A32

Table 3-44. Performance Test Failure Symptoms, Probable Causes, and Corrective Actions-Continued

Symptom	Probable cause of failure	Corrective action
2. Performance gradually degrades as data rate Is increased over the range of 10000 MB/S to 9.9999 MB/S and cannot be corrected, by demodulator phase adjustment	a. Receive bit synchronizer not properly alined	a. Perform receive bit synchronizer alinement per paragraph 3-22
	b. If in BPSK mode, take corrective action	b Replace card(s) in the following order A2A12 A2A10 A2A8 A2A9
	c If in QPSK mode, halve the TRANSMIT INPUT DATA RATE and place the MONITOR ERROR COUNT switch in positions 8 and 9 to isolate the problem to the I or Q channel	
	(1) If trouble Is in I channel, take corrective action c (1)	(1) Replace card(s) in the following order A2A12 A2A10 A2A8 A2A9
	(2) If trouble is in Q channel, take corrective action c(2)	(2) Replace card(s) in the following order A2A36 A2A34 A2A32 A2A33
3 Performance is out of tolerance at all rate ranges	a. Demodulator gain not properly adjusted	a. Perform demodulator AGC level adjustment per paragraph 3-17 If output cannot be properly adjusted, proceed to corrective action step b below
	b. Receive bit synchronizer gain not properly adjusted	b Perform receive bit synchronizer AGC alinement (para 3-23) If output cannot be properly adjusted, proceed to step c below
	c. Receive bit synchronizer timing not properly adjusted	c. Perform receive bit synchronizer alinement (para 3-22) If output cannot be properly adjusted, proceed to step d below
	d Card failure	d. If In BPSK mode, take corrective action e below If In QPSK mode, halve the TRANSMIT INPUT DATA RATE and place the MONITOR ERROR COUNT switch in positions 8 and 9 to isolate the problem to the I or Q channel If in the I channel, take corrective action e below If in the Q channel, take corrective action below
	e. Card failure in I channel	e. Replace card(s) in the following order A2A12 A2A10 A2A8 A2A9
	f. Card failure in Q channel	f. Replace card(s) in the following order A2A36 A2A34 A2A32 A2A33
4. Major differences in performance observed on either side of receive bit synchronizer breakpoints below	a. Receive bit synchronizer timing not properly adjusted	a. Perform receive bit synchronizer alinement (para 3-22) If output cannot be properly adjusted, proceed to step b
	b. Card failure	b. If In BPSK mode, take corrective action c below If In QPSK mode, halve the TRANSMIT INPUT DATA RATE and

Table 3-44. Performance Test Failure Symptoms, Probable Causes, and Corrective Actions-Continued

Symptom	Probable cause of failure	Corrective action
4. Major differences In performance observed on either side of receive bit synchronizer breakpoints -Continued		place the MONITOR ERROR COUNT switch in positions 8 and 9 to isolate the problem to the I or Q channel. If in the I channel, take corrective action c below. If in the Q channel, take corrective action d below
	c. Card failure In 1 channel	c. Replace card(s) in the following order A2A10 A3A32
	d. Card failure In Q channel	d. Replace card A2A34
5. TEST OUTPUTS CLOCK frequency not within +1 least significant digit when operating in self-test, MONITOR ERROR COUNT switch position 1.	a. Stable clock circuits not properly adjusted	a. Perform stable-clock adjustment per paragraph 3-13. If output cannot be properly adjusted, proceed to step b Below.
	b. Card failure	b. Replace card(s) in the following order A3A41 A3A43 A3A38 A3A29 A3A42
6. TEST OUTPUTS CLOCK frequency not within +1 least significant digit when operating in self-test, MONITOR ERROR COUNT switch position 2	a. Transmit frequency synthesizer not prop erly alined	a Perform transmit frequency synthesizer alinement per paragraph 3-14 If output cannot be properly adjusted proceed to step b below
	b. Card failure	b. Replace card(s) In the following order A3A42 A3A35 A3A36 A3A37
7. TEST OUTPUTS CLOCK frequency not within $\pm$1 least significant digit %hen operating in self-test, ERROR COUNT switch position 3	a Receive frequency synthesizer not properly alined MONITOR to step b below	a Perform receive frequency synthesizer alinement per paragraph 3-15. If output cannot be properly adjusted, proceed
	b. Card failure	b. Replace card(s) m the following order A3A13 A3A14 A3A15 A3A18 A3A16 A3A17
8. Major differences In performance between modulator ranges	Card failure	Replace card(s) In the following order A2A26 A3A32
9. Performance in tolerance with no external coding, out of tolerance with external coding	Failure In the external coder Interface cards of the modem A3A27 S1 is in position 1 for "normal phase". If decoder. or phase is transposed, external coder/decoder (KY-801/G) indicates approx 185 errors. In which case change A3A27 switch S1 to position 2 (para 3-21f).	If soft bits are being generated (can be checked by positions 8, 9, 10, 11, 13, and 14 of the MONITOR ERROR COUNT switch), replace the external coder/ A3A28 A3A27 A3A7 A3A6 If no soft bits are being generated, replace the following card(s), A2A8 A2A32 A2A29 A3A8

Table 3-44. Performance Test Failure Symptoms, Probable Causes, and Corrective Actions-Continued

Symptom	Probable cause of failure	Corrective action
10. Performance out of tolerance using Digital Communications Test Set	a. Digital Communications Test Set failure Set b. Card failure	a. Replace Digital Communications Test b. Replace card(s) in the following order A3A5 A3A31 A3A30

b. Demodulator Tests. A common cause of degraded performance is misalinement or failure of the demodulator circuits. Operation within the various demodulator ranges checks the phase adjustment and the filters. Repeat the performance tests at bit rates within each of the demodulator ranges. If operation is within tolerance in one or more of the ranges, perform the demodulator phase adjustment in accordance with paragraph 3-21. A final check of the demodulator can be made by connecting an oscilloscope to TP1 of the data integrators A2A10 and A2A34 (fig. 3-14) to ensure that the demodulator data output is between 1.5 and 3.0 volts peak.

c. Receive Bit Synchronizer Tests. The bit synchronizer breakpoints also provide troubleshooting aids to isolate the cause of performance degradation. Repeat the noise test at symbol rates of 159.99 kb/s and 160.00 kb/s (para 3-38 b). If performance differs significantly between tests, perform bit synchronizer alinement per paragraph 3-22. If no change in performance at the above breakpoint, repeat the noise test at symbol rates of 1.2799 Mb/s and 1.2800 Mb/s (para 3-38 b). If performance differs significantly at these two rates, perform bit synchronizer alinement per paragraph 3-22.

d Frequency Synthesizer Tests. The synthesizer breakpoints are most readily checked in the self-test mode. Set the MODE switch to TEST, set the MONITOR ERROR COUNT thumbwheel switch to position 1, and connect a frequency counter to the front panel TEST OUTPUTS CLOCK connector. Set the TRANSMIT INPUT DATA RATE switches to any position within the range of 1.000 MB/S to 1.2499 MB/S, monitor the frequency counter, and verify indication is selected rate $\pm$1 least significant digit Repeat checks at rate changes of 1.2500 MB/S to 2.4999 MB/S, 2.5000 MB/S to 4.9999 MB/S, and 5.0000 MB/S to 9.9999 MB/S. If any indication is not as specified, perform the stable clock adjustment per paragraph 3-13. Change the MONITOR ERROR COUNT thumbwheel switch setting to position 2 and repeat the above frequency checks. If any indication is not as specified, perform the transmit frequency synthesizer alinement per paragraph 3-14. Change the MONITOR ERROR COUNT thumbwheel switch setting to position 3 and set both the TRANSMIT and RECEIVE QPSK/BPSK switches to BPSK. Repeat the above frequency checks by setting both the TRANSMIT INPUT DATA RATE and RECEIVE I CHANNEL SYMBOL RATE switches to a frequency setting within each of the above ranges. If any indication is not as specified, perform the receive frequency synthesizer alinement per paragraph 3-15.

e Modular Tests. Although the modulator is not usually a cause for performance test failure, tests may be made within each of the modulator data rate ranges of table 3-42 The modulator output power at ATlJ1 should also be checked to verify that it is at least $\pm$9.5 dBm.

f. Encoder/Decoder Tests A failure mode may be experienced wherein the performance test is within tolerance with no external error correction coding, but out of tolerance when external coding is employed. The probable cause of this type of failure is either the external encoder/decoder or the modem encoder interface circuits. However, before extensive card or assembly replacement is considered, a check should be made to ensure that the receive bit synchronizer is generating the soft decision bits required for external error correction decoding. This function can be verified during the performance test by switching the MONITOR ERROR COUNT thumbwheel to positions 8, 9, 10, 11, 13, and 14. In each of these six positions, both the DATA 1 and 0 lamps of the MONITOR section of the modem front panel should be illuminated to indicate that the soft decisions are being generated. If the soft decisions are not being generated, the probable failure is the applicable quantizer card or bit sync buffer card, A2A29, and test interface card, A3A8. If the soft decisions are being generated but the coded performance is out of tolerance, the failure is in either the coder/decoder itself or in the associated interface cards in the modem. See also item 9, table 3-44.

g. I/O Circuit Tests. If the performance test was conducted using Digital Communications Test Set TS-3642(V) I/G, disconnect the test set. Set MODE

switch to LINK and repeat performance testing using the internal PN sequence generator and comparator. If test results still are out of tolerance, the input and output circuits may be eliminated as the cause of failure. If performance returns to within specification, replace input or output circuit cards as required.

3-40. Assembly Location

Figures 3-22 through 3-26 are illustrations showing location of assemblies, subassemblies, and components not previously shown in this manual, and which may be used in the maintenance of the QPSK/BPSK modem.

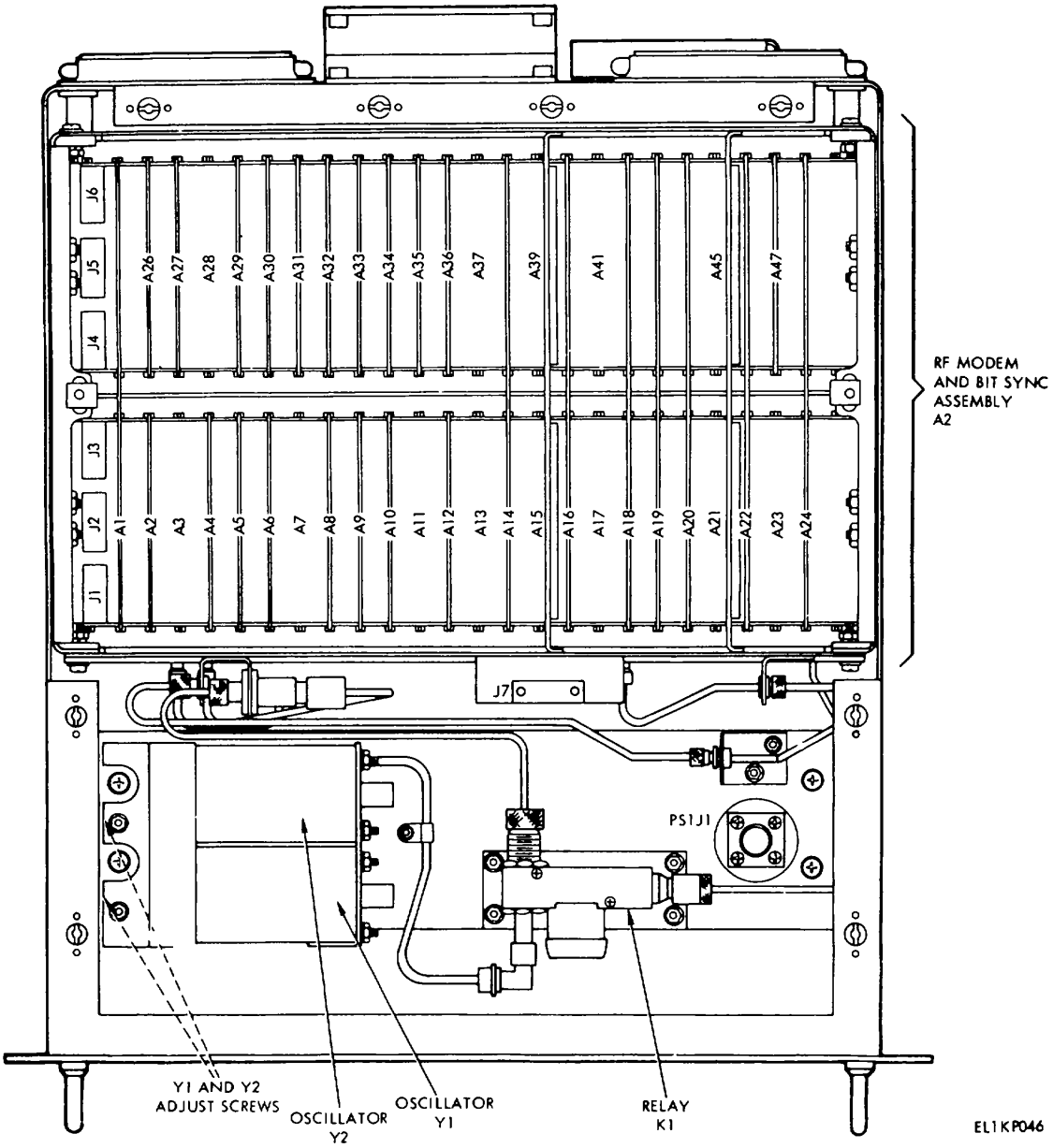
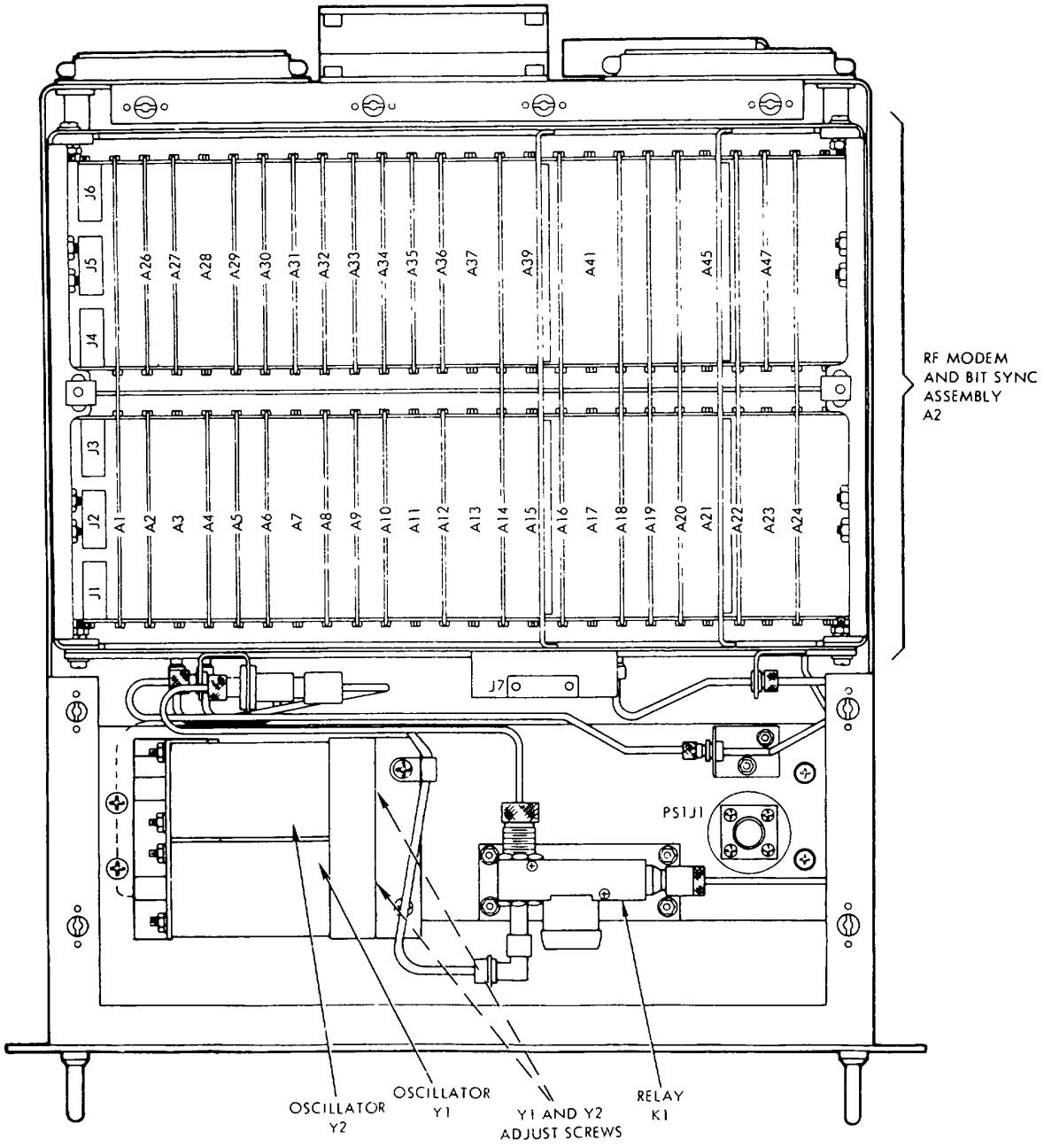


Figure 3-22. QPSK/BPSK modem, top view (top cover removed).



NOTE

UNDER CONTRACT DAAK80-79-C-0289,
OSCILLATORS Y1 AND Y2 WERE ROTATED
180 DEGREES FOR BETTER ACCESS TO ADJUSTMENTS

EL1KP141

Figure 3-22.1. QPSK/BPSK modem (Y1 and Y2 rotated), top view, top cover removed (Contract DAAK80-79-C-0289).

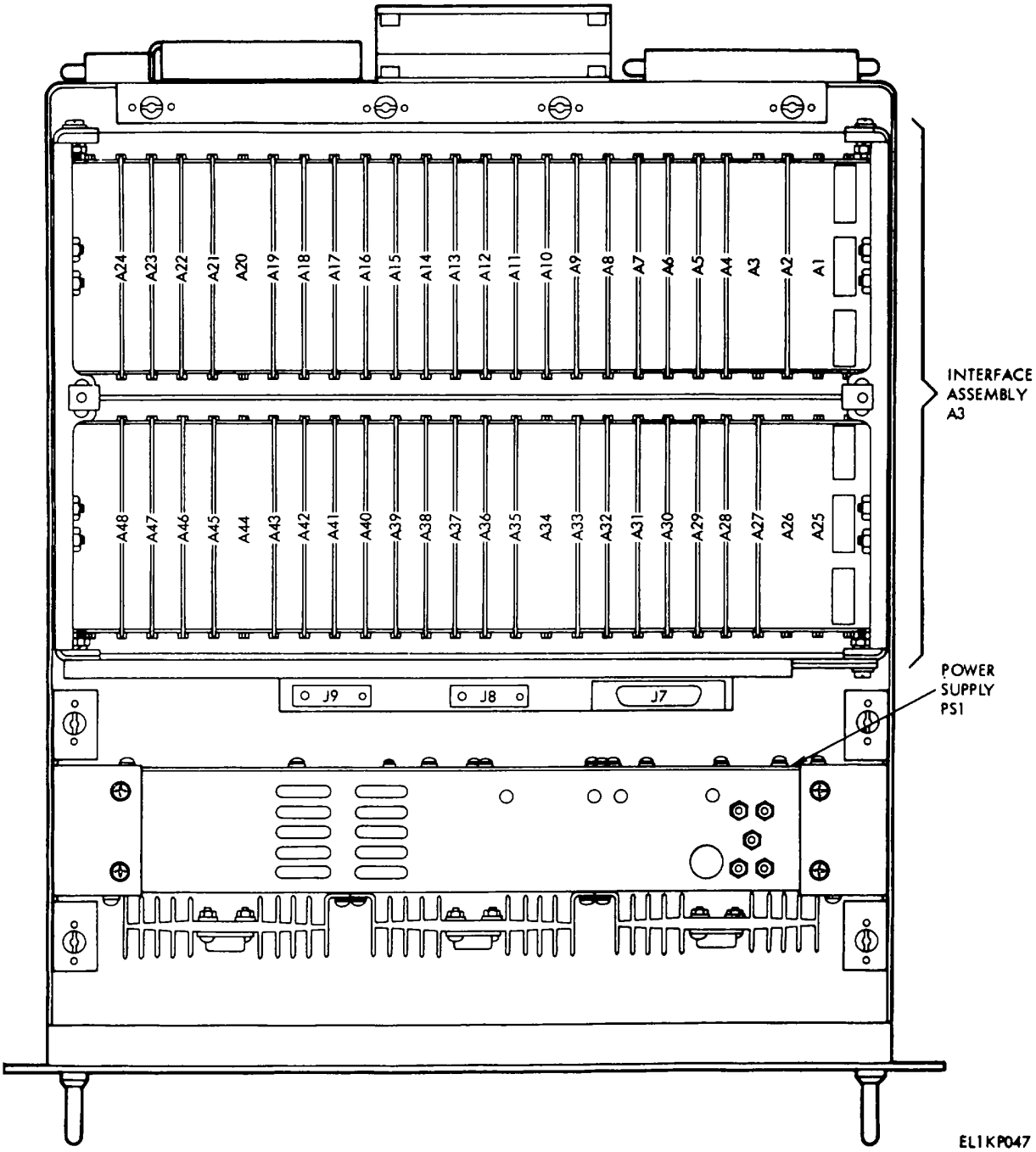


Figure 3-23. QPSK/BPSK modem, bottom view (bottom cover removed).

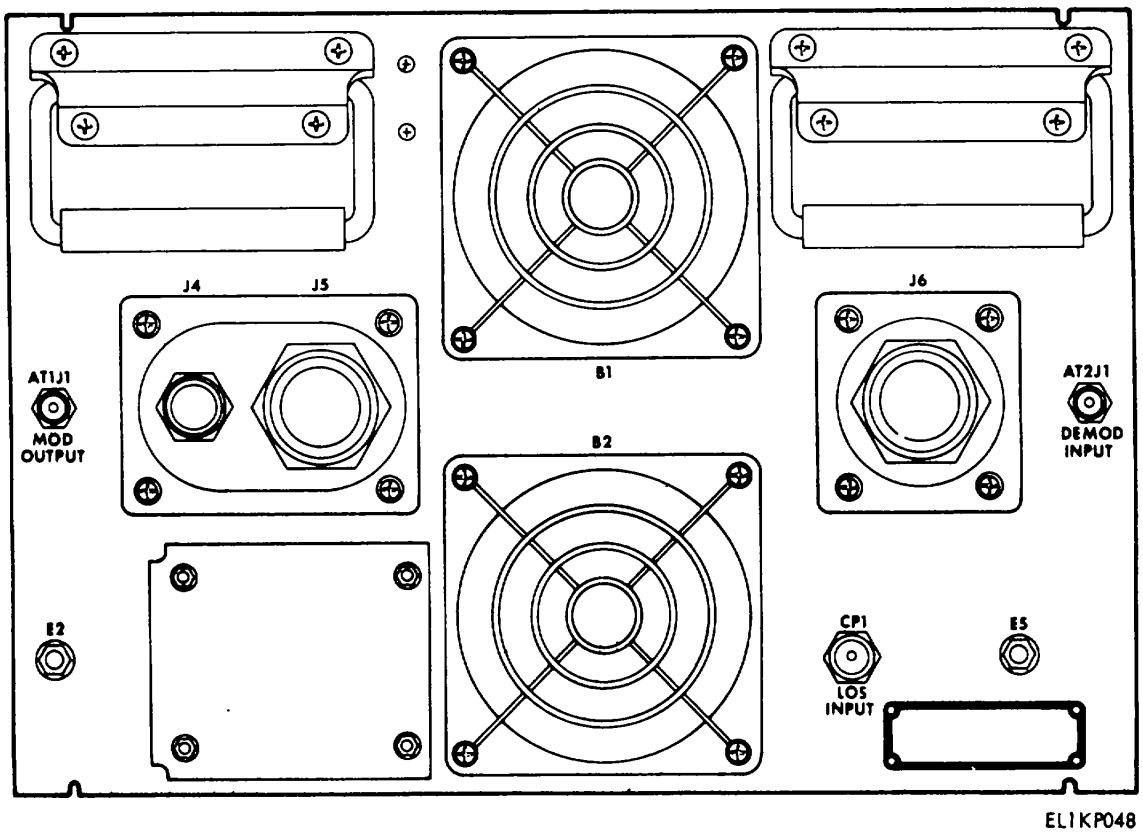


Figure 3-24. QPSK/BPSK modem, rear view.

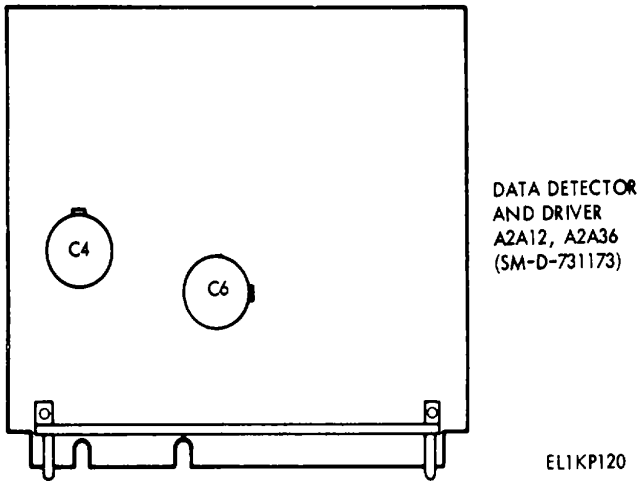


Figure 3-25. Data detector and driver, test points and adjustment locations.

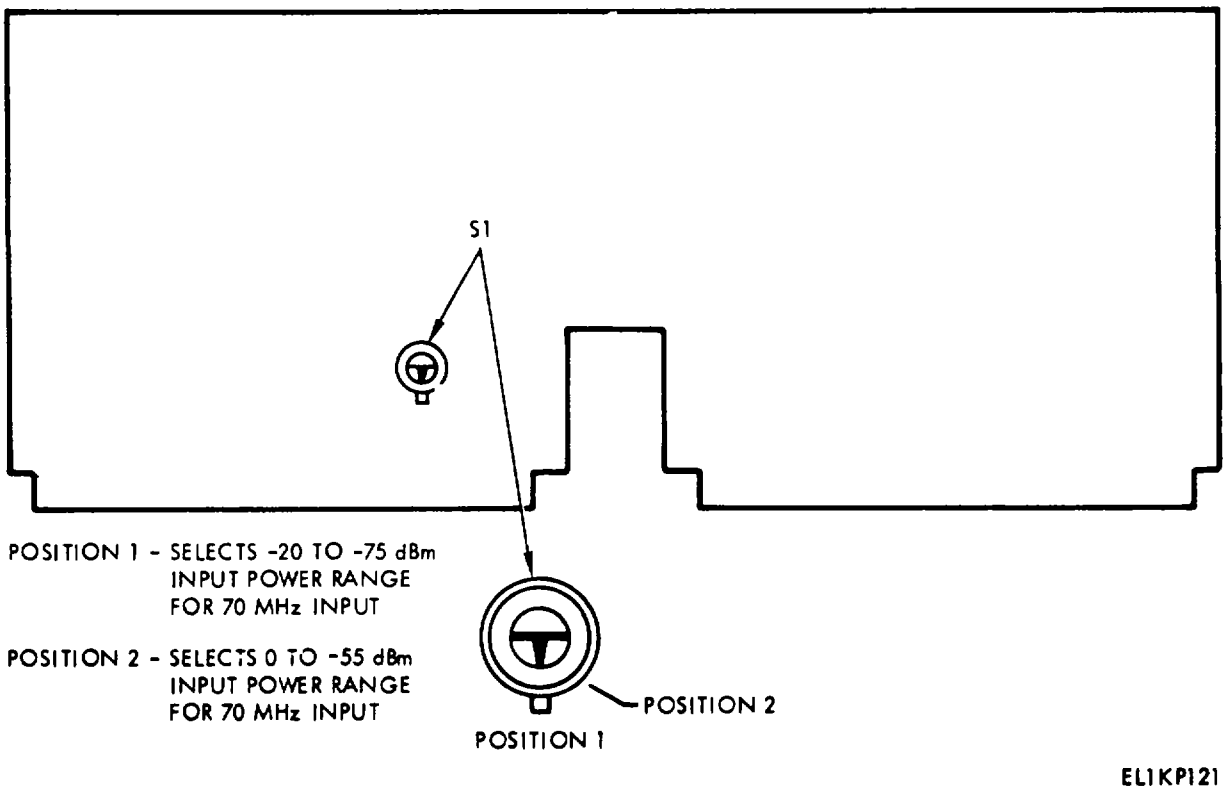


Figure 3-26. 70-MHz input range selection switch S1, 70-MHz gain control amplifier card, A2A16.

CHAPTER 4
GENERAL SUPPORT MAINTENANCE INSTRUCTIONS

4-1. Scope of General Support Maintenance

General support maintenance consists of testing, adjusting, and repairing of all repairable subassemblies of the QPSK/BPSK modem.

4-2. Tools and Test Equipment

Tools and test equipment required for general support maintenance are listed below:

a. Card Test Fixture SM-D-868407.
b. Card Test Fixture SM-D-868408.
c. Card Test Fixture SM-D-868410.
d. Card Test Fixture SM-D-868412.
e. Card Test Fixture SM-D-868416.
f. Alinement Tool JFD 52, 84.
g. Attenuator Fixture SM-D-877511 (2 required).
h. Power Supply Fixture SM-D-868418.
i. RF Power Meter, Millivac MV828A.
j. Electronic Counter AN/USM-122A with AN/GRM-32D Plug in.
k. Spectrum Analyzer IP-1216/PGR with PL-1399/U Plug In and PL-1388/U Plug In.
l. Sweep Generator, HP 8601A.
m. Digital Voltmeter, Fluke 8000A.
n. Function Generator, Wavetek 142.
o. Oscilloscope, Tektronix 485A.
p. Precision Power Supply, Power Design 4010.
q. Card Puller, Protolab 7920 and 423678.
r. Vector Voltmeter, HP 8405A.
s. 50-ohm Termination, Amphenol 35725-51 (2 required).
t. Multimeter ME-419/U.
u. 50-ohm Feed-Thru Termination TEK 011-0049-01 (2 required).
v. Tool Kit, Electronic Equipment TK-105/G.
w. Pin Extraction Tool RX20-25, Burndy.
x. Pin Extraction Tool, Teradyne, 600-0027-000.
y. Pin Insertion Tool, MS 24256A20.
z. Pin Insertion Tool, MS 24256A16.
aa. Pin Extraction Tool, MS 24256R20.
ab. Pin Extraction Tool, MS 24256R16.
ac. Pin Crimp Tool and Turret M22520-1-01 and M22520-1-02.
ad. Card Extender (2), SM-D-759649.
ae. Automatic Test System, GR-1792.
af. LTS-1 Card Test Adapter (for GR-1792).
ag. Step Attenuators, HP 355C and HP 355D.
ah. Test Set, Modem TS-3580/G.
ai. Digital Communications Test Set TS-3642(V) I/G (Harris 7003).
aj. Error Rate Counter TS-3641/G (Harris 7002).
ak. Card Test Fixture, SM-D-877827.
al. Card Test Fixture, SM-D-877832.
am. Probe (10X), Tektronix P6054A (2 required).
an. Impedance Bridge General Radio 1650B.
ao. Power Supply (500 mA), Power Design 2005A (3 required).
ap. Interface Test Unit (ITU), SM-D-877812.
aq. Pattern Adapter, SM-D-877817.
ar. Test Modulator/Phase Shifter, SM-D-877801.
as. Stopwatch (0. sec), Minerva.
at. Power Meter, Thermistor ME-441/U with coaxial thermistor mount MX-7772/U.
au. Attenuators, Fixed, 3 dB (2 each), 6 dB.
av. Extender Card, SM-D-877735.
aw. Reflection Transmission Kit, HP 11652A.
ax. Test Set, Triple Attenuator SM-D-877809.
ay. RF Filter, 4 MHz BW (Fo70MHz).
az. Power Supply-Oscillator Test Fixture, SM-D-882197.
ba. Autotransformer, Variac W50M.
bb. AN/GSC-24 Simulator.
bc. Power Supply, QPSK/BPSK, SM-C-742003.
bd. AC Voltmeter, HP 400F.
be. Test Set, ACDC 66-991-000.

4-3. Procedures

Procedures for PSK modem subassembly test, adjustment, and repair are provided in DMWR 11-5820-847.

CHAPTER 5
QPSK/BPSK MODEM POWER SUPPLY DESCRIPTION AND MAINTENANCE INSTRUCTIONS

Section I. GENERAL DESCRIPTION

5-1. General

This chapter contains descriptive information and maintenance procedures for power supply PS1, which provides all the dc power requirements for the QPSK/BPSK modem. This section describes the physical and electrical characteristics and identifies the constituent subassemblies of the power supply. Section II gives a detailed explanation of circuit operation. Direct support troubleshooting and maintenance instructions are provided in section III.

5-2. Physical Characteristics

The power supply (fig. 5-1) is physically comprised of a metal chassis that contains most of the electronics, and three heat-sink assemblies that are attached to one side of the metal chassis. The dimensions of the metal chassis are 8 x 15 x 2.5 inches, and the complete assembly, including the heat sinks, weighs 16 pounds. Input power to the supply is furnished via an external cable that connects to chassis mounted jack J1 (fig. 5-2). Outputs from the power supply are routed through

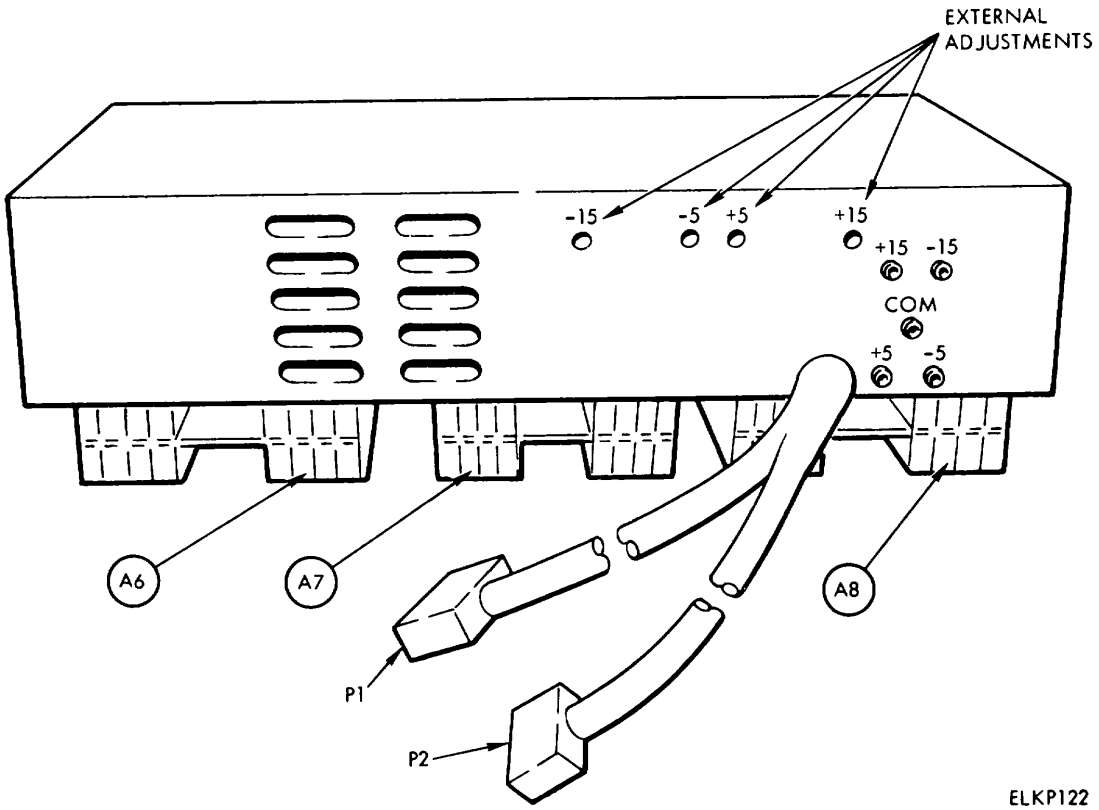


Figure 5-1. Power supply PS1, external view.

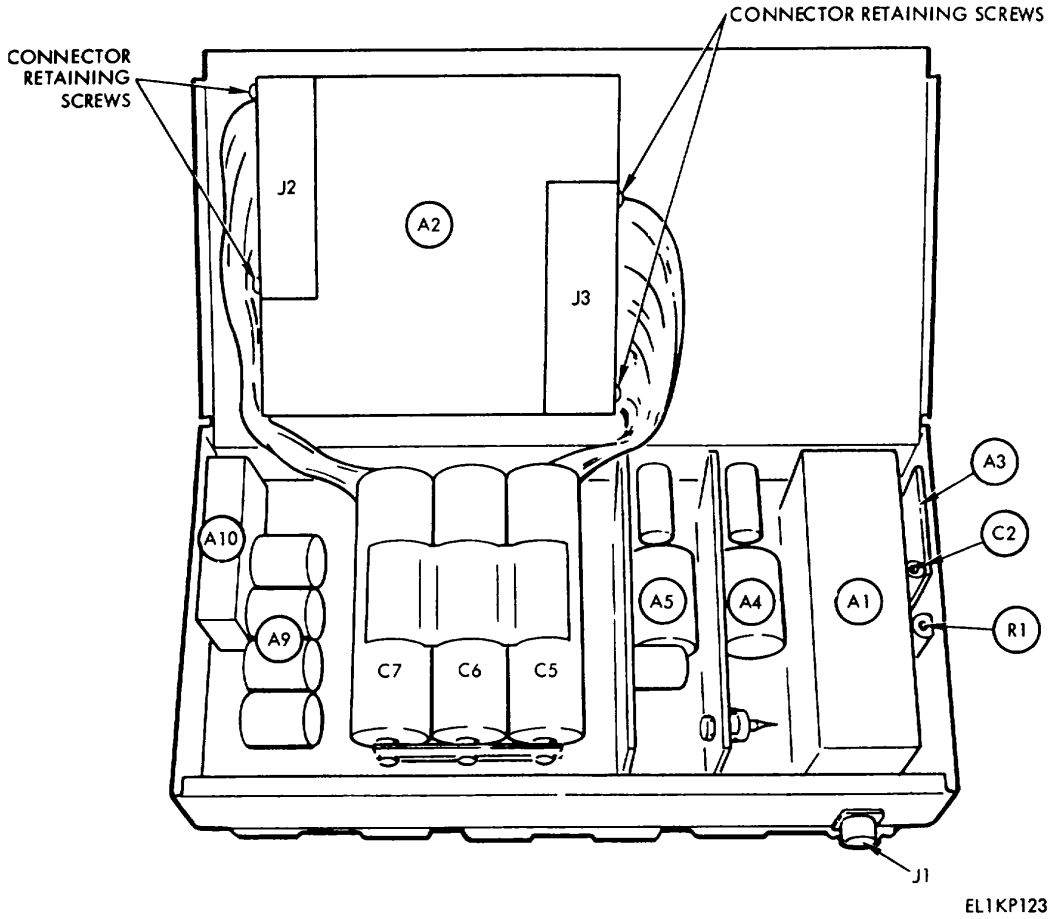


Figure 5-2. Power supply, top view with top cover open.

two cables, approximately 20 inches and 15 inches long, that are terminated in plugs P1 and P2, respectively. These output plugs connect to jacks (A2J7 and A3J9) located on the sides of the QPSK/BPSK modem card files. External test points are provided on the power supply for monitoring the dc outputs, and access ports are available to allow screwdriver adjustment of individual output voltages. The ten major subassemblies (figs. 5-1 and 5-2) of the power supply are listed below with their associated reference designators.

a. Transformer assembly, A1.
b. Printed circuit board, A2 (voltage regulator).
c. Circuit card assembly, A3 (starter circuit).
d. Component board assembly number 1, A4.
e. Component board assembly number 2, A5.
f. Heat sink assembly number 1, A6.
g. Heat sink assembly number 2, A7.
h. Heat sink assembly number 3, AS.
i. Terminal board assembly, A9 (filter capacitors).
j. SCR assembly, A10 (SCR overvoltage crowbars).

5-3. Electrical Characteristics

The power supply converts input line power to the regulated de operating levels required by the QPSK/BPSK modem. The dc output levels are +5, -5, +15, and -15 volts dc. The power supply is forced-air cooled and features overload and short-circuit protection circuitry. Refer to table 5-1 for a tabulation of performance characteristics.

Table 5-1. Performance Characteristics

Parameter	Characteristic
Ac input	120 volts ac +10%, 45 to 420 Hz, single phase
Dc outputs	+ 15 volts dc at 7 amps -15 volts dc at 5 amps +5 volts dc at 21 amps -5 volts dc at 5 amps
Output regulation Line and load	Less than +0 1%for line input variation from 108 to 132 volts ac and loads of 10% to 90%.
Ripple and noise	10 mV rms, 1 0 volt peak-to-peak
Overvoltage trip	
+5 and -5 volts de outputs	6 to 7 volts dc.
+ 16 and -15 volts dc outputs	17 to 18 volts de.
Current limit:	
+5 volts dc output	24 to 26 amps
-5 volts dc output	5 8 to 6 3 amps
+15 volts dc output	8 0 to 8.8 amps
-15 volts dc output	5 8 to 6 3 amps.

Section II. FUNCTIONAL DESCRIPTION

5-4. General

This section describes the operation of power supply circuits. A functional block diagram description is followed by a detailed discussion of each functional circuit in the power supply.

5-5. Block Diagram Description

a. The power supply functionally consists of an input transient suppressor, a bridge rectifier and capacitor filter, two dc-to-dc converters, and four output voltage regulators (fig. 5-3). The ac input to the power supply is routed through a transient suppressor, which absorbs short-duration transients on the input line. The output of the transient suppressor is then rectified and filtered to produce a voltage level containing ripple at twice the frequency of the input source. This voltage level is fed to two dc-to-dc converters where it is chopped to produce a square wave that is that is subsequently rectified and filtered to generate true dc levels. Each dc-to-dc converter drives two series regulators that provide the plus and minus dc .outputs required by the modem. The voltage regulators maintain constant output levels regardless of fluctuations in source voltage, output loading, and temperature.

b. Included in the power supply is a starter circuit that has no affect on power supply operation. This starter circuit is used in the initial checkout of the power supply by the manufacturer, and is bypassed by the addition of a jumper prior to final test and shipment.

WARNING

The bridge rectifier and capacitor filter perform full wave rectification of the ac input without using an input isolation transformer, and the dc output from the

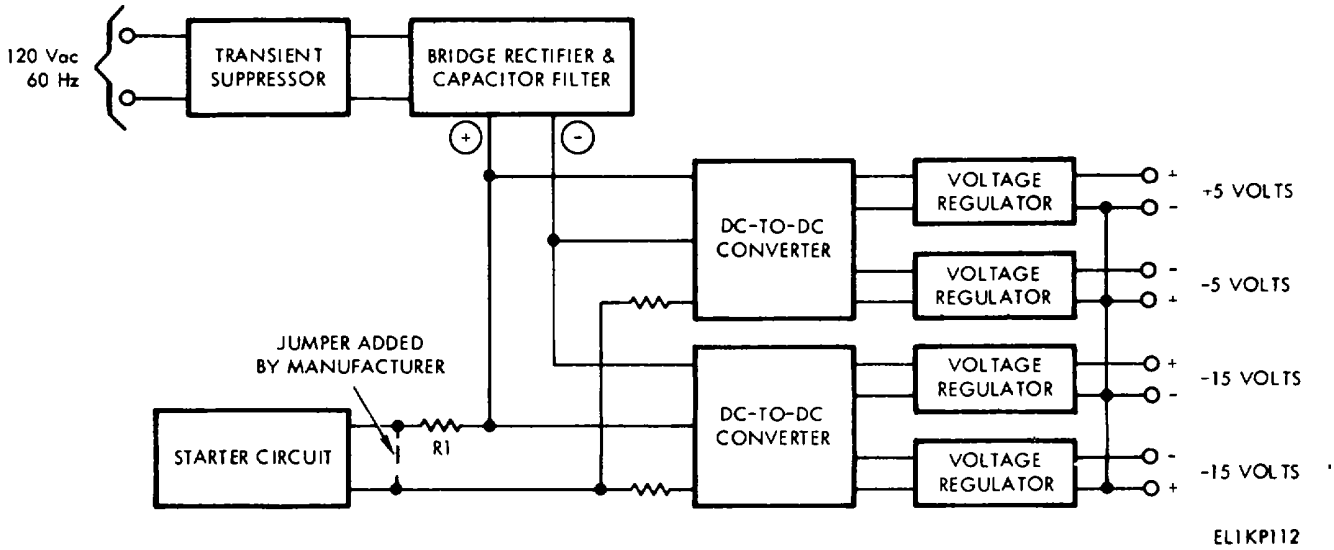


Figure 5-3. Dc power supply block diagram.

capacitor filter does not have one side tied to chassis ground. Therefore, large potentials do exist between the floating ground and chassis ground.

5-6. Circuit Description

a. Transient Suppressor. The transient suppressor (fig. FO-57, which includes two filters, absorbs short duration transients that might otherwise damage circuits in the power supply. Back-to-back Zener diodes (CR1) absorb the energy of high-amplitude low frequency transients, so that they are not passed on to power supply input circuits. The filters, consisting collectively of L1, L2, C1, C2, C3, and C4, serve primarily to prevent high frequency switching transients, generated within the power supply, from being reflected back into the input line and into other equipment. The filters also prevent electro-magnetic energy on the input line from being fed into the load circuits through the power supply.

b. Bridge Rectifier and Capacitor Filter. Diodes CR2, CRB, CR4, and CR6 form a full-wave bridge rectifier for the ac input (fig. FO57). Capacitors C5, C6, and C7 provide filtering to remove or smooth out the remaining ac component in the output of the bridge rectifier. The filtered output is applied directly to the dc-to-de converters through a jumper that bypasses the starter circuit (oscillator), which is used only for factory testing of the power supply.

c. Do-to-Dc Converter.

(1) *General* The dc-to-dc converters (fig. 5-4) transform the dc voltage derived from the input line power to specific dc levels required by the individual voltage regulators. The two dc-to-dc converters accept the output of the bridge rectifier and capacitor filter circuit, generate a square wave signal, and then rectify and filter this signal to produce a de level that is fed to the output voltage regulator circuits. One dc-to-dc converter is associated with the -5 and +5 volts dc power supply outputs, and the other is associated with the -15 and +15 volts dc outputs. The operation of both dc-to-dc converters is identical, therefore only one is described.

(2) *Inverter components*. A dc-to-dc converter functionally consists of an inverter, two full-wave rectifiers, and an output filter. The inverter is a push-pull switching inverter that provides two square wave outputs and is comprised of two power transistors (Q4 and Q6), and two transformers (TIA and T1B) containing a core material that has a rectangular hysteresis loop characteristic. Transistors Q4 and Q6 function as multivibrator type switches and are controlled by feedback current coupled to their bases from the composite action of the two saturating transformers.

(3) *Inverter switching*. Switching action starts in the inverter because of a small inherent imbalance in the circuit that causes one of the transistors, for example Q4, to start conducting before the other. The resulting voltage induced in the secondary winding (29 and 30) of transformer T1A is applied to the primary of base drive transformer T1B that is in series with feedback resistor R164. The secondary windings of T1B are connected so that transistor Q5 is reverse-biased and held at cutoff, while Q4 is driven to saturation. As transformer T1B saturates, the rapidly increasing primary current causes a greater voltage drop across feedback resistor R164. This increased voltage drop across R164 reduces the voltage applied to the primary of T1B, thus reducing the base drive input to Q4, which in turn decreases the collector current as Q4 eventually reaches cutoff. The curtailing of the collector current of Q4 causes the field of T1A to collapse, thereby reversing the polarity across the windings of transformers T1A and T1B. Transistor Q4 is then held at cutoff, while Q5 is rapidly driven to saturation. The transistors operate in this condition until transformer T1B saturates, and the circuit then returns to the initial state and the cycle is repeated.

(4) *Start resistor*. Resistor R8 assures a positive start for both transistors in the inverter when input power is applied. Then the circuit imbalance and regenerative action previously described causes the inverter to begin the switching action.

(5) *Square wave conversion* The square wave output of the inverter is rectified and filtered. The full-wave rectifier associated with the +15 volts dc output consists of CR17 and CR18, and the one associated with the -15 volts dc output consists of CR19 and CR20. RC snubbers, such as C13 and C17, are connected in parallel with each diode to dampen the transients that occur when a rectifier goes from the recovery to the blocking state upon each transition of the inverter square wave. Output filtering is provided by L8 and C22, and L7 and C21.

d. Output Voltage Regulator.

(1) General. The voltage regulator (fig. FO-58), provided for each of the four output voltages, also includes both short circuit and overvoltage protection circuity. Figure 5-5 is a simplified block diagram of the functional circuit groups in the voltage regulator. All four voltage regulators incorporate the same functions and operate similarly, therefore the following circuit description applies to each.

(2) *Regulator circuits.*

(a) The voltage regulator for the +15-volt de output is used as an example in this circuit description. This series type regulator is comprised of a monolithic circuit element (IC2); transistors Q20, Q21, Q10, Q13; and interconnecting discrete components (fig. 5-6). The integrated circuit element IC2 is a multifunction component that has equivalent circuitry as shown in figure 5-6, which is a simplified schematic representation

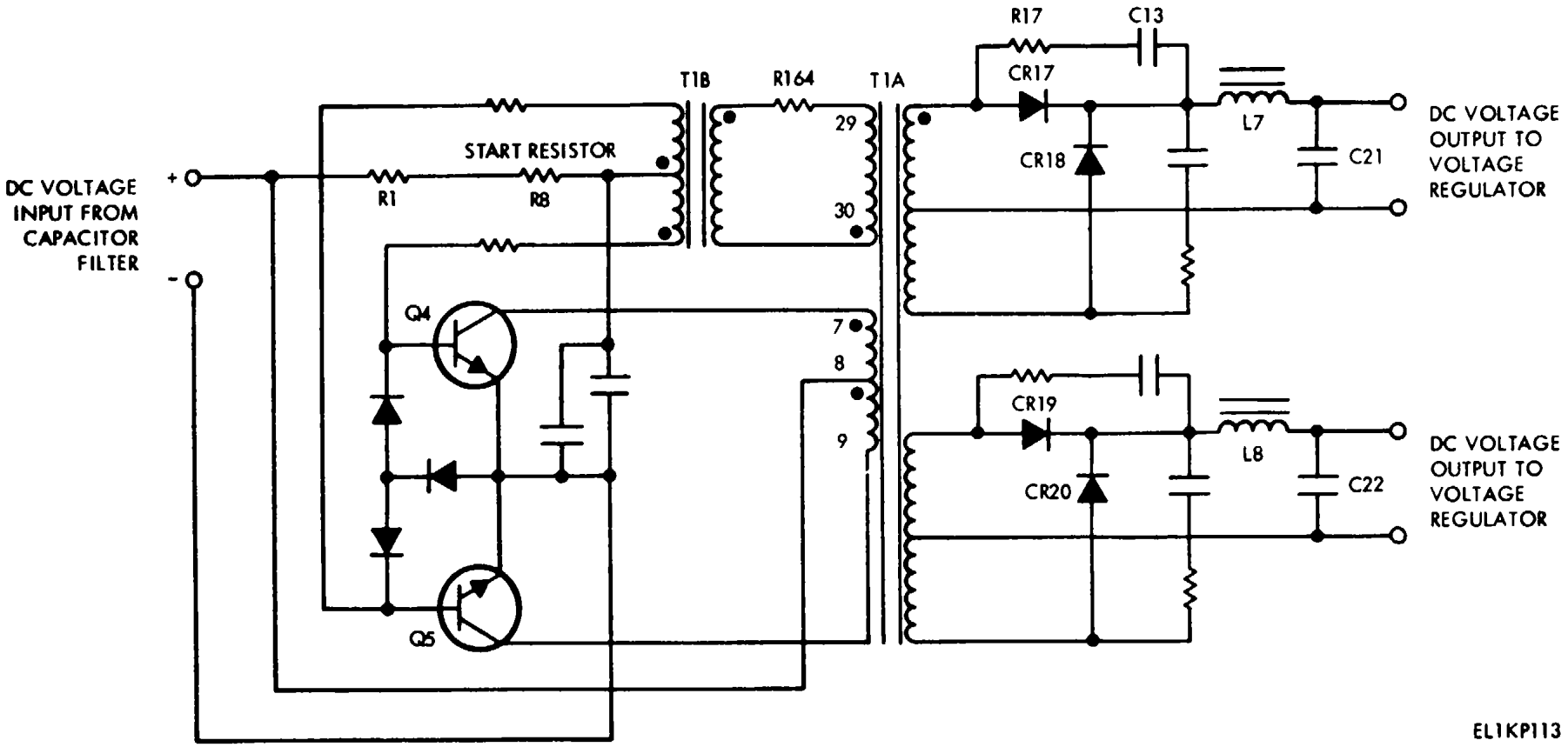


Figure 5-4. Example of dc-to-dc converter.

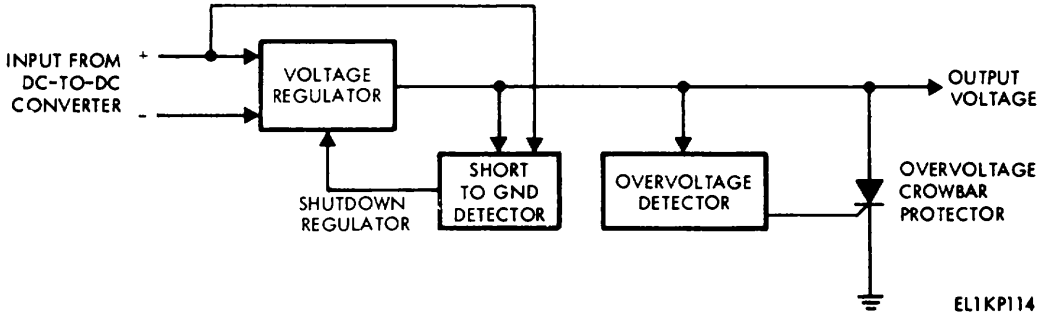


Figure 5-5. Regulator and output circuit block diagram.

of the regulator circuit. Circuit element IC2 includes a built-in reference voltage source, error amplifier, and series pass transistor. This device also provides for output current limiting by driving an internal circuit-limiting transistor from an external current-sensing resistor. Resistors R55, R66, R64 and R84 contribute to setting the allowed upper current level that flows through current sensing resistor R88. Resistor R88, in conjunction with R89, also splits the load current through transistors Q20 and Q21. Whenever the upper current level is exceeded, causing the current-limiting transistor within IC2 to conduct, the output voltage from the regulator is reduced. If the voltage reduction to compensate for the overcurrent load is large enough, the short circuit (undervoltage) detector (para (4) below) will shutdown the voltage regulator via Q13 to prevent excessive power build-up in the series pass control element. The current-limiting feature of IC2 protects the output regulator from overload conditions within the range of a short circuit up to an overcurrent load which turns on the undervoltage detector.

(b) A temperature-compensated reference voltage is fed through R71 as one input to the error amplifier in IC2. The other input to the error amplifier is taken from the sampling resistor network consisting of R70, R13, and R12, which collectively sample a portion of the regulators output voltage. The error amplifier produces a signal that is proportional to the difference between the two inputs. The error amplifier output drives transistor Q10, which inverts the signal so that it is properly phased for negative feedback and amplifies it to drive the series pass control element (Q20 and Q21). The control element interprets the signal and compensates accordingly to maintain the output voltage at a near constant level for temperature, input line, and load current variations.

(c) The sampling resistor network of R70, R13, and R12 determine the closed-loop regulator gain. The output voltage can be varied by adjusting potentiometer R12. The RC network of R71 and C15 controls the rate of rise of the reference voltage generated within IC2, when power is first applied to the output regulator. This in turn controls the rate of rise of the regulator output voltage, and prevents the overvoltage detector circuit ((3) below) from detecting a false overvoltage condition at power turn-on.

(d) If the power supply output is shorted to ground, transistor Q13 is turned on by a signal from the undervoltage detector. When Q13 is turned on, the series pass control element (Q20 and Q21) is turned off, removing the load from the output regulator to prevent internal damage.

(e) Capacitor C14 presents a very low output impedance for sudden changes in load current, thus preventing large changes in output voltage when abrupt load changes occur. Capacitor C14, in conjunction with components R68, C11, R61 and C10, reduces the tendency of the regulator loop to oscillate during heavy loads. Resistor R68 also aids in limiting the current through Q13 and the base-to-collector junction of the current-limiting transistor in IC2, when Q13 is turned on and C14 discharges through them. Diode CR5 prevents C14 from charging in the reverse direction.

(3) *Overvoltage protector.*

(a) To prevent the modem circuits from being exposed to an overvoltage condition if a power supply output regulator fails, an overvoltage protection circuit is used. The overvoltage protection circuit for the +15 volt dc power supply is shown in figure 5-7, and is typical of the same circuits used in the other three output regulators.

(b) Transistors Q1, Q2 and QS form a voltage comparator. The trip-level voltage of the comparator is determined by resistors R5, R6, R2, and R3. The voltage applied to the base of Q3 is less than that applied to CR2 during normal operation, therefore Q1 is cutoff, Q2 conducts, and SCR CR61 does not con-

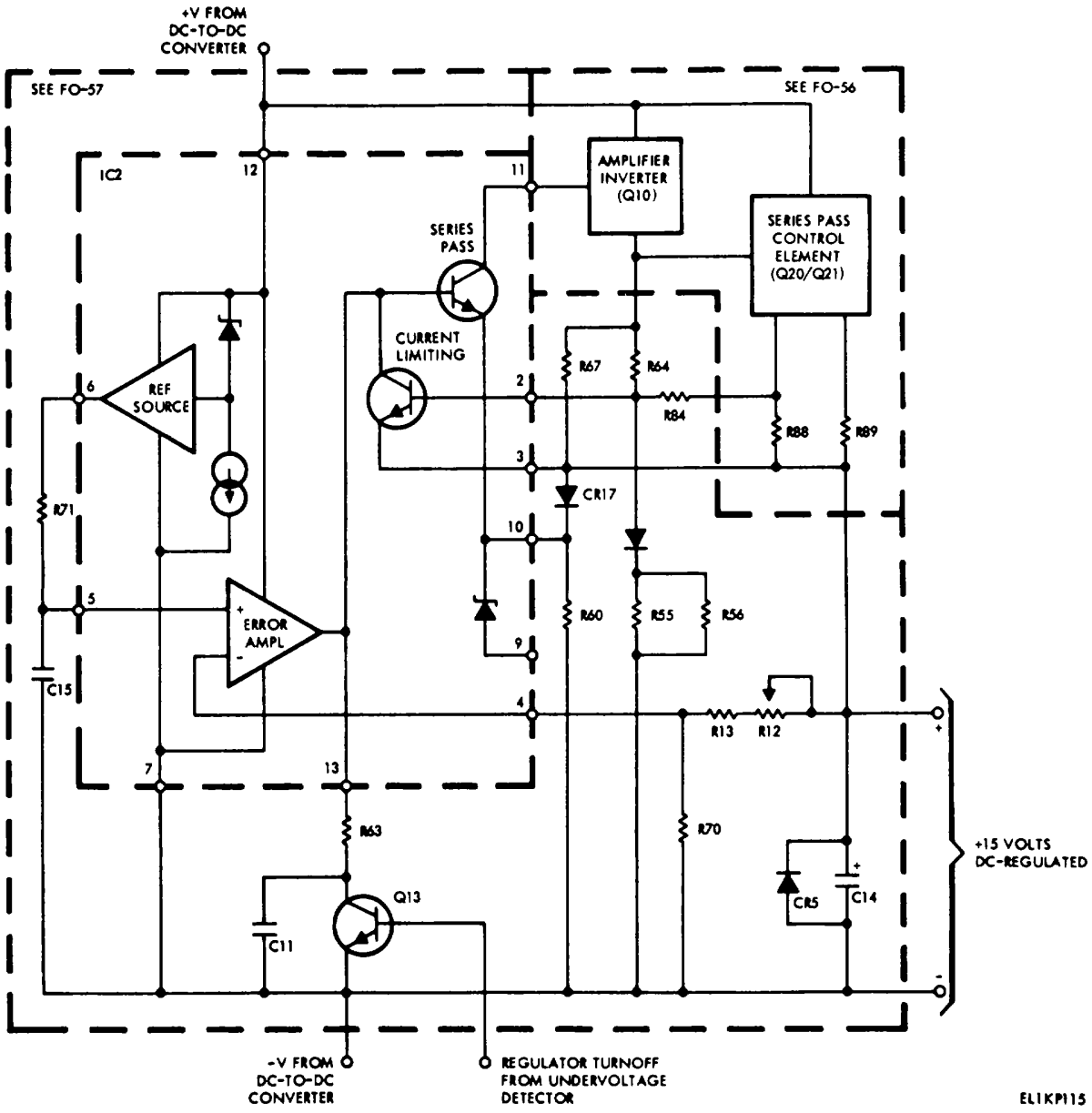


Figure 5-6. +15 voltage regulator.

duct. When the voltage output from the regulator exceeds the preset overvoltage limit, the voltage at the base of Q3 becomes more positive than the reference voltage of diode CR2, thus transistor Q2 is cutoff and Q3 and Q1 conduct. The conduction of transistor Q1 drives the SCR (CR61) into conduction, which reduces the output voltage.

(4) *Undervoltage detector.* The simplified circuit shown in figure 5-8 is the undervoltage detector used for the +15 volt voltage regulator, and is typical of the undervoltage detectors employed in the other dc voltage sources. This circuit serves to protect the output regulator from damage if a short circuit develops across the external load. Capacitors C8 and C9 prevent the turn-off of the voltage regulator (through Q13) during initial power turn-on. After power turn on, CR4 conducts and turns on transistor Q4. With Q4 conducting, Q12 is held cutoff. When either a short circuit develops

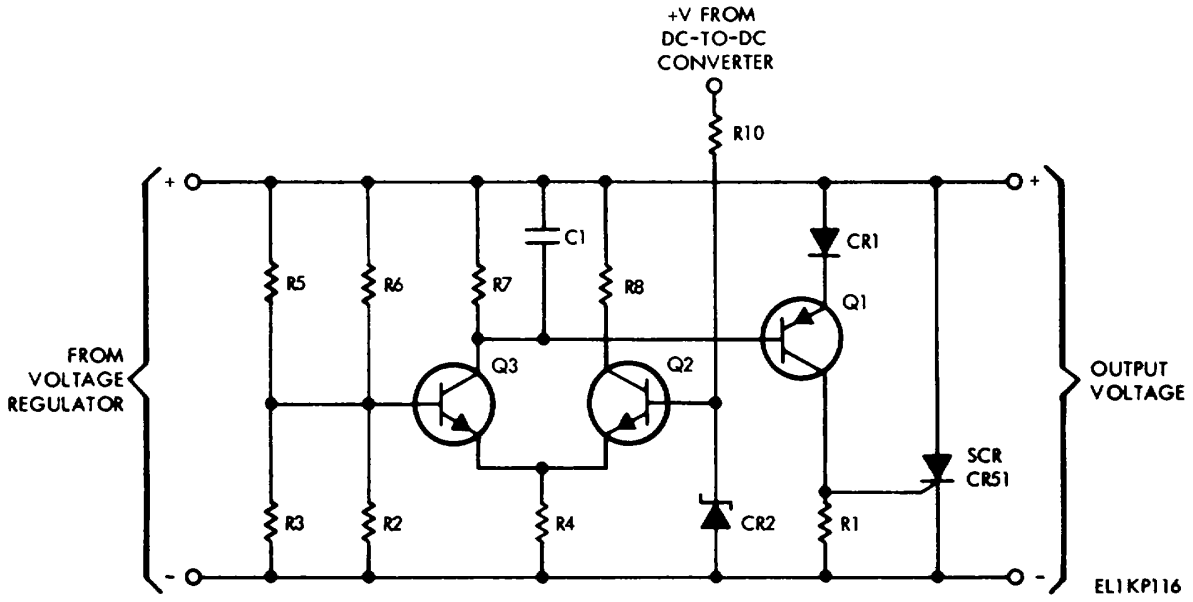


Figure 5-7. Overvoltage protector, simplified schematic diagram.

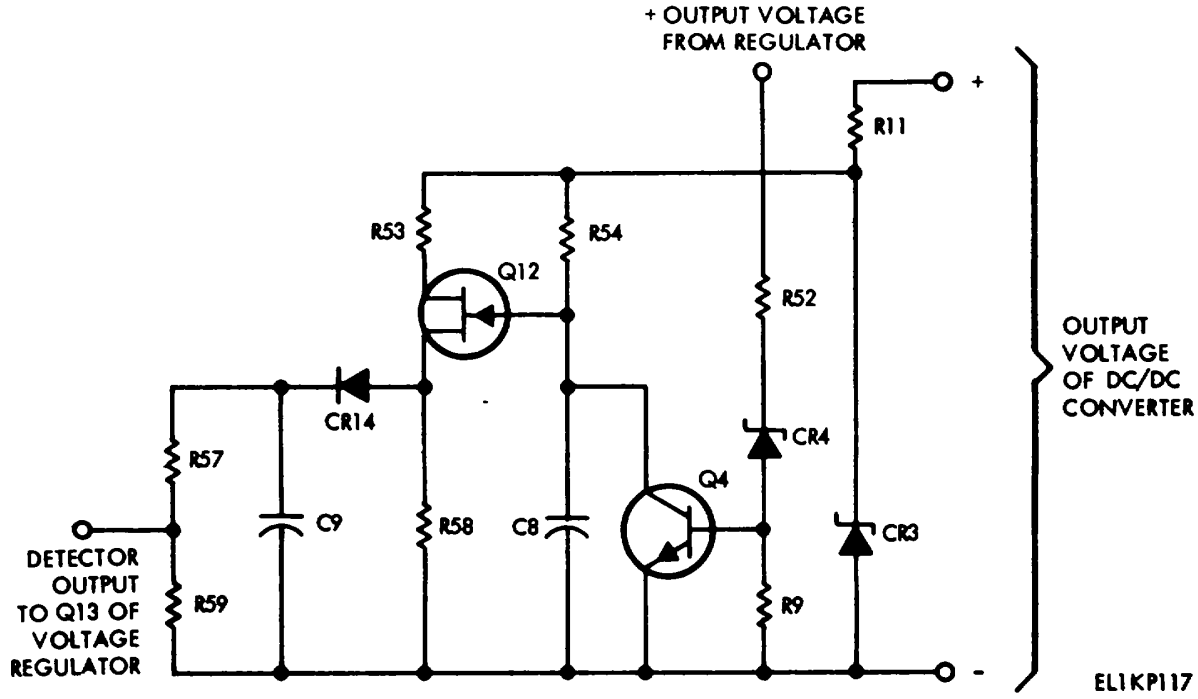


Figure 5-8. Example of undervoltage detector circuit.

circuit develops across the load, or the current-limiting action of the voltage causes the regulator output voltage to fall below the voltage value of CR4, transistor Q4 cuts off causing Q12 to conduct. When Q12 conducts, a signal is applied to turn on transistor Q13 in the voltage regulator, which effectively shuts down the regulator to prevent damage.

Section III. DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

5-7. General

This section contains detailed maintenance instructions for performing direct support maintenance on the power supply. This maintenance level includes testing, troubleshooting, and replacement operations. Direct support maintenance on the power supply is initiated through the failure of organizational maintenance to obtain the required outputs by adjustment, or because of other system problems, such as blown fuses, which indicate faulty power supply operation. A power supply suspected of faulty operation should first be bench checked in accordance with the performance test procedure of paragraph 5-9. Adjustments performed by direct support maintenance are limited to those external adjustments controlling the dc output levels. Internal adjustments, such as setting the overvoltage trip points and overcurrent limits, are not to be attempted at this maintenance level.

5-8. Tools and Test Equipment

The equipment required for testing, troubleshooting, and repairing the power supply is listed below.

a. Oscilloscope, Teletronix 485A.
b. Multimeter ME-419.
c. Digital Voltmeter, Fluke 8000A-01.
d. Autotransformer, Variac W50M.
e. Power Supply/Oscillator Test Fixture, SM-D-882197.

5-9. Performance Testing

a. Pretest Information The performance test procedure should be used in conjunction with the troubleshooting instructions to initially localize a fault. Also, each power supply shall be performance tested following any repair activity, to verify correct operation. Prior to testing a power supply, conduct a visual inspection for obvious defects and make repairs as required. First inspect the exterior of the assembly, and then remove the top cover (see para 5-llb) and inspect each subassembly. Look for blistered (overheated) components such as resistors and transistors, loose terminal connections, broken wires, and leakage of electrolyte from capacitors. Also ensure that heat sink fins are free of dust and dirt.

b. Performance Test Procedure

WARNING

Primary and secondary voltage commons in this power supply are isolated from the chassis. Therefore, large potentials do exist between floating ground and chassis ground.

CAUTION

Whenever power is applied to a power supply, sufficient airflow must be provided to ensure adequate cooling. An external fan must be setup with airflow directed onto the power supply Failure to observe this precaution will result in equipment damage.

(1) Verify that the AC POWER switch on the test fixture is in the off (down) position.

(2) Plug the test fixture line power cord into a 115 V ac source. Verify that the test fixture internal fan is operating.

(3) Connect equipment as shown in figure 5-9. Set the multimeter to the 50 V DC scale.

(4) Position an external fan so that the airflow passes directly over the power supply.

NOTE

Steps (5) through (29) describe the output loading and adjustment test

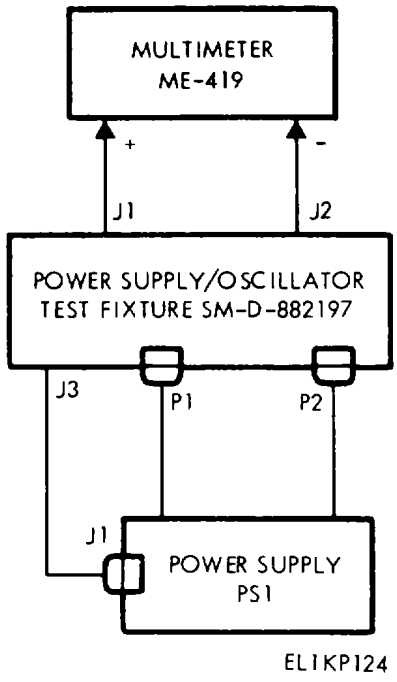


Figure 5-9. Initial test setup–power supply assembly test.

(5) Set the test fixture AC POWER switch to the ON position, and set LOAD SELECT switch to position 1. Set the multimeter to the 10 V DC scale.

(6) Adjust the +5 V control on the power supply for the lowest possible voltage, as indicated on the multimeter. Verify that the voltage is ≤4.9 volts dc.

(7) Adjust the +5 V control on the power supply for the highest possible voltage, as indicated on the multimeter. Verify that the voltage is ≥5.3 volts dc.

(8) Adjust the power supply +5 V control to obtain a reading of +5.1±0.2 volts dc on the multimeter.

(9) Set test fixture LOAD SELECT switch to position 2. Verify that the multimeter indicates 5.1 +0.2 volts dc.

(10) Set text fixture LOAD SELECT switch to position 3. Verify that the multimeter indicates 5.1 +0.2 volts dc.

(11) Set the multimeter to the 50 V DC scale, and set text fixture LOAD SELECT switch to position 4.

(12) Adjust the +15 V control on the power supply to obtain the lowest possible reading on the multimeter. Verify a minimum reading of +15.0 volts dc or less.

(13) Adjust the power supply +15 V control to obtain the maximum reading on the multimeter. Verify a reading of +15.6 volts dc or more.

(14) Adjust the power supply + 15 V control for a multimeter indication of ±15.3 +0.1 volts dc.

(15) Set test fixture LOAD SELECT switch to position 5. Observe multimeter for a reading of +15.3 ±0.2 volts dc.

(16) Set text fixture LOAD SELECT switch to position 6, and verify a reading of +15 ±0.2 volts dc on the multimeter.

(17) Set test fixture LOAD SELECT switch to position 7, and verify a reading of + 15.3 ±0.2 volts dc on the multimeter.

(18) Set test fixture LOAD SELECT switch to position 8, and verify a voltage indication on the multimeter of +15.3 ±0.2 volts dc.

(19) Set test fixture LOAD SELECT switch to position 9. Set the multimeter to the 10 V DC scale.
The voltage to be measured is -5 volts dc, however, the polarity is reversed in the test fixture and therefore a positive voltage is indicated on the multimeter. Adjust the power supply -5 V control for +5.1 ±0.2 volts dc as indicated on the multimeter.

(20) Adjust the power supply -5 V control for a minimum reading on the multimeter. Verify that the voltage is S4.9 volts dc.

(21) Adjust the power supply -5 V control for a maximum reading on the multimeter. Verify that the reading is ≥5.3 volts dc.

(22) Adjust the -5 V control of the power supply for a multimeter indication of 5.1 ±0.2 volts dc.

(23) Set text fixture LOAD SELECT switch to position 10, and verify a voltage reading of 5.1 +0.2 volts dc.

(24) Set the multimeter to the 50 V DC scale, and set text fixture LOAD SELECT switch to position 11. The voltage being measured is -15 volts dc, however, the polarity is reversed in the test fixture so therefore the multimeter will indicate a positive voltage.

(25) Adjust the -15 V control of the power supply to obtain the lowest possible voltage indication. Verify that the lowest multimeter reading is S15.0 volts dc.

(26) Adjust the -15 V control of the power supply for the highest possible reading on the multimeter. Verify a reading >15.6 volts dc.

(27) Adjust the power supply -15 V control for a reading of 15.3 +0.2 volts dc.

(28) Refer to table 5-2, and set the test fixture LOAD SELECT switch to the specified positions and observe the multimeter for the associated voltage indications.

(29) Set the test fixture AC POWER switch to the off (down) position, and disconnect the test equipment.

Table 5-2. Load Switching and Voltage Measurements

LOAD SELECT switch position	Voltage Indication
12	15 3±0 2 volts dc
13	15.3± L0 2 volts dc
14	5 1 ±0 2 volts dc
15	5.1 ±0.2 volts dc
16	5.1 ±O 2 volts de
17	5 1 ±0.2 volts dc
18	15.3 ±40.2 volts dec
19	5 1 ±0.2 volts dc
20	15.3 ±40 2 volts dc

NOTE

Steps (30) through (33) below describe the coax cable continuity test.

(30) Set the multimeter to the RX1 scale. Connect the multimeter to power supply PS1P1-N and PS1P2-N center conductors. Verify a resistance S0.2 ohms.

(31) Connect the multimeter between the power supply PS1P1 -N shell (outside conductor) and center conductor. Verify a resistance ≥1.0 megohm.

(32) Connect the multimeter between the power supply PS1P1-M and PSlP2-M center conductors. Verify a resistance 20.2 ohms.

(33) Connect the multimeter between power supply PSIP1-M center conductor and PSlP1-M shell (outside conductor). Verify a resistance 21.0 megohm.

NOTE

Steps (34) through (36) below describe the output ripple test.

(34) Connect equipment as shown in figure 5-10.

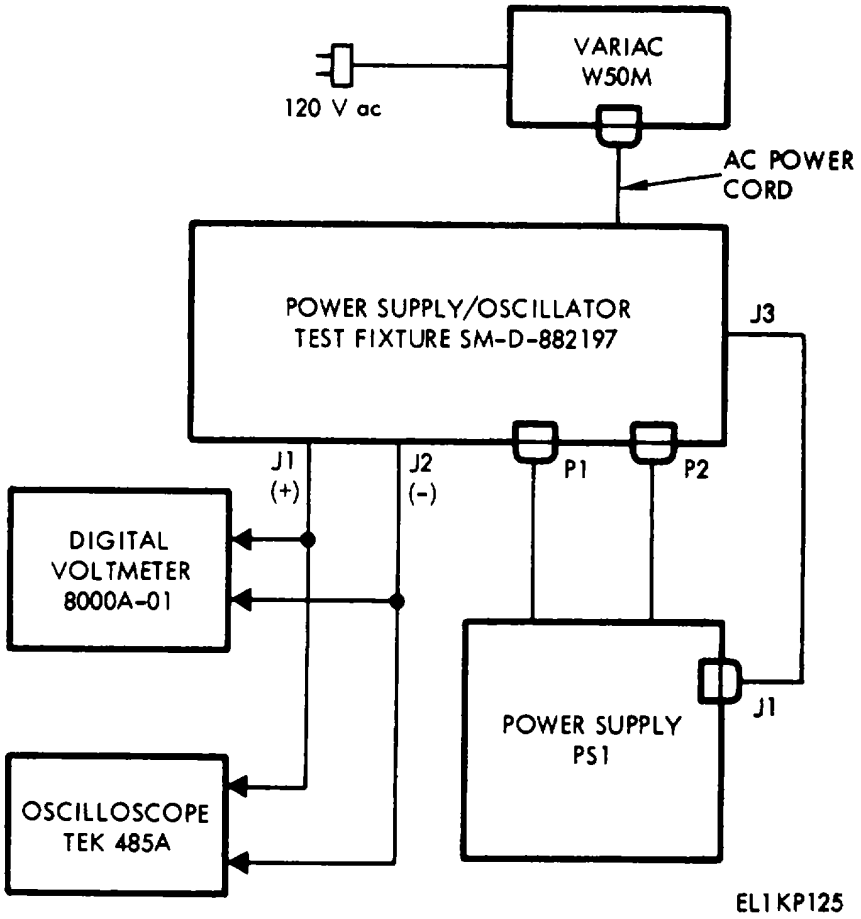


Figure 5-10. Test setup - output ripple regulation and overvoltage trip point test.

(35) Adjust variac for 120 volts ac and set test fixture AC POWER switch to ON.

(36) Refer to figure 5-11 for a typical example of an output waveform showing the ripple characteristics. Set the test fixture LOAD SELECT switch to each of the four positions listed in table 5-3 and use the oscilloscope to verify that any spikes on the selected output due to dc-to-dc converter switching are less than 1.0 volts peak-to-peak. Also, verify that any low level ripple due to input line frequency is less than 30 mV peak-to-peak on each selected output.

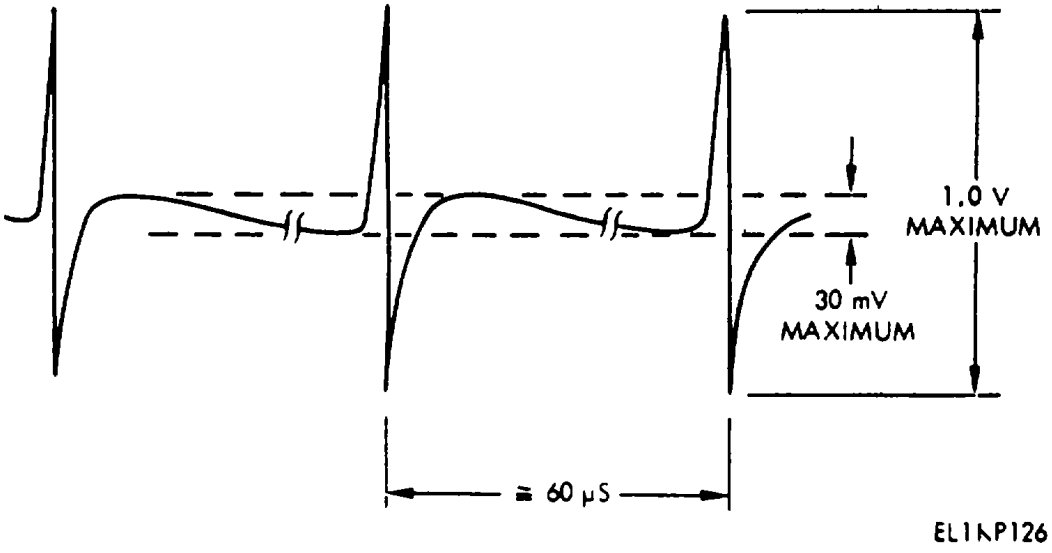


Figure 5-11. Typical dc output showing ripple characteristics.

Table 5-3. Load Switching for Output Ripple Measurements

LOAD SELECT switch position	Dc output voltage
1	+ 5.1* 0.2volts
4	+15.8 +0.2 volts
9	- 5.1 *0.2 volts
11	-15.8 *0.2 volts

NOTE

Steps (37) and (38) below describe the overvoltage trip point test.

(37) Set LOAD SELECT switch on text fixture to position 1. While observing the output voltage on the digital voltmeter, slowly increase the +5 V adjustment on the power supply until the output voltage begins to oscillate. Verify that the output was between 6.0 and 7.0 volts (overvoltage trip point) when the oscillation occurred. Readjust the +5 V control for 5.1 +0.2 volts as read on the digital voltmeter.

(38) Repeat the procedure in step (37) above for text fixture LOAD SELECT switch positions 4, 9, and 11, using the power supply +15 V, -5 V and -15 V adjustments, respectively. Verify that the trip point is between 17 and 18 volts for the ±15 volt outputs (LOAD SELECT position 4 and 11), and between 6.0 to 7.0 volts for the -5 volt output (LOAD SELECT position 9). After verifying the trip point for each output, readjust the appropriate voltage control on the power supply for the normal operating voltage, as listed below:

LOAD SELECT switch position	***Normal output voltage***
4	+15.8 +0.2 volts
9	- 5.1 0.2 volts
11	-15.8 *0.2 volts

NOTE

Steps (89) through (45) below describe the regulation test.

(39) Adjust the variac for 108 volts rms output.

(40) With the digital voltmeter, measure and record the power supply outputs at the +15 V, -16 V, +6 V, and -5 V test points on the power supply.

(41) Disconnect P1 from the test fixture.

(42) Adjust the variac for 132 volts rms output.

(43) With the digital voltmeter, measure and record the power supply outputs at the + 15 V, -15 V, +5 V, and -15 V test points on the power supply.

(44) Verify that the respective +5 volt and -5 volt measurements taken in step (43) above are within : 5 mV of the corresponding measurements taken in step (40) above. Verify that the respective +15 volt and -15 volt measurements taken in step (43) above are within +15 mV of the corresponding measurements taken in step (40) above.

(45) Set test fixture AC POWER switch to the off (down) position, remove input to the variac, and disconnect all test equipment.

5-10. Troubleshooting

a. General Trouble Analysis. A faulty power supply shall first be bench checked in accordance with the performance test procedure in paragraph 5-9. Any out-of-tolerance parameters and abnormal operating conditions displayed during the performance test shall be noted. The fault isolation procedures in this paragraph are presented in tabular format and the individual table titles correspond to the most commonly encountered trouble symptoms observed during performance testing. Refer to figures FO-57 and FO-58 for schematic diagrams of the power supply. For parts location information and authorized repair parts lists, refer to TM 11-5820-847-34P. Appendix C contains a wire list of internal power supply connections.

b. Troubleshooting Procedures.

(1) Detailed troubleshooting instructions are given in table 5-4 through 5-17. These tables consist of step-by-step instructions for isolating faults to a subassembly or a component that is replaceable at the direct support level. When a trouble symptom is identified, refer to the troubleshooting table title that most closely corresponds to the symptom. In addition to the general and detailed troubleshooting tables, listings of typical point-to-point resistance and voltage measurements (tables 5-18 and 5-19) are provided as a fault isolation aids. The troubleshooting tables are listed below:

(a) Table 5-4. Loss of +5 Volt Output, Troubleshooting Procedure.

(b) Table 5-5. Loss of -5 Volt Output, Troubleshooting Procedure.

(c) Table 5-6. Loss of +15 Volt Output. Troubleshooting Procedure.

(d) Table 5-7. Loss of -15 Volt output, Troubleshooting Procedure.

(e) Table 5-8. Loss of +5 and -6 Volt Complementary Outputs, Troubleshooting Procedure.

(f) Table 5-9. Loss of +15 and -15 Volt Complementary Outputs, Troubleshooting Procedure.

(g) Table 5-10. Loss of All Power Supply Outputs, Troubleshooting Procedure.

(h) Table 5-11. High Output Voltage, Troubleshooting Procedure.

(i) Table 5-12. All Output Voltages Low, Troubleshooting Procedure.

(j) Table 5-13. Low +15 and -15 Volt Complementary Outputs, Troubleshooting Procedure.

(k) Table 5-14. Low +5 and -5 Volt Complementary Outputs, Troubleshooting Procedure.

(l) Table 5-15. Low Output Voltage, Troubleshooting Procedure.

(m) Table 5-16. Output Voltage Oscillation, Troubleshooting Procedure.

(n) Table 5-17. Excessive Line Frequen4 Ripple On Outputs, Troubleshooting Procedure.

WARNING

High voltages are present within the power supply. Use extreme care to avoid contact with high voltages when making internal measurements or adjustments with the top cover removed. Remove all power before performing any resistance or continuity checks, or any removal or replacement operations.

WARNING

The input filter capacitors PS1C5, C6, C7 of the power supply do not have one side (-) tied to chassis ground. Therefore large potentials do exist between this floating ground and chassis ground.

WARNING

Before disconnecting the electrical leads to input filter capacitors PSIC5, C6, or C7, allow at least one minute after removing power from the power supply for the capacitor voltage charge to bleed off.

Table 5-4. Loss of +5 Volt Output, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Loss of +5voltoutput.	Measure voltage between J2-1s (-) and J2-14 (+) on voltage regulator board A2. Normal reading is 19 2 volts de.	If reading is normal or high, proceed to step 2. If reading is low, perform step 5.
2	Voltage betwenA2J2-14 andA22-18 is normal or high.	Measure voltage between J2-1s (-) and J2-16 (+) on voltage regulator board A2. Normal reading is greater than 6 volts de.	If reading is normal, go to step 8. If reading is low, voltage regulator board A2 is defective or undervoltage detection ircult has been activated by an overcurrent condition. Replace voltage regulator board A2. If this does not correct fault, return original voltage regulator board to power supply and check components A1OCR49 and A9C51 for short circuits (see table 5-18 for typical output resistanee measurements).
8	VoltagebetweenA2J2-la ndA2J2-16 is normal.	Measure voltage between J2-16 (+) and J2-17 (-) on voltage regulator board A2. Voltage is 0.8 +0.4 volts de.	If voltage reading is high, transistor ASQ12 Is probable cause. If reading is normal, perform step 4.
4	VoltagebetweenA2J2-16andA2J2-17 is normal.	Measure voltage between J2-17 (+) and J2-18 (-) on voltage regulator board A2 Normal voltage reading is 0.8 -0.4 volts dc	If voltage reading is normal, check for presence of 9 256 2 0 volts dc between A2J2-13 (-) and collector of transistor A8Q14 No voltage present indicates probable cause is broken wire between AlTIC-28 and collector of transistor A8Q14. If voltage reading is high, check for open connection between transistor ASQ12 emitter and A8Q14 base
5	Voltage between A2J2-18 and A2J2-14 is low	Probable fault is shorted voltage regulator (A2 subassembly) input, or defective component in dc-to-dc converter circuits (faulty Al, A4, or As subassembly).	Replace subassembly A2 (voltage regulator). If fault is not corrected, return original subassembly A2 to power supply and return power supply to depot for repair.

Table 5-5. Loss of -5 Volt Output, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Los of -5 volt output.	Measure voltage between J3-13 (-) and J3-14(+)on voltage regulator board A2 Normal voltage reading is 19 5 *3 volts dc.	If voltage reading is normal or high, perform step 2 If reading is low, perform step 5.

Table 5-5. Loss of -5 Volt Output, Troubleshooting Procedure-Continued

Step	Symptom	Procedure	Probable cause/corrective action
2	VoltagebetweenA2JS-4l ndA2J3-18 is normal or high.	Measure voltage between J3-13 (-) and J3- 16 (+) on voltage regulator board A2 Normal reading is greater than 6 volts de	If voltage reading is normal, perform step 3. If reading is low, voltage regulator board A2 w defective or undervoltage detection circuit has been tripped by oh overcurrent condition. Replace voltage regulator board A2. If this does not c fault, return original voltage regulator A2 to power supply and check components A1OCR50 and A9C52 for short circuits (see table 5-18 for typical output resistance measurements)
3	VoltagebetweenA2J3-l8andA2JS-16 is normal.	Measure voltage between J3-16 (+) and J3-17 (-) on voltage regulator board A2. Normal reading is less than 1 2 volts de	If voltage reading is high, replace transistor A8Q13. If reading is normal, perform step 4.
4	Voltage between A2J8-16 and A2J3-17 is normal.	Measure voltage between J3-17 (+) and J3-18 (-) on voltage regulator board A2 Normal reading is less than 1.2 volts dc.	If voltage reading is high, transistor A7Q19 is probable cause If reading is normal, resistor A7R87 is open and should be replaced
5	Voltage between A2JS-13 and A2JS-14 is low.	Probable fault is shorted voltage regulator (A2 subassembly) input or defective cornponent in dc-to-dc converter circuits.	Replace voltage regulator board A2. If fault is not corrected, return original subassembly A2 to power supply Power supply should be sent to depot for repair, as fault location procedure indicates trouble is defective Al, A4, or A5 subassembly.

Table 5-6. Loss of +15 Volt Output, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Loss of +l volt output.	Measure voltagebetweenJ2-4(-)andJ2-7 (+) on voltage regulator board A2. Voltage reading is 22.5 :3 0 volts de	If voltage reading is normal or high, perform step 2. If reading is low, perform step 5.
2	Voltage between A2J2-4 and A2J2-7 is normal or high.	Measure the voltage between J2-6 (-) and J2-7 (+) of voltage regulator board A2 Normal reading is 0 8 :0 4 volts dc	If reading is normal, perform step 3 If voltage is high or low, replace voltage regulator board A2. If this does not eliminate fault, return original subassembly A2 to power supply, and check transistor A7Q10 for open or shorted base-to-emitter junction If transistor A7Q10 appears good, check components A10CR51 and A9C53 for short circuits (see table 5-18 for typical output resistance measurements)
3	Voltage between A2J2-6 and A2J2-7 is normal.	Measure the voltage between J2-4 (-) and J2-5 (+) on voltage regulator board A2 Normal voltage reading is greater than 16 volts dc	If voltage is low, transistor A7Q10 is probable cause If voltage is normal, perform step 4.
4	Voltage between A2J2-4 and A2J2-5 is normal.	Measure voltage between J2-5 (+) and J2-9 (-) Normal reading 08 $\pm$0.4 volts dc.	If voltage reading is normal, check resistors A7R88, A7R89, and associated wiring for open circuit. If reading is high, check transistors A7Q20, A7Q21, and associated wiring for open circuit.
5	Voltage between A2J2-4 and A2J2-7 is low.	Probable fault is shorted voltage regulator board A2 input or defective component in dc-to-dc converter circuits (faulty Al, A4, or A5 subassembly).	Replace voltage regulator board A2. If fault is not corrected, return original A2 sub assembly to power supply, and return power supply to depot for repair

Table 5-7. Loss of -15 Volt Output, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Loss of -15 volt output.	Measure voltage between J3-4 (-) and J3-7 (+) on voltage regulator board A2. Normal reading is 22 5 +3.0 volts de	If reading is normal or high, perform step 2. If reading is low, perform step 6.
2	Voltage between A2J3-4 and A2J3-7 is normal or high reading is O 8 :0.4 volts dc	Measure voltage between J3-6 (-) and J3-7 (+) on voltage regulator card A2. Normal reading is 0 8 +0 4 volts dc	If reading is normal, perform step 3 If reading is high or low, replace voltage regulator A2 subassembly. If fault is not corrected, reinstall original A2 subassembly, and check transistor A7Qll for shorted or open base-to-emitter junction. If A7Qll appears good, check components A1OCR62 and A9C54 for short circuit (see table 5-18 for typical output resistance measurements)
3	Voltage between A2J3-6 and A2J3-7 is normal	Measure voltage between J3-4 (-) and J3-5 (+) on voltage regulator board A2 Normal reading is greater than 16 volts de	If voltage reading is low, transistor A7Qll is probable cause If reading is normal, perform step 4
4	Voltage between A2J3-4 and A2J3-5 is normal	Measure voltage between J3-5 (+) and J3-9 (-) of voltage regulator board A2. Normal reading is 0.8 :0.4 volts de	If voltage reading is normal, check resistors A7R90 and A7R91 and associated wiring for open circuit If reading is high, check transistors A7Q22 and A7Q23 and associated wiring for open circuit.
5	Voltage between A2J3-4 and A2J3-7 is low.	Probable fault is shorted input to voltage regulator board A2 or defective component in dc-to-dc converter circuit (faulty A1, A4, or As subassembly).	Replace voltage regulator board A2. If fault Is not corrected, return original A2 sub assembly to power supply, and return power supply to depot for repair.

Table 5-8. Loss of +5 and -5 Volt Complementary Outputs, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Loss of both + 65 and -5 volt outputs.	Dc-to-de converter not operating. Measure voltage between capacitors PS1C6, C6, C7 common (-) bus and transformer A1T1C-14. Normal voltage reading Is 155 *80 volts de.	If voltage reading Is normal, perform step 2. If no voltage Is present, check for broken wires or connections from PS1CS (+) to A1T1C-14 and repair as required.
2	Voltage between capacitors PS1Cs, C6, C7 common (-) bus and A1T1C-14 is normal.	Measure voltage between capacitors PSiC6, C6, C7 common (-) bus and transformer AlT1D-20. Normal reading is 0.6 +0 3 volts de	If voltage reading is normal, perform step 8 If reading is high check for open resitores A6R10 or A6R12, open base-to-emitter junction on transistors A6Q6 or A6Q7, open transformer winding between A1T1D-19, AlT1D-20, or AlTlD-21 If voltage reading is not present, resistor A3R1 is open In the event a transformer A1T1D winding or resistor A3R1 is open, return the power supply to the depot for for repair
3	Voltage between capacitors PS1C5, C6, C7 common (-) bus and A1TID-20 is normal.	Remove input power from power supply and measure continuity between transformer windings as follows A1T1D- 17 to A1T1C-16 — 1 ohm max A1T1C-14 to A1T1C- 13 — 1 ohm max. A1T1C-14 to A1T1C- 15 — 1 ohm max	If any measurement exceeds 1 ohm, subassembly Al is faulty and power supply should be returned to depot If measurements are normal, perform step 4.

Table 5-8. Loss of +5 and -5 Volt Complementary Output, Troubleshooting Procedure-Continued

Step	Symptom	Procedure	Probable cause/corrective action
4	Transformer winding continuity is normal.	Check for the following possible faults: a. Shorted diode A6CR5S or A6CR55, or open A6CR64. b. Shorted base-to-emitter junction on transistors A6Q6 or A6Q7. c. Open base-to-collector junction on transistors A6Q6 or A6Q7. d. If items above are normal, check for open resistor A1R165.	 Replace faulty diode. Replace faulty transistor. Replace faulty transistor. Return power supply to depot for repair

Table 5-9. Loss of +15 and -15 Volt Complementary Outputs, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Loss of both +16 and -15 volt outputs.	Dc-to-dc converter not operating or +15 volt output has failed. Measure voltage between J8-4 (-) and J8-7 (+) on voltage regulator board A2. Normal reading is greater than 18 volts.	If reading is normal, refer to table 5-6, step 1. If reading is low or mer, perform step 2.
2	Voltage between A2J3-4 and A2J3-7 is low or zero.	Dc-to-dc converter not operating. Measure voltage between capacitors PS1C6, C6, C7 common (-) bus and transformer A1TIA-& Normal reading is 1655 :L0 volts dc.	If voltage reading is normal, perform step S. If no voltage is present, check for broken wires or connections between capacitor PS1C5(+)and transformer AlTlA-8.
3	Voltage between capacitors PS1C5, C6, C7, (-) bus and transformer A1TlA -8 is normal.	Measure voltage between capacitors PS1C6, C6, C7, (-) bus and transformer A1T1 B-26 Normal reading is 0 6 0.3 volts dc	If voltage reading is normal, perform step 4. If reading is high, check for open resistors A6R9 or A6Rll, open base-to-emitter junction on transistors A6Q4 or A6Q6, open transformer winding between A1T1B-26, A1T1B-25, or A1TlB-27. If no voltage is present, open resistor A3R8 is probable cause. In the event a transformer A1T1B winding or resistor A3R8 is open, return the power supply to the depot for repair.
4	Voltage between capacitors PS1C5, C6, C7 common (-) bus and A1T1B-26 is normal.	Remove input power from power supply and measure continuity between transformer windings as follows: A1T1B-28 to A1T1A-29 1 ohm max A1T1A-8 to A1T1A-7 1 ohm max A1T1A-8 to A1T1A-9 1 ohm max	If any measurement exceeds 1 ohm, sub-assembly Al is defective and power supply should be returned to the depot for repair If all measurements are normal, perform step 5
5	Transformer winding continuity is normal.	Check for the following possible faults: a. Shorted diode A6CR66 or A6CR58 or open diode A6CR67 b. Shorted ban-to-emitter junction on transistors A6Q4 or A6Q6. c. Open base-to-collector junction on transistors A6Q4 or A6Q6. d. If items above are normal, check for open resistor A1R164.	 Replace defective diode. Replace defective transistor. Replace defective transistor. Return power supply to depot for repair.

Table 5-10. Loss of All Power Supply Outputs, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	No dc outputs	Check for open ac line power fuse	Replace ac line fuse. If fuse blows upon application of power, perform step 2 If ac line fuse is not open, perform step 7
2	Ac line fuse blows on power application	Remove input power from power supply and disconnect two pairs of leads from the (+) bus of capacitors PS1C5, C6, and C7 Reapply Input power to power supply	If ac line fuse blows, short circuit Is in transient suppressor or bridge rectifier circults, return power supply to depot for repair If ac line fuse does not blow, fault is in capacitors PS1C5, C6, C7, dc-to-dc converter circuits, or voltage regulator input Perform step 3
8	Input line fuse does not blow with capacitor PSICS, C6, C7 + bus disconnected	Check capacitors PS1C5, C6, and C7 for high leakage or shorts Leakage resistance is less than 100K ohms	If capacitors PS1C5, C6, or C7 show evldence of leakage or shorting, replace faulty components. If capacitors are good, perform step 4
4	Capacitors PSlC5, C6, andC7 not faulty	Check between following points for indicated resistance. A2J2-13 to A2J2-14 2000 ohms mm A2J3-13toA2J3-14 2000 ohms mm A2J2-4 to A2J2-7 2000 ohms min A2J3-4 to A3J3-7 2000 ohms min.	If all resistance measurements are satisfactory, perform step 6 If a measurement is less than the indicated value, note the particular measurement and perform step 5
5	Resistance measurement in step 4 not satisfactory	Remove voltage regulator board A2 and repeat abnormal measurement taken in step 4 on the power supply	If measurement is not satisfactory, fault is in voltage regulator board A2 Replace the faulty voltage regulator board A2 If the measurement is still low, the fault is in subassembly A4 or A5 In this case, return the power supply to the depot for repair
6	Voltage regulator board A2 resistance measurements normal.	Fault Is in dc-to-dc converter switching circuits or transformers. Check the following for defects a. Check transistors A6Q4, A6Q5, A6Q6, and A6Q7 for shorted junctions b. Check diodes A6CR53 through A6CR58 for shorted junctions c. Check transformers AlT1A through A1T1D for shorts	 Replace defective transistor Replace defective diodes Return power supply to depot if a transformer is shorted
7	No dc outputs, input line fuse normal	Fault is open circuit in input bridge rectifier, transient suppressor, or chassis-mounted resistor PSIR1 Measure voltage across capacitors PS1C5, C6, and C7 Normal voltage is 155 ±20 volts dc	If voltage is normal or high, check for open chassis-mounted resistor PSiR1 or broken wires to transformers If voltage reading is low, perform step 8
8	Voltage across capacitors PS1C5, 6, C7 is low	Check forward and reverse resistance (in-circuit) of rectifier diodes A4CR2, A4CR3, A4CR4, A4CR5 Normal forward resistance is 15 ohms maximum (RX1 scale), reverse resistance is 5K ohm minimum (RX100 scale)	If any resistance measurement is abnormal, probable cause is diode, return power supply to depot for repair If resistance measurements are normal, perform step 9
9	Bridge rectifier diodes forward and reverse resistance normal	Check continuity from ac input connector J1-1 to circuit junction of diodes A4CR3 and A4CR4, and from J1-2 to circuit junction of diodes A4CR2 and A4CR5 choke is open, return power supply to depot for repair	Open circuit indicates broken wire or open transient suppressor choke (AIL1 or AIL2) in subassembly Al Repair broken wire as necessary If transient suppressor

Table 5-11. High Output Voltage, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
		NOTE If output voltage exceeds overvoltage trip point, output will oscillate.	
1	Output voltage s high and cannot be reduced by output adjustment.	Fault is in voltage regulator board A2 or caused by leaky output transistors Replace voltage regulator card A2	If output voltage can be adjusted to within required limits by output voltage adjustment, original voltage regulator board A2 is defective. If new voltage regulator board A2 does not correct fault, return original regulator board to power supply and perform step 2
2	Voltage regulator board A2 not defective.	To detect any shorted or leaky output transitors, make the following voltage checks at the specified points on the voltage regulator board A2 connectors. A voltage reading less than the designated value or one with reversed polarity indicates a shorted or leaky output transistor(s).	
		Output circuit — Measurement points — Voltage reading	
		+5volt J2-18(-)toJ2-17(+) — +0.4	Perform step 3.
		J2-17(-)to J2- 16(+) — +0.4	Replace transistor A8Q12
		- volt J-18(-) to J-17 (+) — +0.4	Replace transistor A7Q19
		J8-17 (-) to J8-16 (+) — +0.4	Replace transistor A8Q18.
		+15 volt J2-9 (-)toJ2-5 (+) — +0.4	Perform step 8S.
		J2-6 (-)toJ2-7 (+) — +0.4	Replace transistor A7Q10.
		-15volt J8-9 (-)toJ8-5 (+) — +0.4	Performstep8.
		J8-6 (-)toJ3-7 (+) — +0.4	ReplacetransistorA7Qll.
3	Voltage In step 2 indicate faulty output transistors.	To isolate a particular faulty transistor in output stages consisting of multiple parallel-connected transistors, such La the +6, +15 and -15 volt supplies, monitor the output voltage of the supply and disconnect the collector leads of the parallel transistors one at a time. After each collector lead is disconnected, check for a decrease in the abnormally high output. When performing this cheek, only one collector should be disconnected at any one time. The three groups of parallel-connected output transistors are listed below. +5 volt supply: A8Q14, Q15, Q16, Q17, Q18 +15 volt supply A7Q20, Q21 -15 volt supply A7Q22, Q23.	If the collector for a faulty transistor is disconnected, the associated high output voltage will decrease. When this occurs, replace the applicable transistor.

Table 5-12. All Output Voltages Low, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Low output, all voltages.	Fault is low line voltage, bridge rectifier diode open, or open filter capacitor Verify input voltage.	If input line voltage is normal, go to step t
2	Input line voltage normal.	Check capacitors PS1C5, C6, and C7 for open condition (See fig 5-13A for typical oscilloscope waveform and table 5-18 for resistance measurement checking capacitors.)	Replace faulty capacitor. If no capacitor is faulty, return power supply to depot for bridge rectifier diode fault Isolation and to aid In repair.

Table 5-13. Low +15 and -15 Volt Complementary Outputs, Troubleshooting Procedure.

Step	Symptom	Procedure	Probable cause/corrective action
1	Low +15and-15voltoutputg.	Probable fault is in de-to-dc converter. With oscilloscope verify presence of 310 volt peak-to-peak square wave (see fig 5-12A) at A1TlA-9 and AlTlA-7, using (-) bus of PSiC6, C6, C7 as ground reference At both measurement points the low part of waveform should be less than 8 volts, indicating transistors A6Q5 and A6Q4 are saturating.	If waveform indicates absence of transistor saturation at both AlT1A-9 and AiTlA-7, check diode A6CR57 for open or shorted condition and check resistors A6R9 and A6Rll for correct values If correct waveform is not present at only one point (AlTlA-7 or A1TlA-9), proceed to step 2 or 3 as applicable
2	Waveform at A1TlA-9 does not indicate transistor saturation.	Transistor A6Q5 not saturating. Check for open diodes A6CR57, A6CR56, A6CR58. Also check for leaky transistor A6Q4 or low gain of transistor A6Q5 (See fig 5-12B and 6-12C for typical waveshapes in troubleshooting components.)	Replace defective component(s) as necessary
3	Waveform at AlT1A-7 does not indicate transistor saturation.	Transistor A6Q4 not saturating Check for open diodes A6CR56, A6CR57, A6CR58. Also check for leaky transistor A6Q6 or low gain of transistor A6Q4. (See fig 5-12B and 5-12C for typical waveshapes in troubleshooting components.)	Replace defective components as necessary.

Table 5-14. Low +5 and -5 Volt Complementary Output, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Low +5and 4voltoutputs.	Probable fault is in dc-to-dc converter. With oscilloscope verify presence of 810 volt peak-to-peak square wave (see fig. 5-12A) at AlTIC-18 and AlTiC-15, using (-) bus of PS1C5, C6, C7 as ground reference. At both measurement points the low part of waveform should be less than 3 volts, indicating transistors A6Q6 and A6Q7 are saturating	If waveform indicates absence of transistor saturation at both AlTIC-15 and AiT1C-13, check diode A6CR64 for open or short condition and check resistors A6R10 and A6R12 for correct values If normal waveform is not present at only one point (AlT1lC-15 or A1T1lC-13), proceed to step 2 or 8 as applicable.
2	Waveform at A1T1lC-18 does not indicate transistor saturation.	Transistor A6Q6 not saturating Check for open diodes A6CR65, A6CR54, A6CR56 Also check for leaky transistor A6Q7 or low gain of transistor A6Q6. (See fig 5-12B and 5-12C for typical waveshapes in troubleshooting components)	Replace defective components as necessary.

Table 5-14. Low +5 and -5 Volt Complementary Outputs, Troubleshooting Procedure-Continued

Step	Symptom	Procedure	Probable cause/corrective action
3	Waveshape at A1T1lC-15 does not indicate transistor saturation	Transistor A6Q7 not saturating. Check for open diodes A6CR53, A6CR54, A6CR55. Also check for leaky transistor A6Q6 or low gain of transistor A6Q7 (See fig. 5-12B and 5-12C for typical waveshapes in troubleshooting components)	Replace defective components as necessary

Table 5-15. Low Output Voltage - Single Output, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Low output voltage on single output	Fault is in voltage regulator board A2, rectifier circuit in dc-to-dc converter, or output drive transistors. Replace voltage regulator board A2	If output voltage returns to normal, original voltage regulator is faulty If fault is not corrected, return original voltage regulator to power supply and perform step 2.
2	Voltage regulator board A2 is not defectlve.	Make the following applicable voltage checks at the specified points on the voltage regulator board A2 connectors ***Output circuit — Measurement points — Voltage reading*** + 6volt J2-13(-)toJ2-14(+) — 19 :±3 - 5volt J8-13(-)toJ3-14(+) — 14.5±25 +15volt J2-4(-)toJ2-7(+) — 22 5±3 -15 volt J3-4(-) to J3-7 (±) — 22.5 :±3	If the measured voltage is low, fault is in subassembly Al, A4, or A5 Return the power supply to depot for repair If the measured voltage is normal or high, perform step 3.
3	Voltage measured at voltage regulator input point is normal or high	Measure the following applicable voltage at the voltage regulator board A2 connectors ***Output circuit — Measurement points — Voltage reading*** + 5 volt J2-13 (-)to J2-17 (+) — 6 4 ±'0.5 - 5 volt J3-13 (-) to J3-17 (+) — 6.4+± 0.5 + 15 volt J2-4(-) to J2-5 (+) — 16.9 +±0.5 -15 volt J3-4(-) toJ3-5(+) — 16.5 +:±0 5	If the voltage measured is low, the following applicable transistor is the probable cause +5 volt output, transistor ASQ12 -5 volt output, transistor A8Q13 +15 volt output; transistor A7Q10. -15 volt output, transistor A7Q11. If the measured voltage is high, the following applicable transistors are probable causes +5 volt output, transistors A8Q14 through ASQ18 -5 volt output, transistor A7Q19 +15 volt output, transistors A7Q20 and A7Q21. -15 volt output; transistors A7Q22 and A7Q23

Table 5-16. Output Voltage Oscillation, Troulbeshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Output oscillates between approximately zero volts and normal output level.	Oscillation is result of output level adjustment set too high, high voltage fault, or faulty overvoltage detection circuit. Adjust output level adjustment on voltage regulator board A2 to reduce output to proper level.	If output adjustment does not affect oscillation problem, perform step 2.

Table 5-16. Output Voltage Oscillation, Troubleshooting

Step	Symptom	Procedure	Probable cause/corrective action
2	Output adjustment does not affect oscillation	Observe output voltage on oscilloscope and determine if upper level of waveform exceeds overvoltage trip point (see table 5-1 for trip point limits)	If upper level exceeds overvoltage limit, refer to table 5-11. If upper level of waveform Is below the overvoltage trip point, replace voltage regulator board A2 If voltage regulator substitution does not correct fault, reinstall original voltage regulator and perform step 3.
3	Voltage regulator board A2 substitution does not correct fault.	Replace appropriate SCR crowbar diode +5 volt supply: A10CR49 -5 volt supply: A10CR50 +15 volt supply: A10CR51 -15 volt supply: A10CR52	If SCR crowbar replacement does not correct fault, perform step 4
4	SCR crowbar diode is not faulty	Check appropriate current limit resistor for open condition: +5 volt supply A8R82 -5 volt supply A7R87 +15 volt supply A7R88 -15 volt supply A7R90	Replace open resistor

Table 5-17. Excessive Line Frequency Ripple on Outputs, Troubleshooting Procedure

Step	Symptom	Procedure	Probable cause/corrective action
1	Excessive ripple on all outputs.	Refer to table 5-12 for troubleshooting procedure. (See flg. 5-11 for allowable ripple limit on dc outputs.)	
2	Excessive ripple on single output,	Fault Is defective voltage regulator board A2 or output filter. Replace voltage regulator board A2. (See fig. 5-11 for allowable ripple limits on de output.)	If excessive ripple is reduced, voltage regulator was faulty. If ripple is not reduced, reinstall original voltage regulator board. Probable cause is then the output filter capacitor (A9C51, A9Cs2, A9CB8, or A9C64) associated with the de output containing the ripple.
3	Excessive ripple on complementary outputs	Probable cause is defective component in de-to-dc converter (See fig 5-11 for allowable ripple limits on dc outputs)	If ripple is present in +15 volt complementary outputs, perform troubleshooting procedure in table 5-13 If ripple is present on +5 volt outputs, perform troubleshooting as outlined In table 5-14

Table 5-18. Typical Resistance Measurements

From (+)	To (-)	Scale	Reading	Comments
PS1C5(+)	PS1C5(-)	R x 100	12000	
PSl1J-l	PS1J1-2	R x 100	>100KΩ	
PS1J1-2	PS1J1-1	R x 100	>100KΩ	
+5 V (TP)	COM (TP)	R x 100	950Ω	
+15V(TP)	COM(TP)	R x 100	1550Ω	
-15 V (TP)	COM (TP)	R x 100	1650Ω	
-S V (TP)	COM (TP)	R x 100	950Ω	
+5 V (TP)	COM (TP)	R x 10000	50KΩ	With A2J2 and A2J3 disconnected allow one minute charge time
+15 V(TP)	COM (TP)	R x 10000	150KΩ	
-15 V(TP)	COM (TP)	R x 10000	150KΩ	
-5 V (TP)	COM (TP)	R x 10000	50KΩ	

(2) To perform certain measurements as required in the troubleshooting procedures, removal of the power supply top cover and partial removal of other subassemblies are necessary. Removal and replacement procedures are covered in paragraph 5-11. For all resistance and voltage measurements required in the troubleshooting procedures, use a multimeter unless otherwise specified All component reference designators in the troubleshooting procedures are prefixed with the pertinent subassembly reference designator to aid in the physical location of components

5-11. Removal and Replacement Procedures

a. Power Supply PS1. To remove or replace the

Table 5-19. Typical Voltage Measurements

From (+)	To (-)	Scale (+dc)	Reading (in volts)	Comments
PS1C5(+)	PS1C5 (-)	250V	155	120 V ac, 60 Hz input.
PS1R1(top)	PS1C5 (-)	50V	21	PS1R1 located on right side of chassis
A2J2-14	COM (TP)	50 V	19 0	+ 5 V regulator.
A2J2-16	COM (TP)	10V	68	+ 5 V regulator.
A2J2-17	COM (TP)	10 V	6 3	+5 V regulator.
A2J2-18	COM (TP)	10 V	5 7	+5 V regulator.
A2J2-7	COM (TP)	60V	22.5	+15 V regulator..
A2J2-6	COM (TP)	50 V	22 0	+16 V regulator.
A2J2-5	COM (TP)	50V	16 9	+ 15 V regulator.
A2J2-9	COM (TP)	50 V	16 1	+ 15 V regulator.
A2J3-14	COM (TP)	50V	14 5	-5 V regulator.
A2J3-16	COM (TP)	25V	1 75	-5 V regulator.
A2J3-17	COM (TP)	25V	1 25	-5 V regulator.
A2J3-18	COM (TP)	25V	0 6	-5 V regulator.
A2J3-7	COM (TP)	10 V	7 5	-15 V regulator.
A2J3-6	COM (TP)	10 V	6 9	-15 V regulator.
A2J3-5	COM (TP)	25 V	1.15	-15 V regulator.
A2J3-9	COM (TP)	2.5 V	0 60	-15 V regulator.

power supply, refer to the instructions in paragraph 3-37i.

b. Power Supply Top Cover. Remove the thirteen screws labeled A in figure 5-14. Lift top cover and swing back to position shown in figure 5-2, revealing voltage regulator board A2 To replace the top cover, reverse the above procedure.

c. Printed Circuit (Voltage Regulator) Board A2. Remove top cover as instructed in b above. Remove the two retaining screws (fig. 5-2) from each connector (A2J2 and A2J3) on the voltage regulator board and disconnect the cable connectors. Remove the seven screws labeled B in figure 5-14, to free the board from the top cover. Reinstall the voltage regulator board in the reverse order of removal.

d Heat Sink Assemblies A6, A7, and A8.

(1) Remove two retaining screws (fig. 5-15) from one side of the heat sink assembly, then loosen the two retaining screws on the other side of the

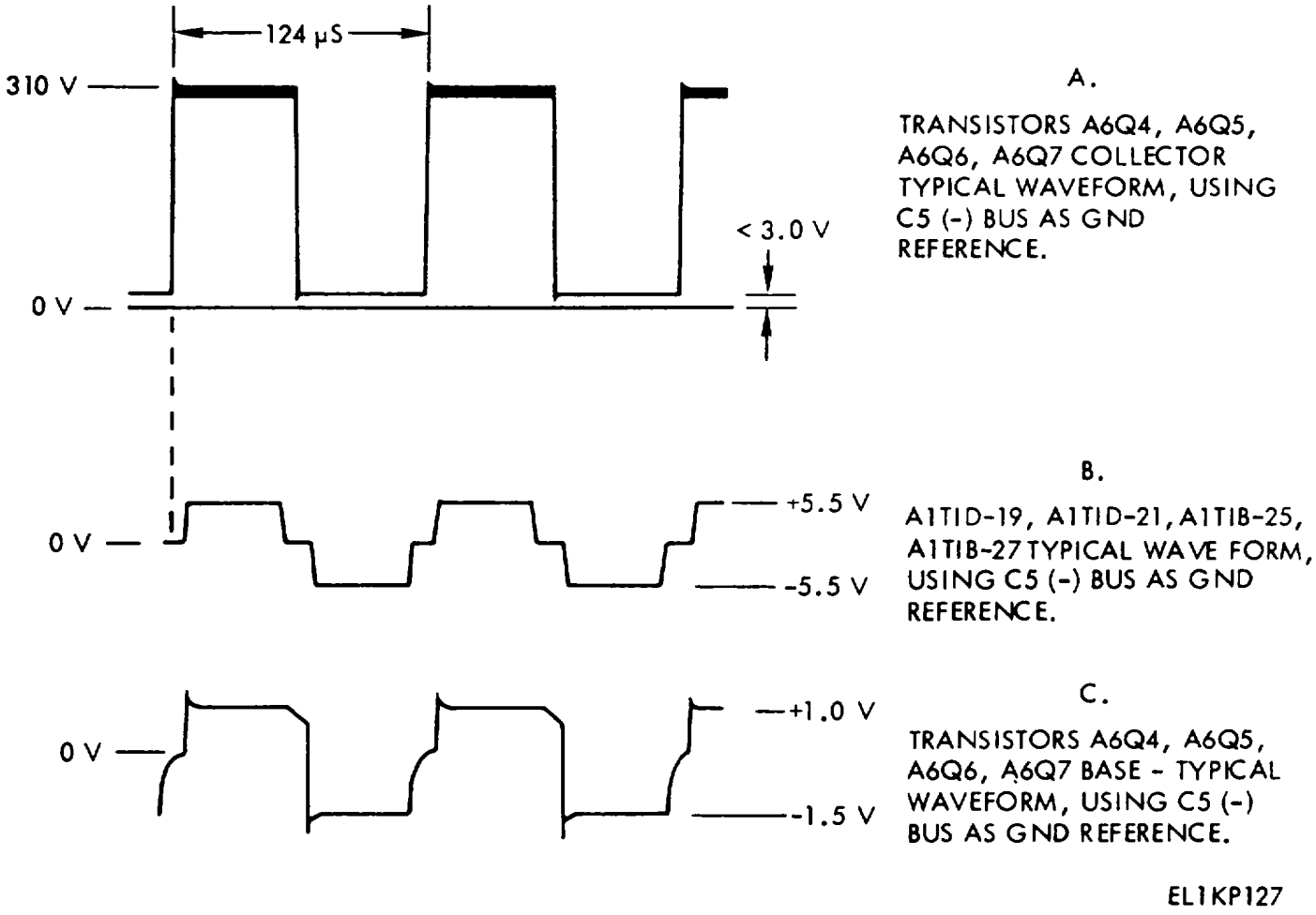


Figure 5-12. Dc-to-dc converter-typical waveforms

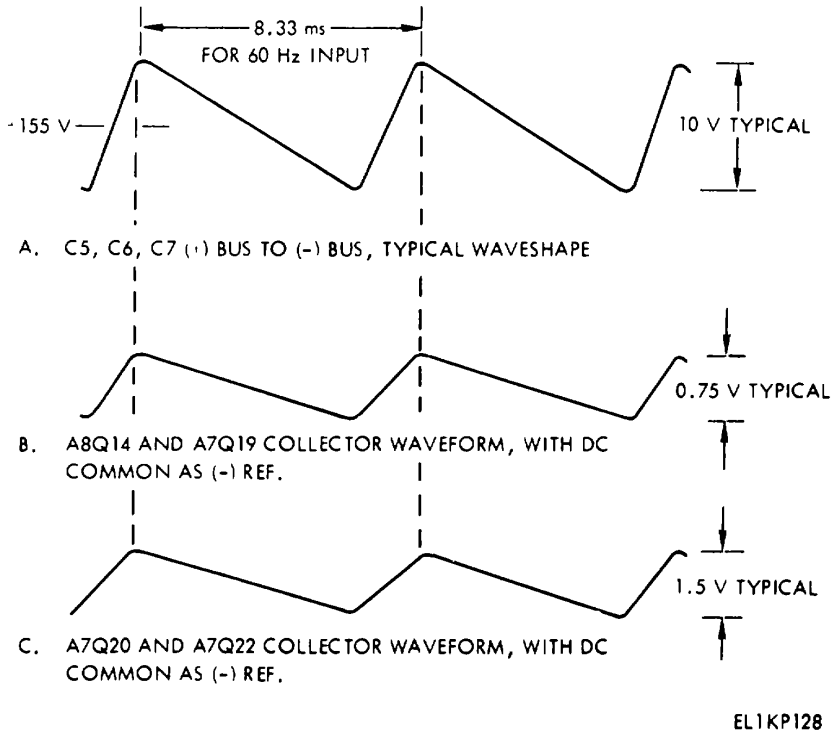


Figure 5-13. Typical input filter and output drive circuit waveforms.

assembly. Slide the heat sink assembly sideways to free it from the loosened screws, and fold it out and away from the power supply chassis as shown in figure 5-15 for access to heat sink assembly components.

(2) When replacing power transistors on a heat sink assembly, be sure to install insulating washers with thermal compound applied to both sides of washers

(3) Replace heat sink assemblies by reversing the order of removal instructions in paragraph (1) above.

e Terminal Board Assembly A9. Loosen and remove heat sink assembly A8 as described in d above, to expose terminal board A9 mounting screws.

Remove the four mounting screws and nuts securing the terminal board to the chassis.

NOTE

It is generally possible to remove most of the components on the terminal board without removing the terminal board from the chassis.

f. SCR Mounting Assembly A10. Remove the two mounting screws located on the side of the power supply adjacent to the SCR mounting assembly. When replacing an SCR on the mounting assembly, be sure to install insulating washers with thermal compound applied to both sides of the washer. When replacing SCR CR49, it is necessary to bend the long lead on CR49 to prevent interference with the top cover of the power supply. While bending the lead, support the lead between the glass seal and the bend to prevent cracking the seal.

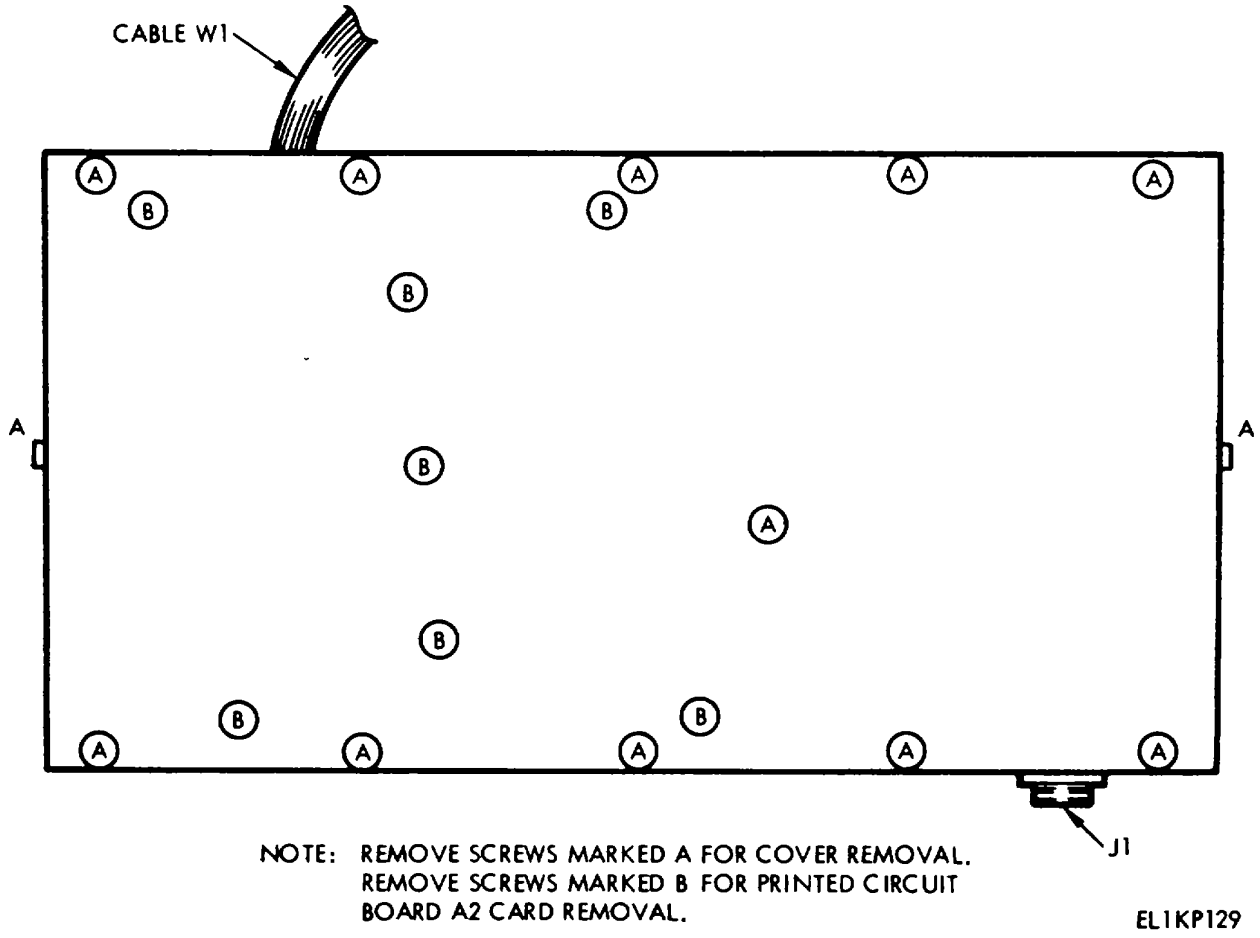


Figure 5-14. Top view of power supply.

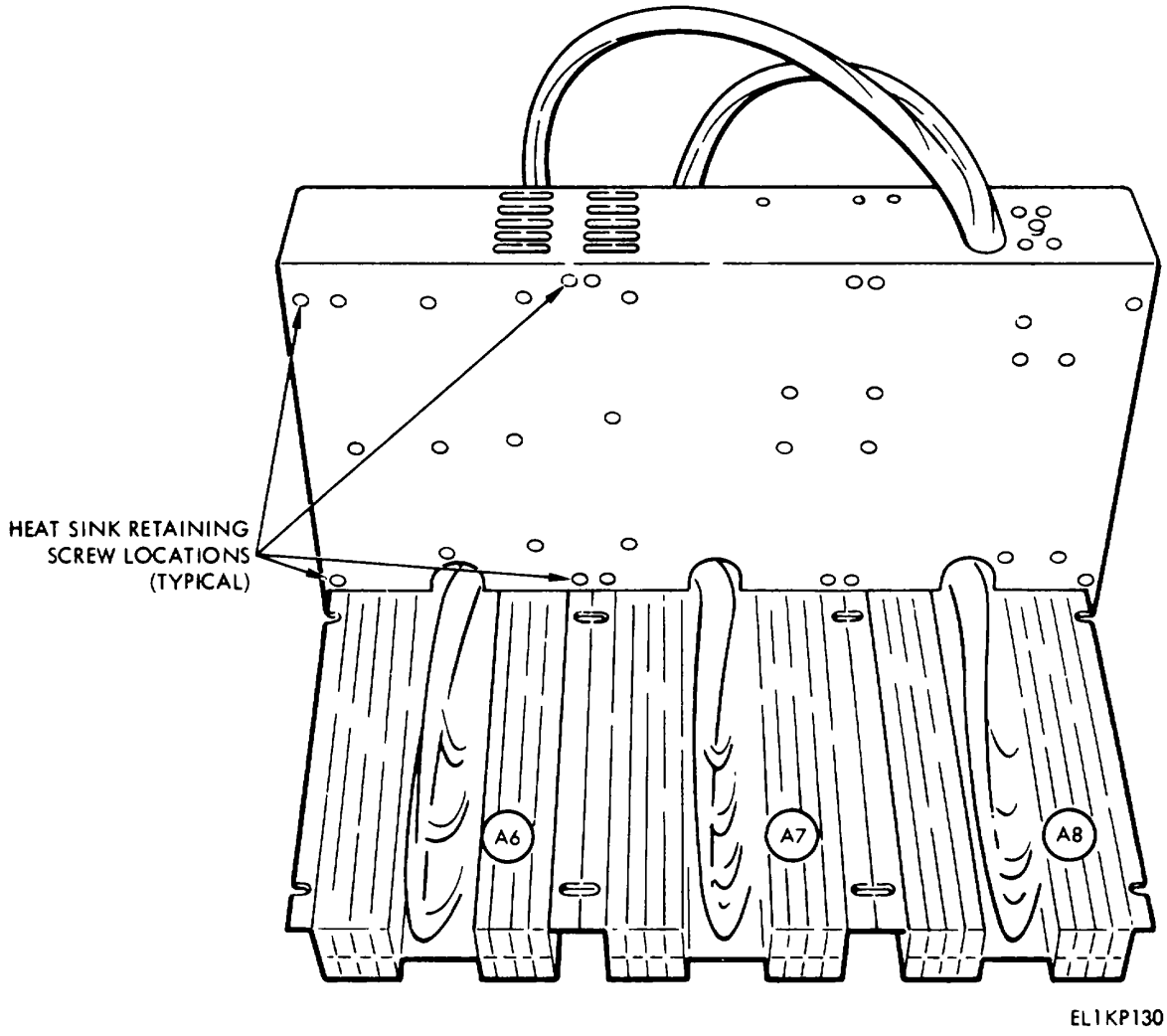


Figure 5-15. Bottom of power supply chassis with heat sinks folded out

APPENDIX A

REFERENCES

TB 11-6625-2838-35	Calibration Procedure for Counter, Error Rate TS-3641/G. (To be published).
TB 11-6625-2839-35	Calibration Procedure for Test Set, Digital Communications TS-3642 (V) I/G (To be published.)
TM 11-5820-803-12	Operator's and Organizational Maintenance Manual: Modem, Digital Data MD-921/G (NSN 5820-00-155-8581).
TM 11-5820-803-34	Direct Support and General Support Maintenance Manual: Modem, Digital Data MD-921/G (NSN 5820-00-155-8581).
TM 11-5820-804-12	Operator's and Organizational Maintenance Manual: Modem, Digital Data MD-920/G (NSN 5820-00-155-8576).
TM 11-5820-804-34	Direct Support and General Maintenance manual for Modem, Digital Data MD - 920/G (NSN 5820-00-155-8576).
TM 11-5820-847-12	Operator's and Organizational Maintenance Manual' Modem, Digital Data MD-1002/G.
TM 11-5820-847-20P	Organizational Maintenance Repair Parts and Special Tools List for Modem, Digital Data MD- 1002/G. (To be published.)
TM 11-6625-2772-14	Operator's and Organizational Maintenance Manual for Test Set Modem TS-3580/G. (To be published.)
TM 11-6625-2838-14	Operator's, Organizational, Direct Support, and General Support Maintenance Manual for Counter, Error Rate TS-3641/G. (To be published.)
TM 11-6625-2838-24P	Organizational, Direct Support and General Support Maintenance Repair Parts and Special Tools Lists for Counter, Error Rate TS-3641/G. (To be published.)
TM 11-6625-2839-14	Operator's, Organizational, Direct Support, and General Support Maintenance Manual for Test Set, Digital Communications TS-3642 (V) I/G. (To be published.)
TM 11-6625-2839-24P	Organizational, Direct Support and General Support Maintenance Repair Parts and Special Tools Lists for Test Set, Digital Communications TS-3642 (V) I/G. (To be published.)
TM 38-750	The Army Maintenance Management System (TAMMS) (To be published)
TM 740-90-1	Administrative Storage of Equipment.
TM 750-244-2	Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command).

APPENDIX B

GLOSSARY OF TERMS

This appendix defines the mnemonics used to identify the signals carried between cards, card files, and subassemblies.

Table B-1. Glossary of Terms

Mnemonic	Description
ALM RST	Alarm Reset
ALPHA MODE 0	Places the error comparator in the Alpha Flunk mode (is low logic level for positions 10, 11, 13, and 14 of the ERROR COUNT thumbwheel).
AUD ALM 1	Audible Alarm.
AUD ALM 2	Audible Alarm
BB 70 OSC	Modulator Test Indication.
B/S I LSBC	Bit Synchronizer, I Channel, Least Significant Bit Complement.
B/S I MSBC	Bit Synchronizer, I Channel, Most Significant Bit Complement.
B/S I SIG NC	Bit Synchronizer, I Channel, Sign Bit Complement
B/S TST RLY	Bit Synchronizer, Test Relay Control Line
B/S Q LSBC	Bit Synchronizer, Q Channel, Least Significant Bit Complement
B/S Q MSBC	Bit Synchronizer, Q Channel, Most Significant Bit Complement.
B/S Q SIONC	Bit Synchronizer, Q Channel, Sign Bit Complement
BUFFM-DICLK	Buffered Mid-Bit I Channel Clock.
BUFFM-DQCLK	Buffered Mid-Bit Q Channel Clock
DEC I LSBC	Decoder I Channel LS9 B Complement.
DEC I MSBC	Decoder I Channel MSB Complement.
DEC I SIGNC	Decoder I Channel Sign Bit Complement.
DM PLL LITE	Demod Phase Lock Fault Indication.
DM PWR LITE	Demod Power Fault Indication.
ECCLKT	Error Comparator, Clock True.
ECDATA	Error Comparator, Data True.
ECDATAMUX	Error Comparator, Multiplexed Data.
ECCLKMUX	Error Comparator, Multlplexed Clock
EC ERROR	Error Comparator, Error Output.
ECPN11	Error Comparator, PN Sequence Generator, Stage 11.
EDEC DATAC	Error Decoder Data Complement.
EDEC I SIGN	Error Decoder I Channel Sign Bit.
EDEC I MSBC	Error Decoder I Channel MSB Complement.
EDEC I LSBC	Error Decoder I Channel LSB Complement.
EDEC OUTCLK	Error Decoder Output Clock.
EDEC Q SIGN	Error Decoder Q Channel Sign Bit
EDEC Q MSBC	Error Decoder Q Channel MSB Complement.
EDEC Q LSBC	Error Decoder Q Channel LSB Complement
EDECRCT	Error Decoder Bit Rate Clock True.
EN CLK RC	Enable Clock Receiver Complement.
ENICF RC	Enable ICF Receiver Complement.
ENMODO	Enable Modem Test (MONITOR ERROR COUNT Thumbwheel Positions 8 through 15).
ENOPERC	Enable Operate Mode Complement
ENSTD RC	Enable Standard Receiver Complement
EN TEST C	Enable Test Mode Complement.
EN TEST I	Enable Test Mode True.
ERROR METG	Error Meter Signal
ERROR MET-	Error Meter Signal Return
EXT ALM 1	External Alarm Contact 1.
EXT ALM 2	External Alarm Contact 2
EXT DEC I LSB +	External Decoder I Channel LSB +
EXT DEC I LSB -	External Decoder I Channel LSB -.

Table B-1. Glossary of Terms - Continued

Mnemonic	Description
EXT DEC I MSB +	External Decoder I Channel Most Significant Bit (+)
EXT DEC I MSB -	External Decoder I Channel Most Significant Bit (-)
EXT DEC I SIGN +	External Decoder I Channel Sign +
EXT DEC I SIGN -	External Decoder I Channel Sign -
EXT DEC Q LSB +	External Decoder Q Channel Least Significant Bit +
EXT DEC Q MSB +	External Decoder Q Channel Most Significant Bit +
EXT DEC Q MSB -	External Decoder Q Channel Most Significant Bit -
EXT DEC Q SIGN +	External Decoder Q Channel Sign +.
EXT DEC Q SIGN -	External Decoder Q Channel Sign -
EXTDEC R+	External Decoder Bit Rate +
EXT DEC R-	External Decoder Bit Rate -
FLK 7	Filter and Distribution Amplifier Card Relay 7
FLK5K6PLLKSPAK4	Filter and Distribution Amplifier Card Relay 5
FLMODDAT	Filtered Modulator Output.
FMEXTENCI +	From External Encoder I Channel +
FMEXTENCI -	From External Encoder I Channel -
FMEXTENCQ +	From External Encoder Q Channel +
FMEXTENCQ -	From External Encoder Q Channel -.
FMEXTENC2R +	From External Encoder 2X Bit Rate +
FMEXTENC2R -	From External Encoder 2X Bit Rate -.
FROM EXT DEC +	From External Decoder +
FROM EXT DEC -	From External Decoder -
FROM EXT DECC(+)	From External Decoder C (+)
FROM EXT DECC(-)	From External Decoder C (-).
I AGC	I Channel AGC.
I CHAN REF	I Channel Reference Carrier
ICHIN	I Channel Input to Bit Sync
I INT OUT	I Channel Integrator Output
I SAMP	I Channel Sample Clock
ICF1	ICF Receiver Output 1
ICF2	ICF Receiver Output 2
ICF 75 B+ IN	ICF 75-Ohm Balanced Input +
ICF 75 B- IN	ICF 75-Ohm Balanced Input -
ICF RCVDAT	ICF Receive Data
ICF Test Sig	ICF Test Signal
INCLK +	Input Clock +.
INCLK -	Input Clock -
INSTD +	Input Standard Data +.
INSTD -	Input Standard Data -
LFOVERFLOWC	Loop Filter Overflow Complement
LFUNDFLOWT	Loop Filter Underflow True
LMP GND	Lamp Ground.
METIAGC	I Channel AGC Meter Signal.
MET B/S GND	Bit Sync Meter Ground
MODDAT	Modulator Output
MOD PWRC	Modulator Power Fault.
MOD PWR LITE	Modulator Power Fault Indicator
MPWRI	Meter Indication for de Power
MQAGC	Q Channel AGC Meter Signal
OAUITOSW	Error Comparator Auto Sync Complement.
ODECDATT	Output Data True
OENTST	Enable Test for Positions 8 through 15 of the ERROR COUNT Thumbwheel
PDETLSB	Phase Detector LSB
PDETMSB	Phase Detector MSB
PERROR SIGN	Phase Error Sign
PERROR MSB	Phase Error MSB
PERROR LSB	Phase Error LSB
PERROR TRANS	Phase Error Transition
PERROR CLKT	Phase Error Clock True
PERROR CLKC	Phase Error Clock Complement
PLLIND	Phase Lock Indication
PNCLK I	PN Sequence Clock Output
PNSEQCLK	PN Sequence Generator Clock Input.
PNSEQ I	PN Sequence for I Channel

Table B-1. Glossary of Terms - Continued

Mnemonic	Description
POSST	Error Comparator Synchronization Pulse
QCHRTN	Q Channel Return
Q INT OUT	Q Channel Integrator Output
R1-10M	Receiver Symbol Rate Decades - 1 to 1OM
R100K-1M	Receiver Symbol Rate Decades - 1OOK to 1M
RlOK-100K	Receiver Symbol Rate Decades - 10 K to 100 K.
R2CLKC	Receiver 2X Symbol Rate Clock
R15MIX	Receive 15 MHz Mixer Input
R Bit Sync Lite	Receiver BIT SYNC FAULT Indicator.
RBS ALM	Receive Bit Sync Fault.
RBSITST	Receive Bit Sync I Channel Test Input.
RBSQTST	Receive Bit Sync Q Channel Test Input.
RDAC 1	Receiver D/A Converter Input -1
RDAC 2	Receiver D/A Converter Input -2.
RDAC 3	Receiver D/A Converter Input -3
RDAC 4	Receiver D/A Converter Input -4
RDAC 5	Receiver D/A Converter Input -5
RDAC 6	Receiver D/A Converter Input -6
RDAC 7	Receiver D/A Converter Input -7
RDAC 8	Receiver D/A Converter Input -8
RDACOUT	Receive D/A Converter Output
RDACOUTR	Receive D/A Converter Return
RDIFFI	Receive Differential Coding
RDUMP	Receive Synthesizer Dump
Receive FLT	Receive Fault
REXT I	Receive External Coder Enable
RF PLL Lite	Receive Phase-Lock Fault
RLDPGM	Receive Load Program
RMIXD	30 +10 MHz to Receive Divider.
RMIXO	Receive Synthesizer 30 +10 MHz From Mixer/Output Amplifier
RPDO	Receive Program Divider Input
RPSKI	Receive BPSK Enable
RPU	Symbol Rate Digits From Thumbwheel
RRD-8	Symbol Rate Switch Setting Between 10000 and 12499 KB/S
RRD-4	Symbol Rate Switch Setting Between 12500 and 24999 KB/S
RRD-2	Symbol Rate Switch Setting Between 25000 and 49999 KB/S
RRD-1	Symbol Rate Switch Setting Between 50000 and 99999 KB/S
RSAMP	Receive Sample From Programmable Divider
RSYNTST	Receive Synthesizer Test
RTXLO	Receive Synthesizer 15- MHz TCXO Output
RVCONT	Control to Receive 15-MHz VCO
RX FREQ	Receive Clock Frequency
RX PWR C	Receive Power Fault
SEQ GEN CLK	PN Sequence Generator Clock
STBCR	Stable Clock
TI-10M	Transmit Data Rate Decades-1 to 1OM
TlOK-100K	Transmit Data Rate Decades- 10K to 100 K
TIOOK-1M	Transmit Data Rate Decades-100K to 1M
T45MA	Transmit 45-MHz Amplifier Output
T15MIX	Transmit 15-MHz Amplifier Output
T45MIX	Transmit 45-MHz Input to Mixer/Output Amplifier
T45MVCO	Transmit 45-MHz VCO Output
TBIT SYNC LITE	Transmit Bit Synchronizer Fault Indicator
TBSALMO	Transmit Bit Synchronizer Fault.
TCLKDLYC	Transmit Clock Delayed Complement
TCLKT	Transmit Clock True
TCLKTDLYT	Transmit Clock Delayed True.
TDAC OUT	Transmit D/A Converter Output
TDATCT	Transmit Data From Input Interface.
TDATST	Transmit Data From Synchronizer.
TDEET	Transmit Data To External Coder
TEXT I	Transmit External Coding Control.
TEXT 2 CLKT	Transmit External Coding 2X Data Rate Clock
TIEXT	Transmit I Channel Data From External Coder.

Table B-1. Glossary of Terms - Continued

Mnemonic	Description
TLDPGM	Transmit Load Program.
TLFSIGN	Transmit Loop Filter Sign Input.
TLFIRAN	Transmit Loop Filter Transition Input.
TMIXD	30 4 10MHz to Transmit Reference Divider
TMXO	Transmit Mixer/Output Amplifier Output
TOEXTENCD +	Data to External Encoder +.
TOEXTENCD -	Data to External Encoder -.
TOEXTENCR +	Clock to External Coder +
TOEXTENCR -	Clock to External Coder -
TPD	Transmit Program Divider Input.
TPDM	Transmit Program Divider Mode Input
TQEXT	Transmit Q Channel Data From External Coder
Transmit FLT	Transmit Fault Indication
TRCEET	Transmit Data Rate Clock to External Coder.
TR2CEET	Transmit 2X Data Rate Clock to External Coder.
TRD 1	Data Rate Switch Setting Between 50000 and 99999 KB/S.
TRD 2	Data Rate Switch Setting Between 25000 and 49999 KB/S.
TRD 4	Data Rate Switch Setting Between 12500 and 24999 KB/S.
TRD 8	Data Rate Switch Setting Between 10000 and 12499 KB/S.
TSCTCXO	45 MHz to Stable Clock
TSEQQ	Q Channel Test Sequence.
TSTALTCKO	Alternate Test Clock
TSTALTDO	Alternate Test Data
TSTCLKCNTL	Test Clock Control
TTSTTDCKO	Standard Test Clock
TSTSTDDO	Standard Test Data.
TST SW	Test Switch.
TST SW GND	Test Switch Ground
TTXLO	Transmit Synthesizer 15-MHz TCXO Output.
TVCO	Transmit 15-MHz VCO Output
TVCONT	Control to Transmit Bit Sync
TXBSDTT	Transmit Bit Synchronizer Data.

APPENDIX C

POWER SUPPLY PS1 WIRE LIST

Table C-1. Power Supply PS1 Wire List

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
J1	1	A1	35	18	W	
J1	2	A1	36	18	BK	
J1	3	A1	30	22	G	
A1	1	CR17	A	18	Y	
A1	2	C21	(-)	18	W/O	
A1	3	CR18	A	18	Y	
A1	4	CR19	A	18	BL	
A1	5	C22	(-)	18	V	
A1	6	CR20	(A)	18	BL	
A1	7	Q4	C	20	R	Twisted pair.
A1	8	C5	(+)	20	W/R	
A1	9	Q5	C	20	BK	Twisted pair.
A1	10	CR15	C	18	BR	
A1	10	CR11	A	24	BR	
A1	11	C20	(+)	18	W/BR	
A1	11	C18	(-)	24	W/BR	
A1	12	CR16	C	18	BR	
A1	12	CR12	A	24	BR	
A1	13	Q6	C	20	W	Twisted pair.
A1	14	C5	(+)	20	W/R	
A1	15	Q7	C	20	GY	Twisted pair.
A1	16	—				Not used.
A1	17	—				Not used.
A1	18	—				Not used.
A1	19	E4		22	GY	Twisted pair.
A1	20	A3	D	22	R	
A1	21	E3		22	W	Twisted pair.
A1	22	CR13	C	16	BK	2 wires.
A1	22	CR9	A	22	BK	
A1	23	C19	(+)	16	W/BK	2 wires.
A1	23	C17	(-)	22	W/BK	
A1	24	CR14	C	16	BK	2 wires.
A1	24	CR10	A	22	BK	
A1	25	E2		22	BK	Twisted pair.
A1	26	A3	A	22	R	
A1	27	E1		22	GY	Twisted pair.
A1	28	—				Not used.
A1	29	—				Not used.
A1	30	J1	3	22	G	
A1	31	—				Not used.
A1	32	—				Not used.
A1	33	—				Not used.
A1	34	CR3	C	18	W/BK	
A1	35	J1	1	18	W	
A1	36	J1	2	18	BK	
A1	37	CR2	C	18	W/BK	
CR2	A	C5	(-)	18	W/GY	

Table C-1. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
CR2	C	A1	37	18	W/BK	
CR3	C	A1	34	18	W/BK	
CR5	C	C5	(+)	18	W/R	
CR9	A	A1	22	22	BK	
CR10	A	A1	24	k22	BK	
CR11	A	A1	10	24	BR	
CR12	A	A1	12	24	BR	
CR13	C	A1	22	16	BK	2 wires.
CR14	C	A1	24	16	BK	2 wires.
CR15	C	A1	10	18	BR	
CR16	C	A1	12	18	BR	
CR17	A	A1	1	18	Y	
CR18	A	A1	3	18	Y	
CR19	A	A1	4	18	BL	
CR20	A	A1	6	18	BL	
CR49	A	TP1		24	R	
CR49	A	C51	(+)	18	R	
CR49	G	P2	12	24	R	
CR49	C	C51	(-)	18	W/R	
CR50	A	C52	(+)	22	W/G	
CR50	G	P3	12	24	W/G	
CR50	C	TP2		24	G	
CR50	C	C52	(-)	22	G	
CR51	A	TP3		24	O	
CR51	A	C53	(+)	22	O	
CR51	G	P2	1	24	O	
CR51	C	C53	(-)	22	W/O	
CR52	A	C54	(+)	22	W/V	
CR52	G	P3	1	24	W/V	
CR52	C	C54	(-)	22	V	
CR52	C	TP4		24	V	
C5	(+)	R1	A	22	W/R	
C5	(+)	CR5	C	18	W/R	
C5	(+)	A1	8	20	W/R	
C5	(+)	A1	14	20	W/R	
C5	(-)	Q6	E	20	W/G	
C5	(-)	CR2	A	18	W/G	
C5	(-)	Q5	E	20	W/G	
C5	(-)	A3	B	22	W/G	
C17	(+)	Q12	C	22	BK/BL	
C17	(+)	P2	14	22	BK/BL	
C17	(-)	A1	23	22	W/BK	
C18	(+)	Q13	C	24	BK/Y	
C18	(+)	P3	14	24	BK/Y	
C18	(-)	A1	11	24	W/BR	
C19	(+)	A1	23	16	W/BK	2 wires.
C19	(+)	Q15	C	16	W/BK	
C19	(+)	Q17	C	16	W/BK	
C19	(-)	C51	(-)	16	W/R	2 wires.
C20	(+)	A1	11	18	W/BR	
C20	(+)	Q19	C	18	W/BR	
C20	(-)	C52	(-)	18	G	
C21	(+)	Q21	C	18	W/Y	
C21	(+)	P2	7	24	W/Y	
C21	(-)	A1	2	18	W/O	
C21	(-)	C53	(-)	18	W/O	
C22	(+)	Q23	C	18	V	
C22	(+)	P3	7	24	V	
C22	(-)	A1	5	18	V	
C22	(-)	C54	(-)	18	V	

Table C-1. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
C22	(-)	A1	5	18	V	
C51	(+)	E10		16	R	
C51	(+)	E13		16	R	
C51	(+)	CR49	A	18	R	
C51	(+)	P2	19	24	R	
C51	(+)	P2	20	24	R	Twisted pair.
C51	(+)	PS1P1	D	20	R	+5 V.
C51	(+)	PS1P1	E	20	R	+5 V.
C51	(+)	PS1P1	H	20	R	+5 V.
C51	(+)	PS1P2	H	20	R	+5 V.
C51	(+)	PS1P2	E	20	R	+5 V.
C51	(+)	PS1P2	J	20	R	+5 V.
C51	(+)	PS1P2	D	20	R	+5 V.
C51	(-)	C19	(-)	16	W/R	2 wire
C51	(-)	CR49	C	18	W/R	
C51	(-)	P2	13	24	W/R	
C51	(-)	P2	15	24	W/R	Twisted pair.
C51	(-)	PS1P2	A	16	W/R	+5 V COM.
C51	(-)	PS1P1	A	16	W/R	+5 V COM.
C51	(-)	TP5		24	W/R	
C52	(+)	E5		18	W/G	
C52	(+)	CR50	A	22	W/G	
C52	(+)	P3	19	24	W/G	
C52	(+)	P3	20	24	W/G	Twisted pair.
C52	(+)	PS1P2	C	16	W/G	-5 V COM.
C52	(+)	PS1P1	C	16	W/G	-5 V COM.
C52	(-)	C20	(-)	18	G	
C52	(-)	CR50	C	22	G	
C52	(-)	P3	13	24	G	
kC52	(-)	P3	15	24	G	Twisted pair.
C52	(-)	PS1P1	F	20	G	-5 V.
C52	(-)	PS1P1	K	20	G	-5 V.
C52	(-)	PS1P2	F	20	G	-5 V.
C53	(+)	E6		18	O	
C53	(+)	CR51	A	22	O	
C53	(-)	P2	10	24	O	
C53	(-)	P2	11	24	O	Twisted pair.
C53	(+)	PS1P2	P	20	O	+15 V.
C53	(+)	PS1P1	L	20	O	+15 V.
C53	(+)	PS1P1	P	20	O	+15 V.
C53	(+)	PS1P1	R	20	O	+15 V.
C53	(+)	PS1P1	T	20	O	+15 V.
C53	(+)	PS1P1	U	20	O	+15 V.
C53	(-)	C21	(-)	18	W/O	
C53	(-)	CR51	C	22	W/O	
C53	(-)	P2	4	24	W/O	
C53	(-)	P2	8	24	W/O	Twisted pair.
C53	(-)	PS1P1	W	16	W/O	+15 V COM.
C53	(-)	PS1P2	W	16	W/O	+15 V COM.
C54	(+)	E7		18	W/V	
C54	(+)	CR52	A	22	W/V	
C54	(+)	P3	10	24	W/V	
C54	(+)	P3	11	24	W/V	Twisted pair.
C54	(+)	PS1P1	X	16	W/V	-15 V COM.
C54	(+)	PS1P2	X	16	W/V	-15 V COM.
C54	(-)	C22	(-)	18	V	
C54	(-)	CR52	C	22	V	
C54	(-)	P3	4	24	V	
C54	(-)	P3	8	24	V	Twisted pair.
C54	(-)	PS1P1	J	20	V	-15 V.

Table C-1. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
C54	(-)	PS1P1	S	20	V	-15 V.
C54	(-)	PS1P1	V	20	V	-15 V.
C54	(-)	PS1P2	S	20	V	-15 V.
C51	(-)	C55				
C55		GND				
PS1P1	D	C51	(+)	20	R	+5 V.
PS1P1	E	C51	(+)	20	R	+5 V.
PS1P1	H	C51	(+)	20	R	+5 V.
PS1P2	H	C51	(+)	20	R	+5 V.
PS1P2	E	C51	(+)	20	R	+5 V.
PS1P2	J	C51	(+)	20	R	+5 V.
PS1P2	D	C51	(+)	20	R	+5 V.
PS1P2	A	C51	(+)	16	W/R	+5 V COM.
PS1P1	A	C51	(-)	16	W/R	+5 V COM.
PS1P2	C	C52	(+)	16	W/G	-5 V COM.
PS1P1	C	C52	(+)	16	W/G	-5 V COM.
PS1P1	F	C52	(-)	20	G	-5 V.
PS1P1	K	C52	(-)	20	G	-5 V.
PS1P2	F	C52	(-)	20	G	-5 V.
PS1P2	P	C53	(+)	20	O	+15 V.
PS1P1	L	C53	(+)	20	O	+15 V.
PS1P1	P	C53	(+)	20	O	+15 V.
PS1P1	R	C53	(+)	20	O	+15 V.
PS1P1	T	C53	(+)	20	O	+15 V.
PS1P1	U	C53	(+)	20	O	+15 V.
PS1P1	W	C53	(-)	16	W/O	+15 V COM.
PS1P2	W	C53	(-)	16	W/O	+15 V COM.
PS1P1	X	C54	(+)	16	W/V	-15 V COM.
PS1P2	X	C54	(+)	16	W/V	-15 V COM.
PS1P1	J	C54	(-)	20	V	-15 V.
PS1P1	S	C54	(-)	20	V	-15 V.
PS1P1	V	C54	(-)	20	V	-15 V.
PS1P2	S	C54	(-)	20	V	-15 V.
TP1		CR49	A	24	R	
TP2		CR50	C	24	G	
TP3		CR51	A	24	O	
TP4		CR52	C	24	V	
TP5		C51	(-)	24	W/R	
Q4	C	A1	7	20	R	Twisted pair.
Q5	C	A1	9	20	BK	Twisted pair.
Q5	E	C5	(-)	18	W/G	
Q6	C	A1	13	20	W	Twisted pair.
Q7	C	A1	15	20	G	Twisted pair.
Q10	C	P2	5	24	R	
Q10	B	P2	6	24	W	
Q11	C	P3	5	24	O	
Q11	B	P3	6	24	Y	
Q12	C	C17	(+)	22	BK/BL	
Q12	B	P2	16	24	W/BL	
Q12	E	P2	17	24	Y	
Q13	C	C18	(+)	24	BK/Y	
Q13	B	P3	16	24	W	
Q13	E	P3	17	24	G	
Q13	E	Q19	B	24	G	
Q14	E	P2	18	24	W/BK	
Q15	C	C19	(+)	16	W/BK	
Q17	C	C19	(+)	16	W/BK	
Q19	C	C20	(+)	18	W/BR	
Q19	E	P3	18	24	W/BR	
Q19	B	Q13	E	24	G	

Table C-1. Power Supply PS1 Wire List - Continued

From		To		Wire		Remarks
Symbol number	Pin	Symbol number	Pin	Size	Color	
Q20	E	P2	9	24	G	
Q21	C	C21	(+)	18	W/Y	
Q22	E	P3	9	24	Y	
Q23	C	C22	(+)	18	V	
R1	A	C5	(+)	22	W/R	
R1	B	A3	E	22	W/R	
E1		A1	27	22	GY	Twisted pair.
E2		A1	25	22	BK	
E3		A1	21	22	W	
E4		A1	19	22	G	Twisted pair.
E5		C52	(+)	18	W/G	
E6		C53	(+)	18	O	
E7		C54	(+)	18	W/V	
E10		C51	(+)	16	R	
E13		C51	(+)	16	R	
A3	A	A1	26	22	R	
A3	B	C5	(-)	22	W/G	
A3	C	—				Not used.
A3	D	A1	20	22	R	
A3	E	R1	B	22	W/R	
P2	1	CR51	G	24	O	
P2	2	—				Not used.
P2	3	–				Not used.
P2	4	C53	(-)	24	W/O	
P2	5	Q10	C	24	R	
P2	6	Q10	B	24	W	
P2	7	C21	(+)	24	W/Y	
P2	8	C53	(-)	24	W/O	Twisted pair.
P2	9	Q20	E	24	G	
P2	10	C53	(+)	24	O	
P2	11	C53	(+)	24	O	Twisted pair.
P2	12	CR49	G	24	R	
P2	13	C51	(-)	24	W/R	
P2	14	C17	(+)	22	BK/BL	
P2	15	C51	(-)	24	W/R	Twisted pair.
P2	16	Q12	B	24	W/BL	
P2	17	Q12	E	24	Y	
P2	18	Q14	E	24	W/BK	
P2	19	C51	(+)	24	R	
P2	20	C51	(+)	24	R	
P3	1	CR52	G	24	W/V	
P3	2	—				Not used.
P3	3	—				Not used.
P3	4	C54	(-)	24	V	
P3	5	Q11	C	24	O	
P3	6	Q11	B	24	Y	
P3	7	C22	(+)	24	V	
P3	8	C54	(-)	24	V	Twisted pair.
P3	9	Q22	E	24	Y	
P3	10	C54	(+)	24	W/V	
P3	11	C54	(+)	24	W/V	Twisted pair.
P3	12	CR50	G	24	W/G	
P3	13	C52	(-)	24	GY	
P3	14	C18	(+)	24	BK/Y	
P3	15	C52	(-)	24	G	Twisted pair.
P3	16	Q13	B	24	W	
P3	17	Q13	E	24	G	
P3	18	Q19	E	24	W/BR	
P3	19	C52	(+)	24	W/G	
P3	20	C52	(+)	24	W/G	Twisted pair.

By Order of the Secretaries of the Army, the Navy, and the Air Force:

BERNARD W. ROGERS
General United States Army
Chief of Staff

Official:

PAUL T. SMITH
Major Genera4 United States Army
The Adjutant General

EARL B. FOWLER
Rear Admiral, United States Navy
Commander, Naval Electronics
Systems Command

DAVID C. JONES, General, USAF
Chief of Staff

Official:

F. M. ROGERS, General USAF
Commander, Air Force Logistics Command

Distribution:

Active Army.

USASA (2)
COE (1)
TSG (1)HISA (Ft Monmouth) (33)
USAARENBD (1)
DARCOM (1)
TECOM (2)
USACC (4)
MDW (1)
Armies (2)
Corps (2)
Instl (2) except
- Ft Gillem (10)
- Ft Gordon (10)
- Ft Huachuca (10)
- Ft Carson (5)
- SAAD (30)
- LBAD (14)

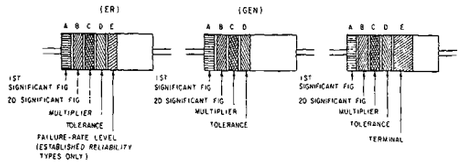
TOAD (14)
SHAD (3)

Ft Richardson (ECOM Ofc) (2)
Svc Colleges (1)
USAICS (3)
USAADS (2)
USAFAS (2)
USAARMS (2)
USAIS (2)
USAES (2)
MAAG (1)
USARMIS (1)
USAERDAA (1)
USAERDAW (1)
Sig FLDMS (1)

ARNG & USAR: None.

For explanation of abbreviations used, see AR 310-50.

*U.S. GOVERNMENT PRINTING OFFICE: 1996 - 406-421 (51320)



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS AND INDICATES TYPE OF TERMINAL.

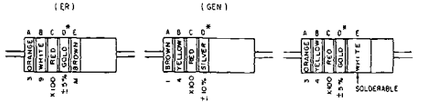
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 1OR0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED. IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

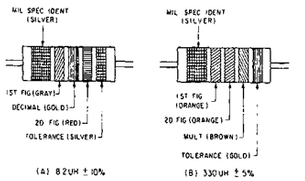
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD

A COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS



COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES AT A. AN EXAMPLE OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN AT B. THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED

TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL

B COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB

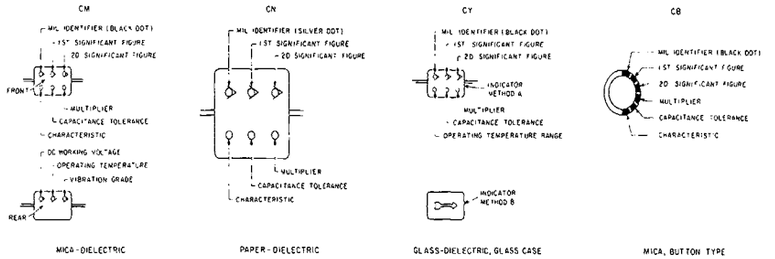


TABLE 3 — FOR USE WITH STYLES CM, CN CY AND CB

COLOR	MIL ID	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE CM	CN	CY	CB	CHARACTERISTIC CM	CN	CB	DC WORKING VOLTAGE CM	OPERATING TEMP RANGE CY CM	VIBRATION GRADE CM
BLACK	CM CY CB	0	0	1			±20%	±20%	A				-55°TO+70°C	10-55 HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55°TO+85°C	
ORANGE		3	3	000		±30%			D		D	300		
YELLOW		4	4	10 000					E				-55°TO+125°C	10-2 000 HZ
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55°TO+30°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						

TABLE 4 — TEMPERATURE COMPENSATING STYLE CC

COLOR	TEMPERATURE COEFFICIENT*	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE: CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	MIL ID
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1 000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

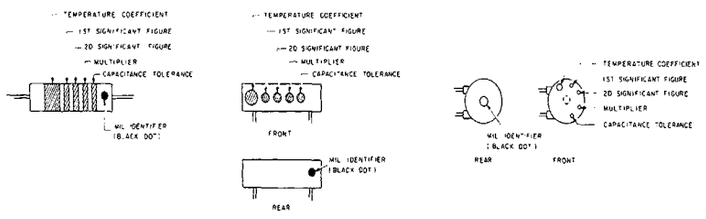
1 THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.

2 LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-11015OC RESPECTIVELY.

3 LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.

4 TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

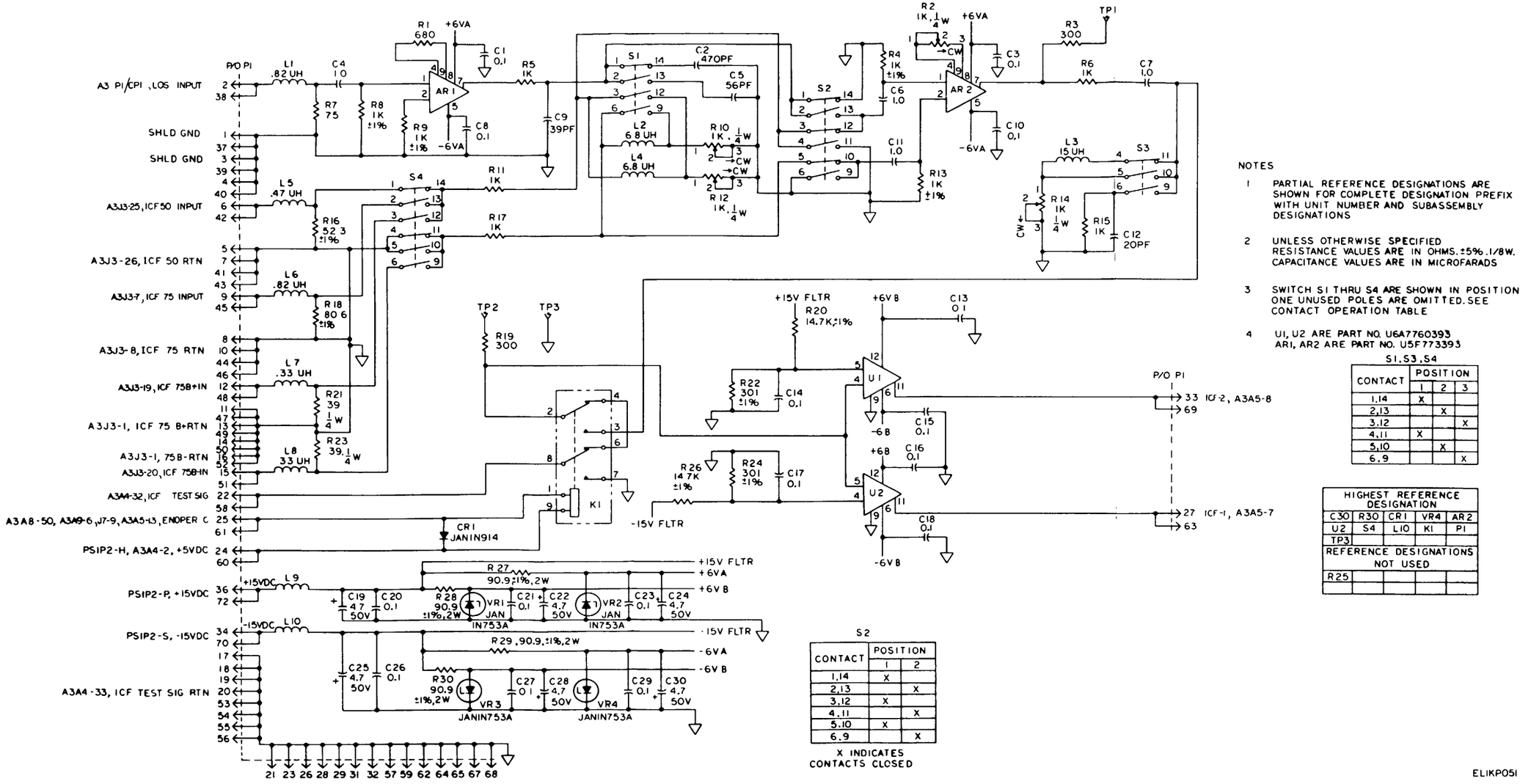
* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.



C COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

ESC FM 913 73

Figure FO-1. Color code markings for MILSTD resistors, inductors, and capacitors.



NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATIONS
2. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS, ±5%, 1/8W. CAPACITANCE VALUES ARE IN MICROFARADS
3. SWITCH S1 THRU S4 ARE SHOWN IN POSITION ONE UNUSED POLES ARE OMITTED. SEE CONTACT OPERATION TABLE
4. U1, U2 ARE PART NO. U6A7760393 AR1, AR2 ARE PART NO. U5F773393

S1, S3, S4

CONTACT	POSITION 1	2	3
1,14	X		
2,13		X	
3,12			X
4,11	X		
5,10		X	
6,9			X

S2

CONTACT	POSITION 1	2
1,14	X	
2,13		X
3,12	X	
4,11		X
5,10	X	
6,9		X

X INDICATES CONTACTS CLOSED

HIGHEST REFERENCE DESIGNATION				
C30	R30	CR1	VR4	AR2
U2	S4	L10	K1	P1
TP3				
REFERENCE DESIGNATIONS NOT USED				
R25				

ELIKP051

Figure FO-2. LOS/cable receiver and decoder, A3A2 (SM-D-742089), schematic diagram.

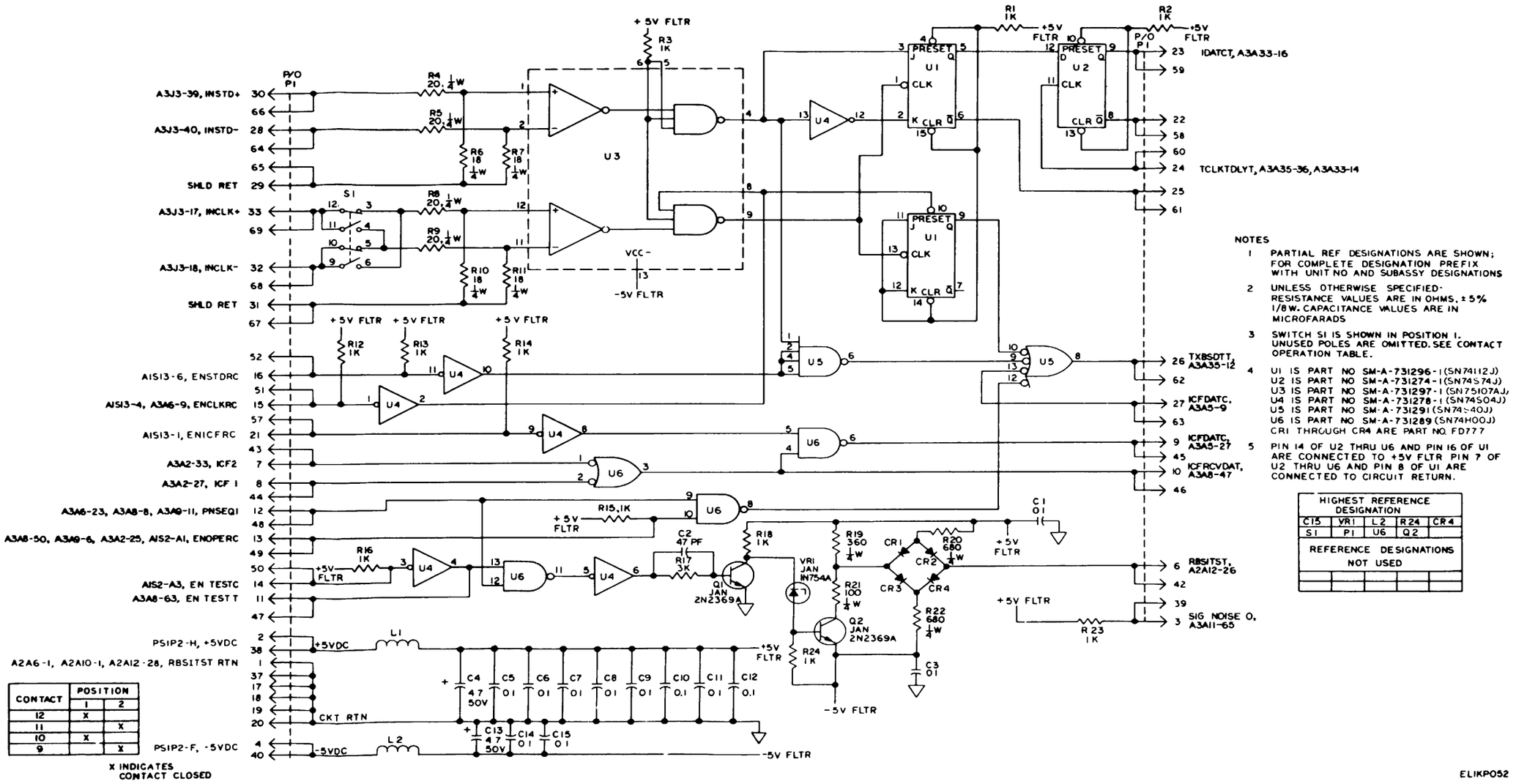


Figure FO-3. Input interface, A3A5 (SM-D-742037), schematic diagram.

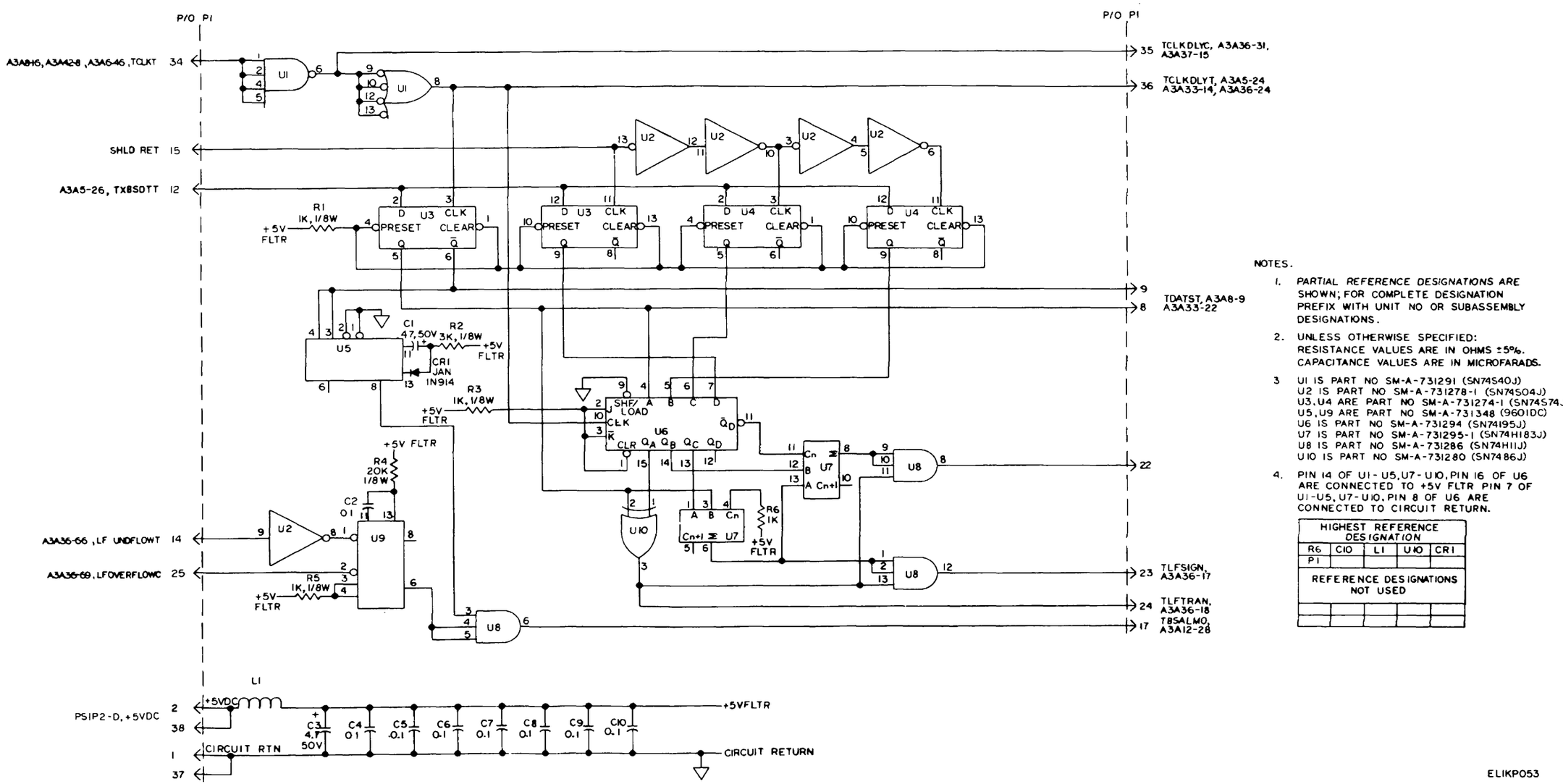


Figure FO-4. Transmit bit detector, A3A35 (SM-D-742045), schematic diagram.

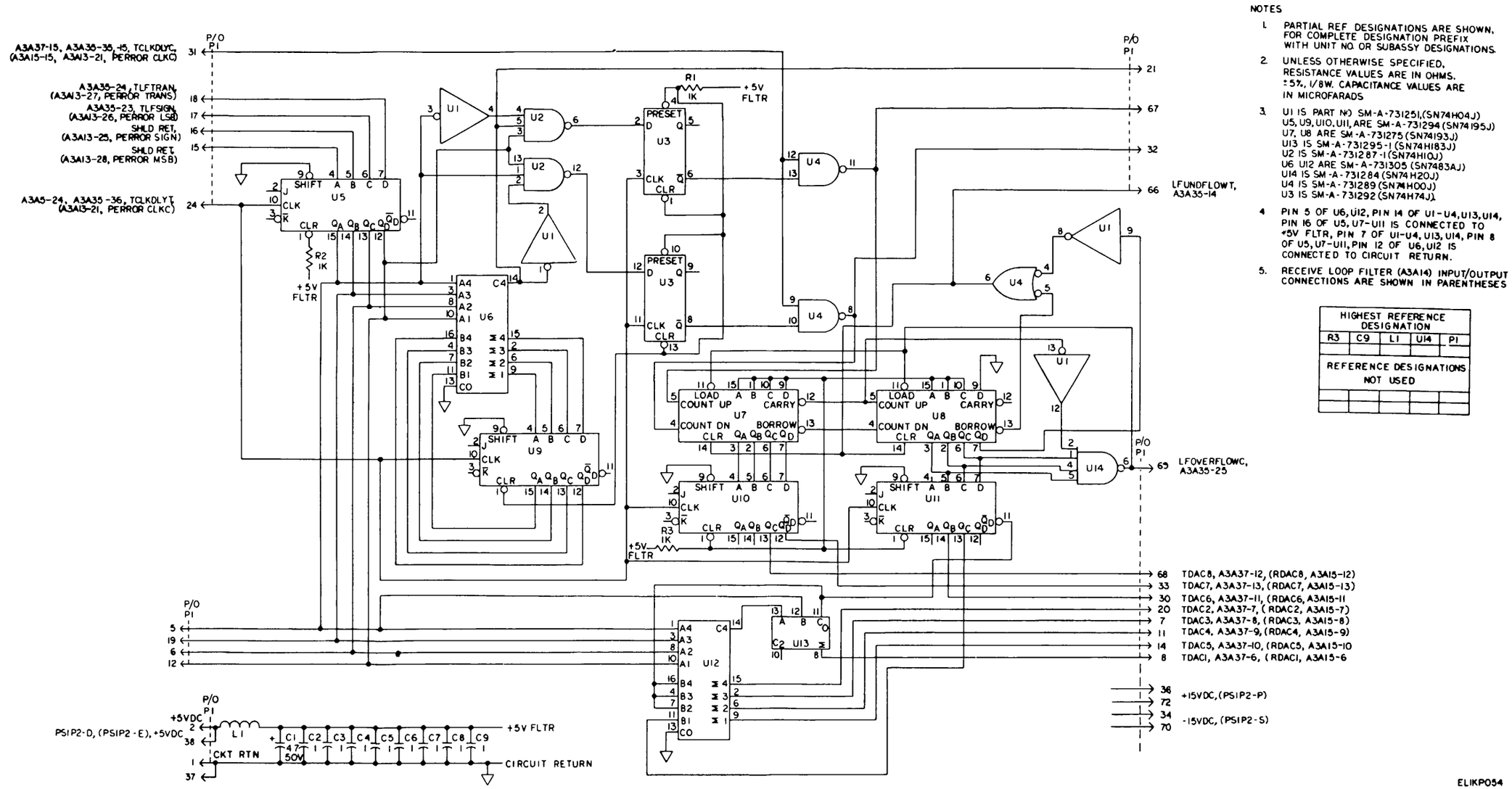
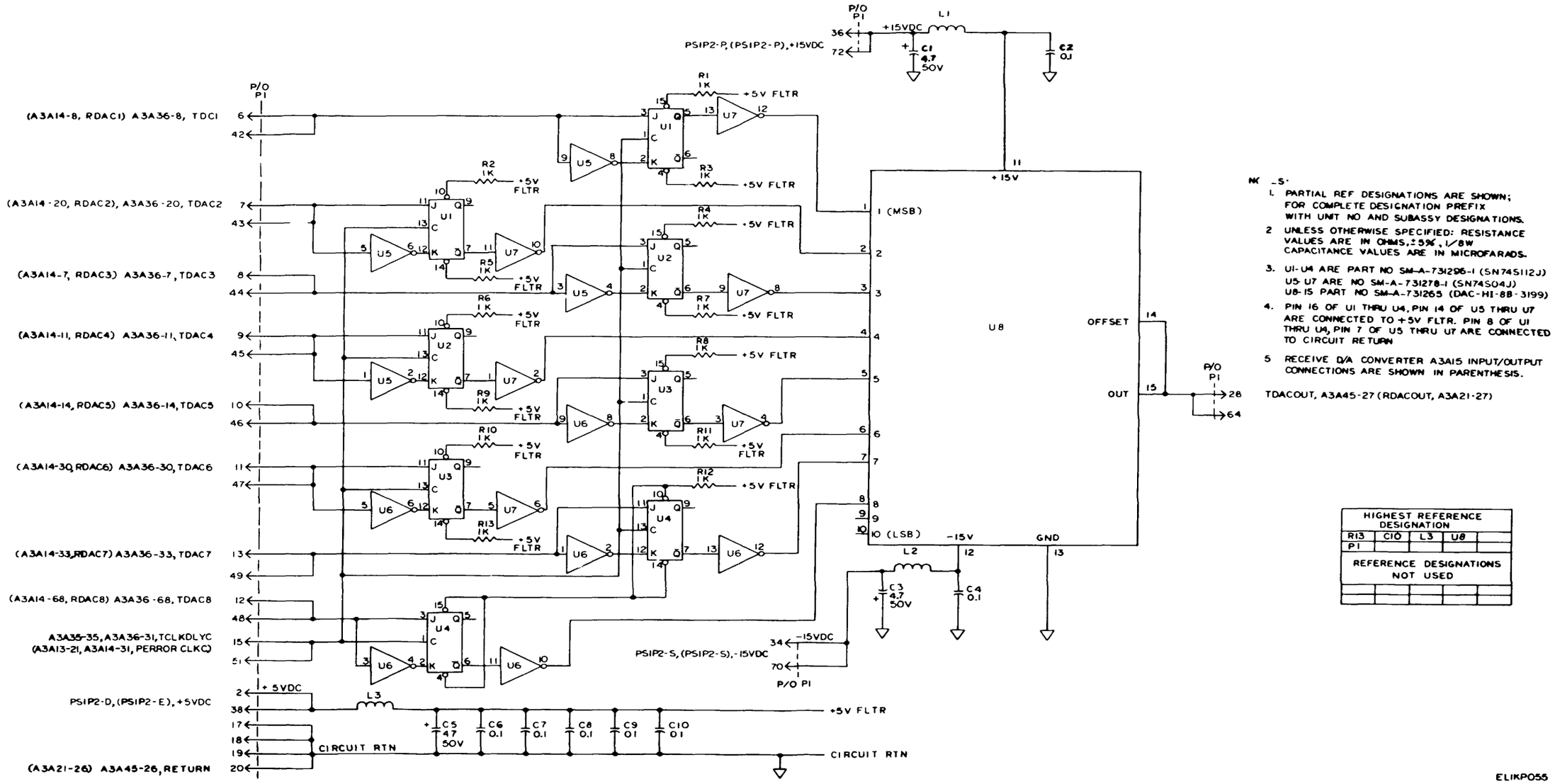


Figure FO-5. Loop filter, A3A14 and A3A36 (SM-D-731221), schematic diagram.



NOTES:

1. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO AND SUBASSY DESIGNATIONS.
2. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, ±5%, 1/8W CAPACITANCE VALUES ARE IN MICROFARADS.
3. U1-U4 ARE PART NO SM-A-731296-1 (SN74S112J) U5-U7 ARE NO SM-A-731278-1 (SN74S04J) U8 IS PART NO SM-A-731265 (DAC-HI-8B-3199)
4. PIN 16 OF U1 THRU U4, PIN 14 OF U5 THRU U7 ARE CONNECTED TO +5V FLTR. PIN 8 OF U1 THRU U4, PIN 7 OF U5 THRU U7 ARE CONNECTED TO CIRCUIT RETURN
5. RECEIVE D/A CONVERTER A3A15 INPUT/OUTPUT CONNECTIONS ARE SHOWN IN PARENTHESIS.

Figure FO-6. Digital-to-analog converter, A3A15 and A3A37 (SM-D-73217), schematic diagram.

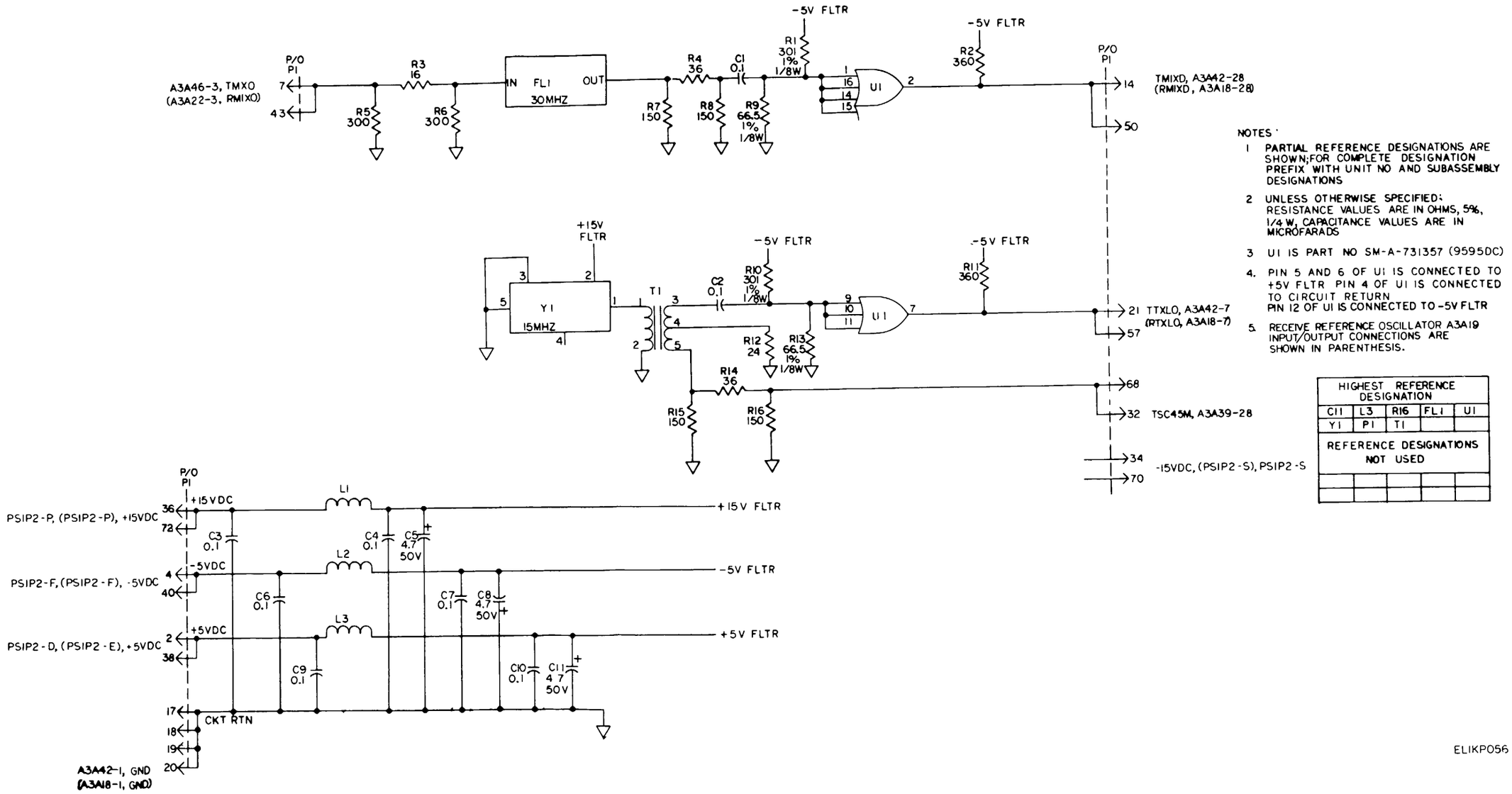


Figure FO-7. Reference oscillator, A3A19 and A3A43 (SM -D-742129), schematic diagram.

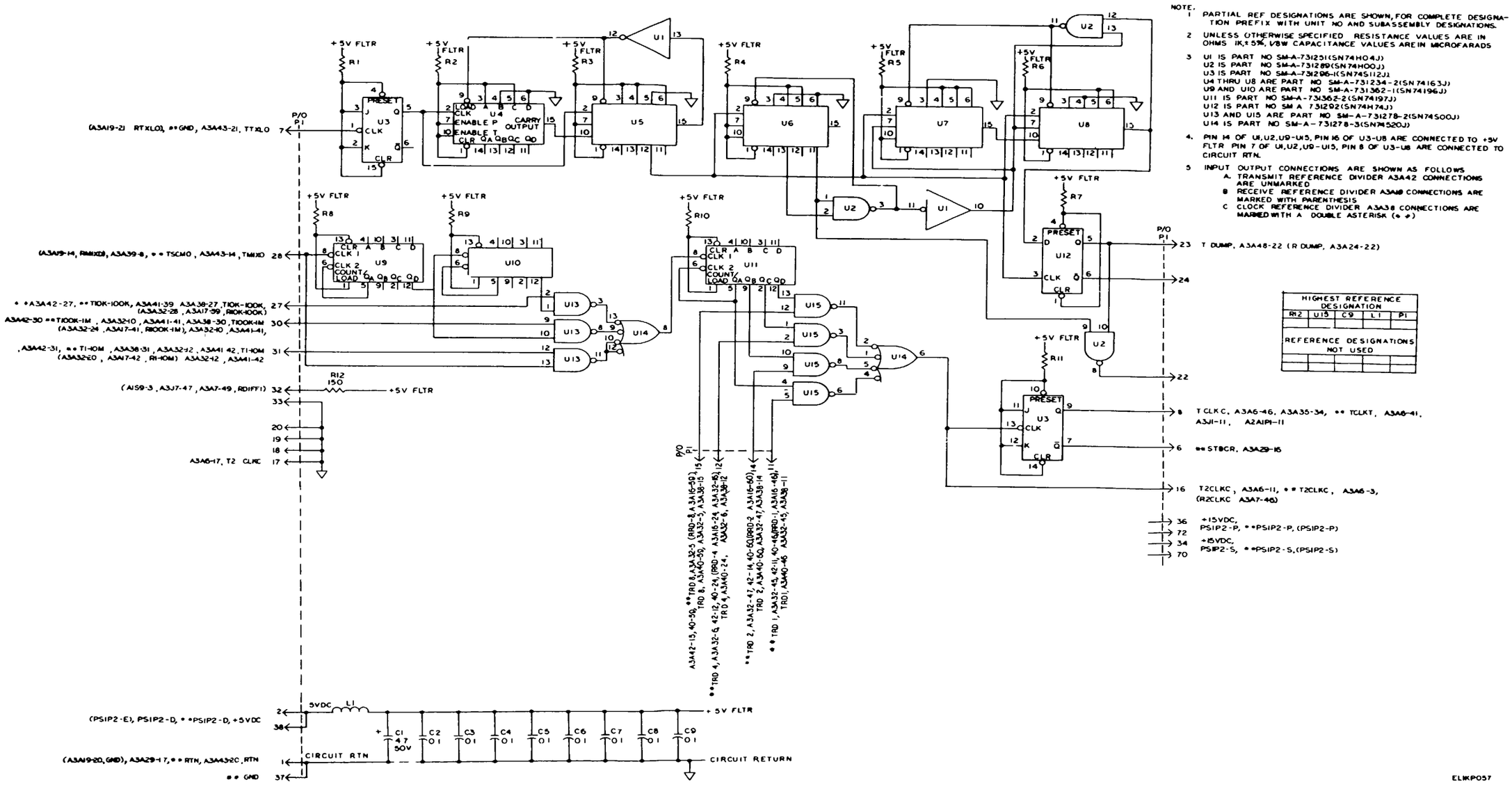
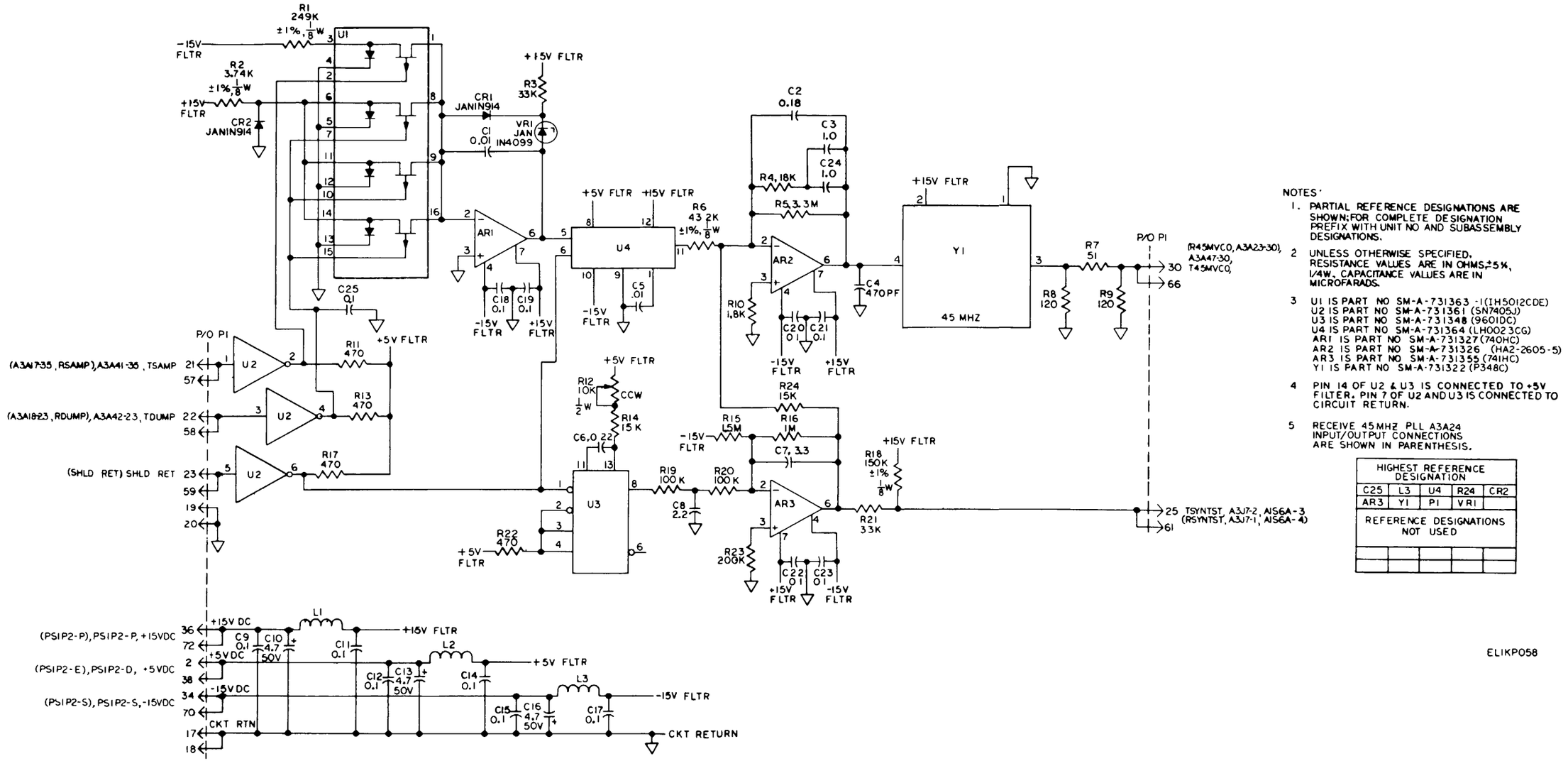


Figure FO-8. Reference divider, A3A18, A3A38, and A3A42 (SM-D-742133), schematic diagram.



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO AND SUBASSEMBLY DESIGNATIONS.
2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4W, CAPACITANCE VALUES ARE IN MICROFARADS.
3. U1 IS PART NO SM-A-731363 -1 (IH5012CDE)
   U2 IS PART NO SM-A-731361 (SN7405J)
   U3 IS PART NO SM-A-731348 (9601DC)
   U4 IS PART NO SM-A-731364 (LH0023CG)
   AR1 IS PART NO SM-A-731327 (740HC)
   AR2 IS PART NO SM-A-731326 (HA2-2605-5)
   AR3 IS PART NO SM-A-731355 (741HC)
   Y1 IS PART NO SM-A-731322 (P348C)
4. PIN 14 OF U2 & U3 IS CONNECTED TO +5V FILTER. PIN 7 OF U2 AND U3 IS CONNECTED TO CIRCUIT RETURN.
5. RECEIVE 45 MHZ PLL A3A24 INPUT/OUTPUT CONNECTIONS ARE SHOWN IN PARENTHESIS.

HIGHEST REFERENCE DESIGNATION				
C25	L3	U4	R24	CR2
AR3	Y1	P1	VR1	
REFERENCE DESIGNATIONS NOT USED				

Figure FO-9. 45 MHz phase lock loop, A3A24 and A3A48 (SM-D-742113), schematic diagram.

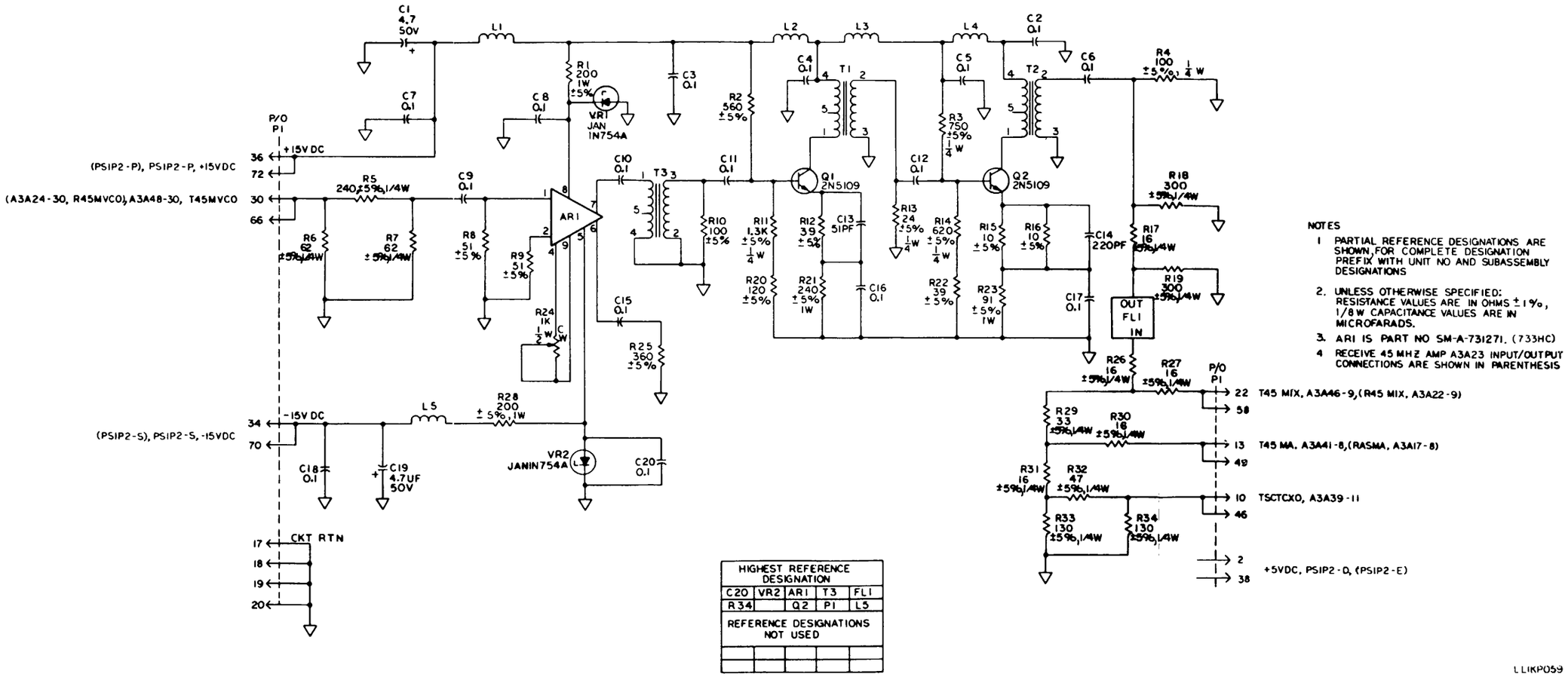


Figure FO-10. 45MHz amplifier, A3A23 and A3A47 (SM-D-742117), schematic diagram.

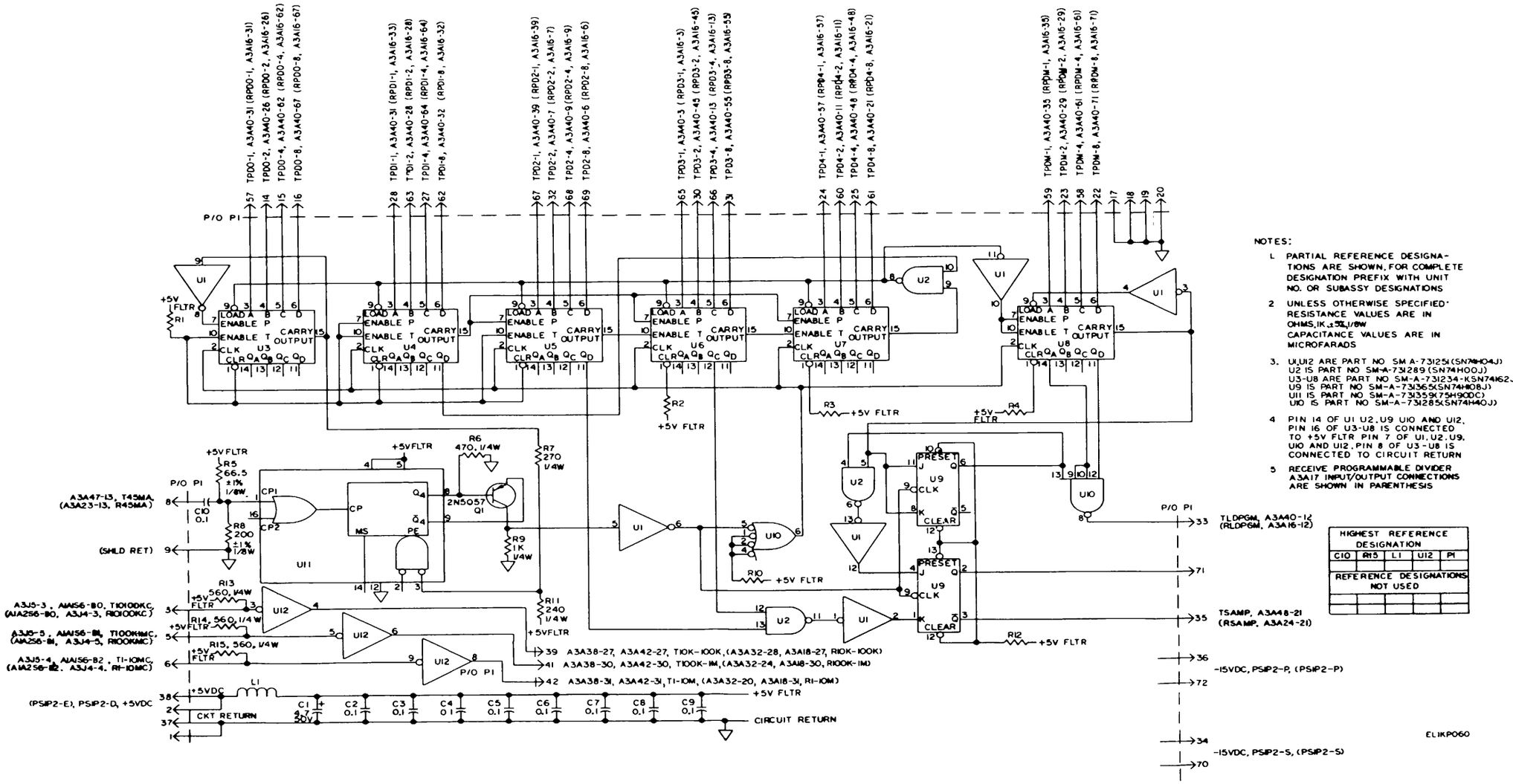


Figure FO-11. Programmable divider, A3A17 and A3A41 (SM-D-742109), schematic diagram.

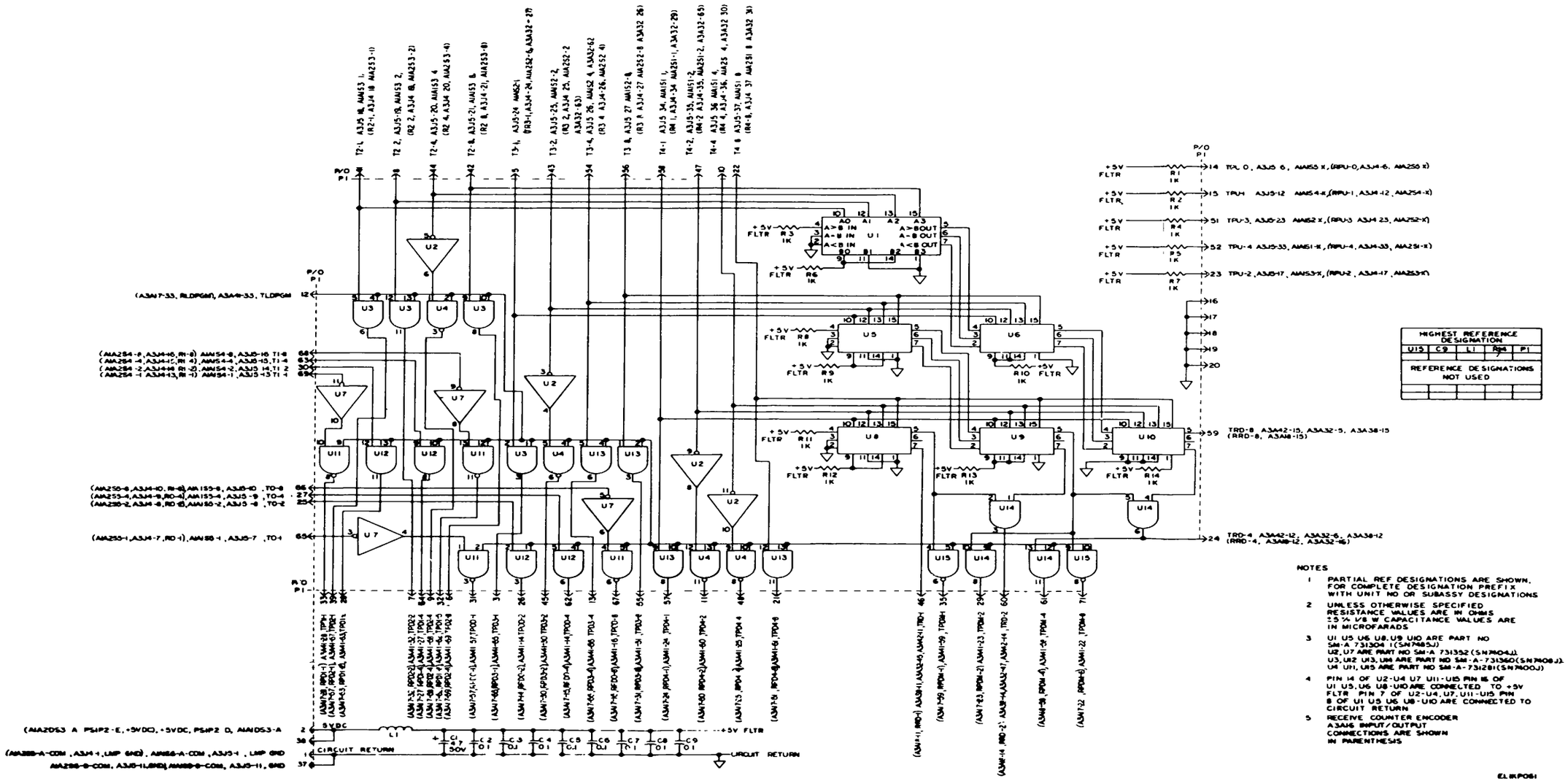


Figure FO-12. Counter encoder, A3A16 and A3A40 (SM-D-742105), schematic diagram.

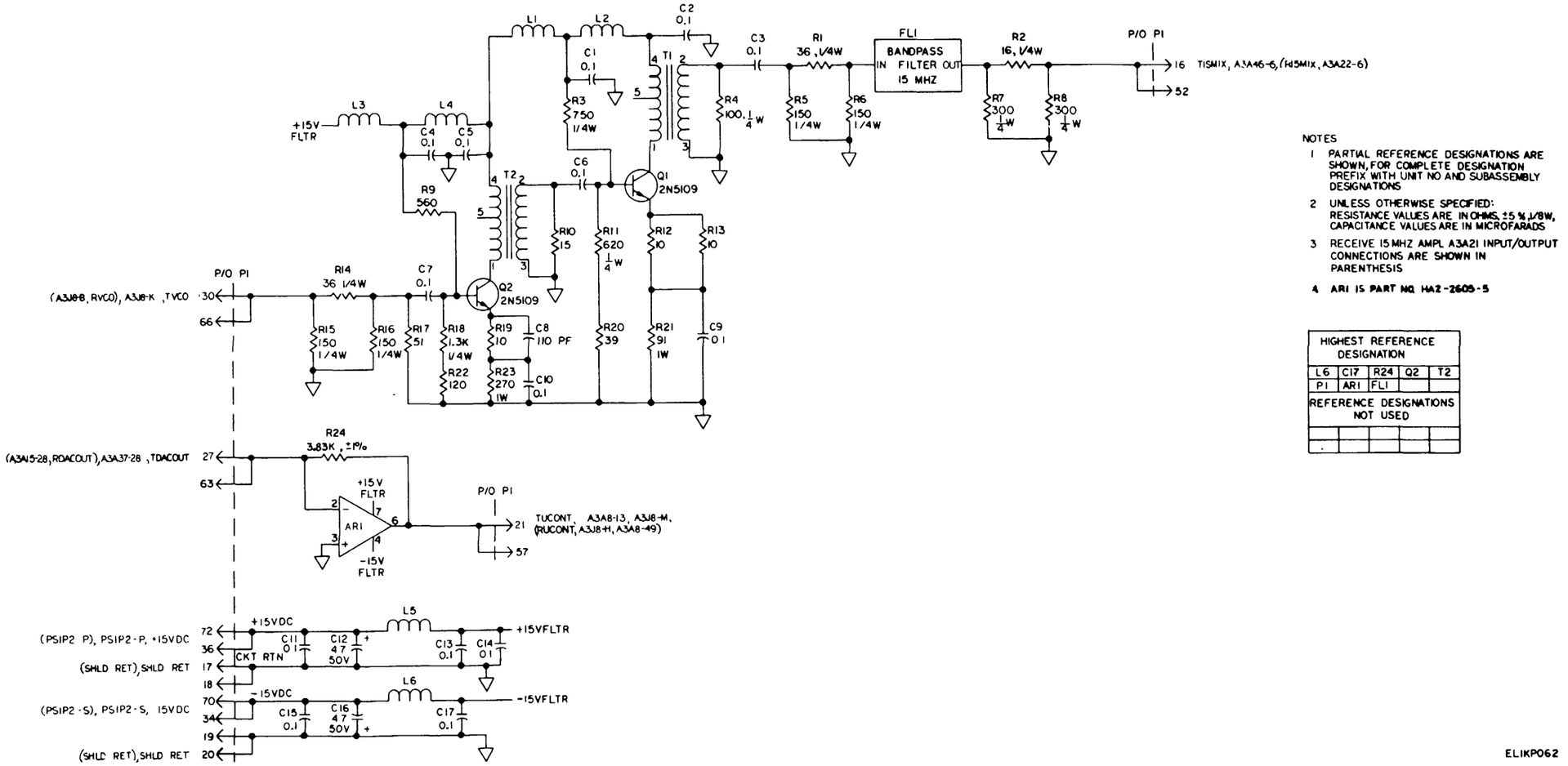


Figure FO-13. 15 MHz amplifier, A3A21 and A3A45 (SM-D-742121), schematic diagram.

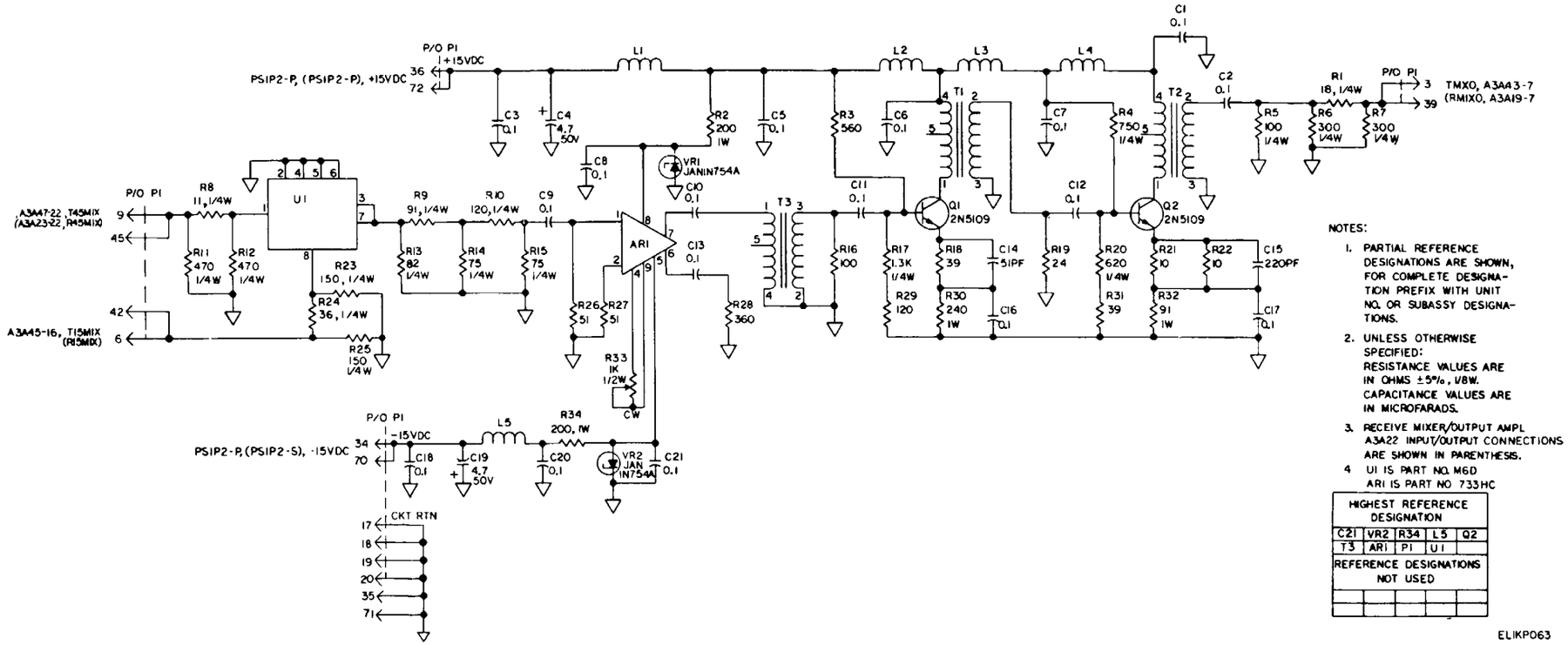


Figure FO-14. Mixer/output amplifier, A3A22 and A3A46 (SM-D-742125),schematic diagram.

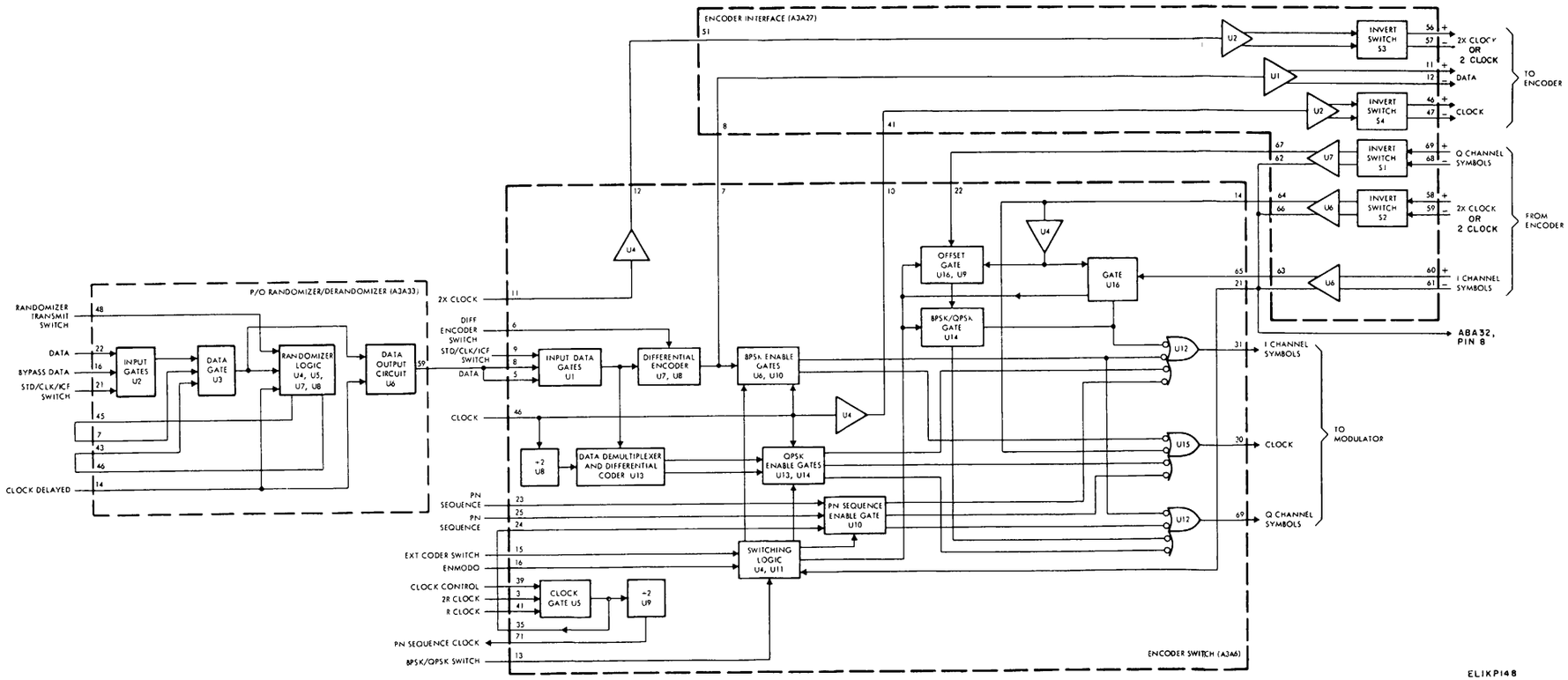


Figure FO-15. Encoder/decoder and interface, functional block diagram.

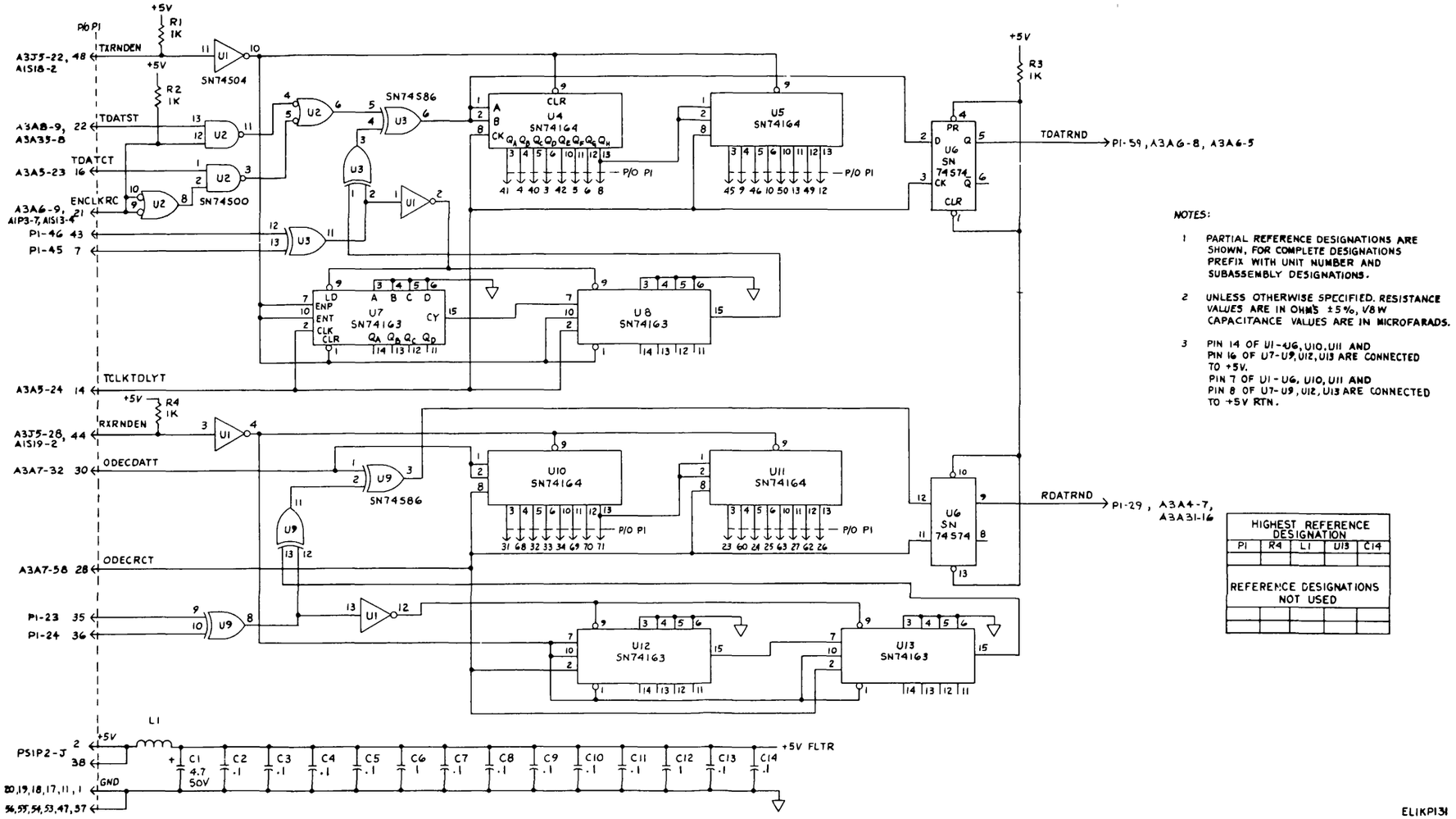


*Figure FO-16. Randomizer/*derandomizer, *A3A33(SM-D-877780),schematic diagram.*

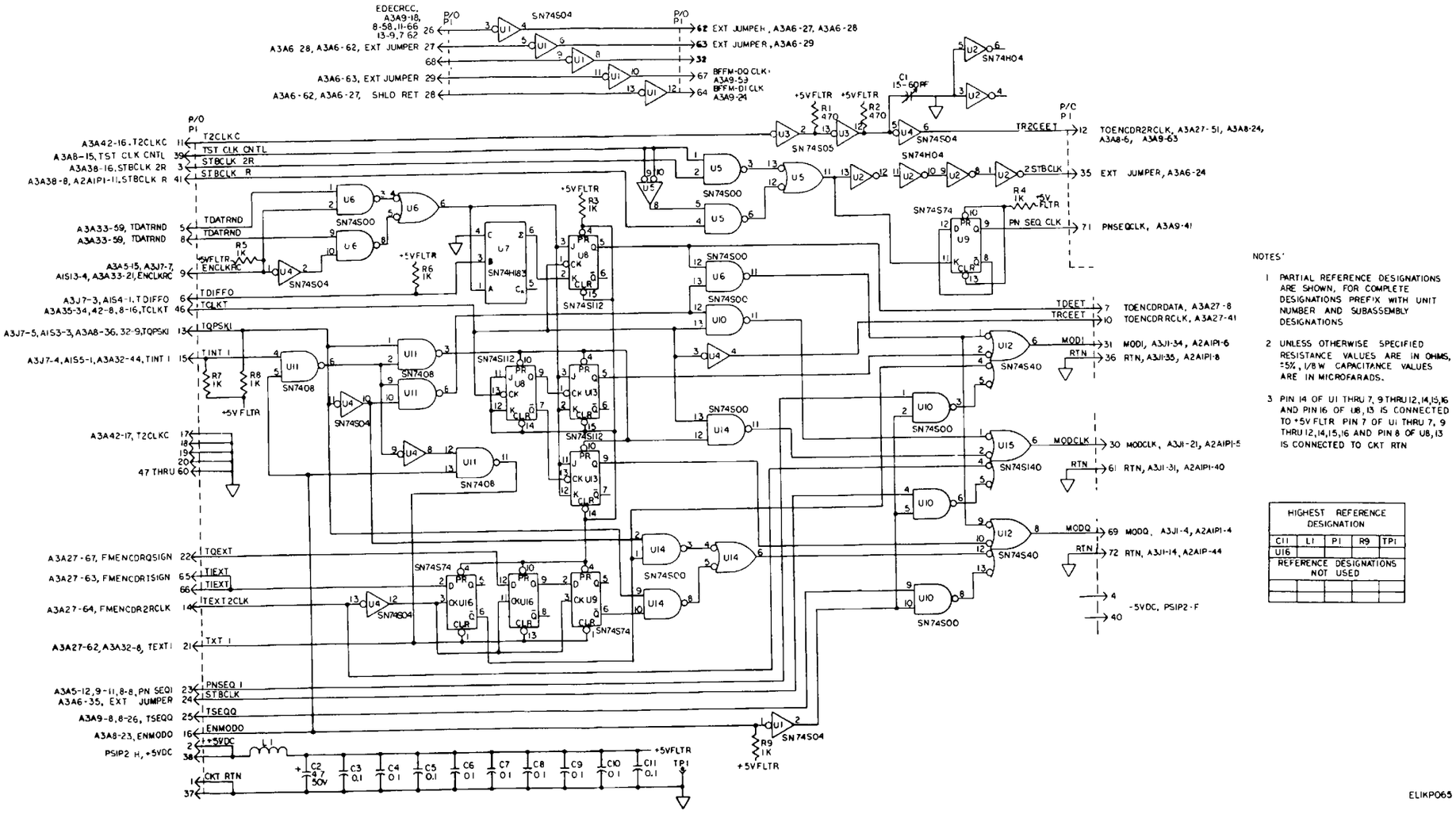


Figure FO-17. Encoder switch, A3A6(SM-S-877730),schematic diagram.

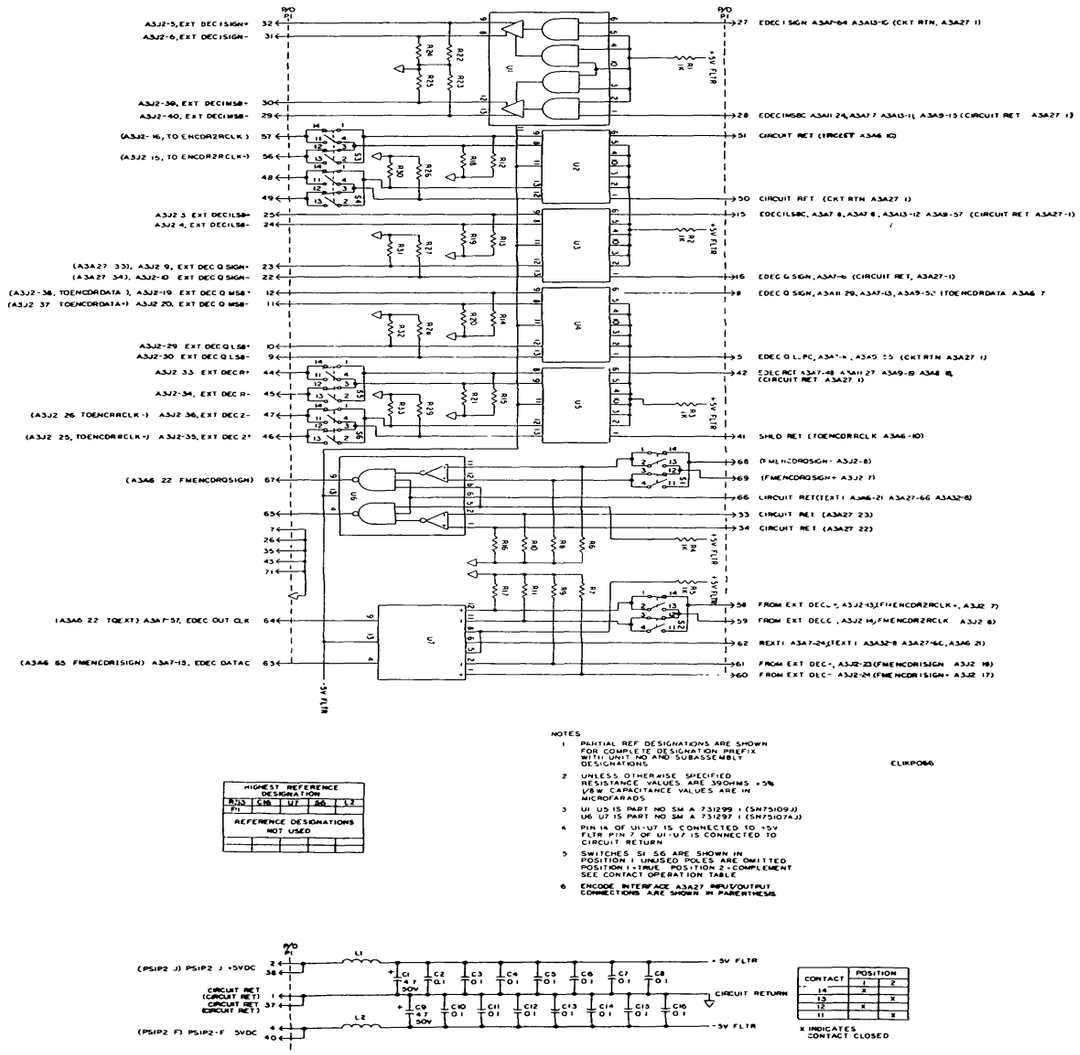


Figure FO-18. Encoder interface, A3A27 and A3A28 (SM-D-742049), schematic diagram.

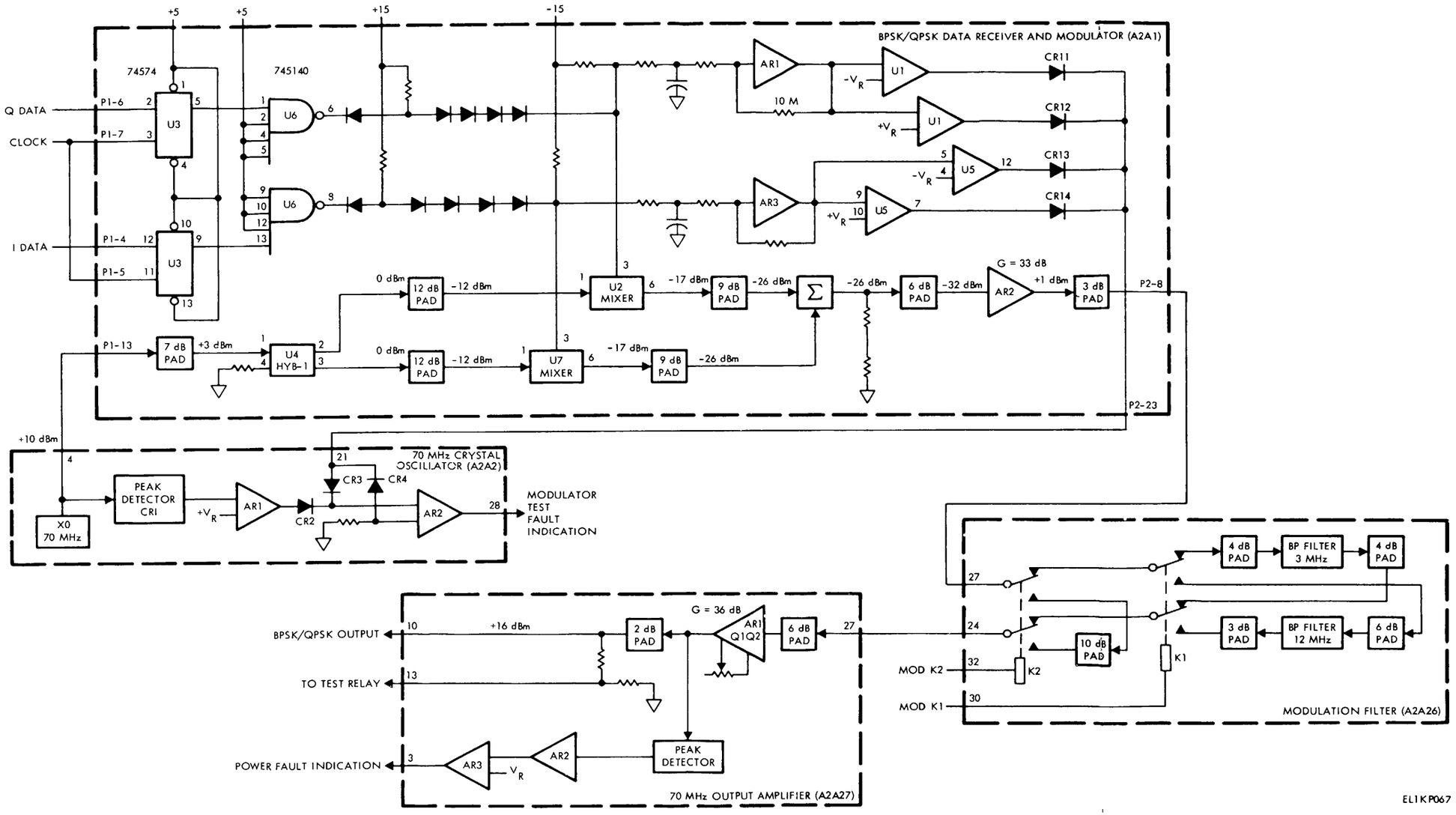


Figure FO-19. RF modulator, functional block diagram.

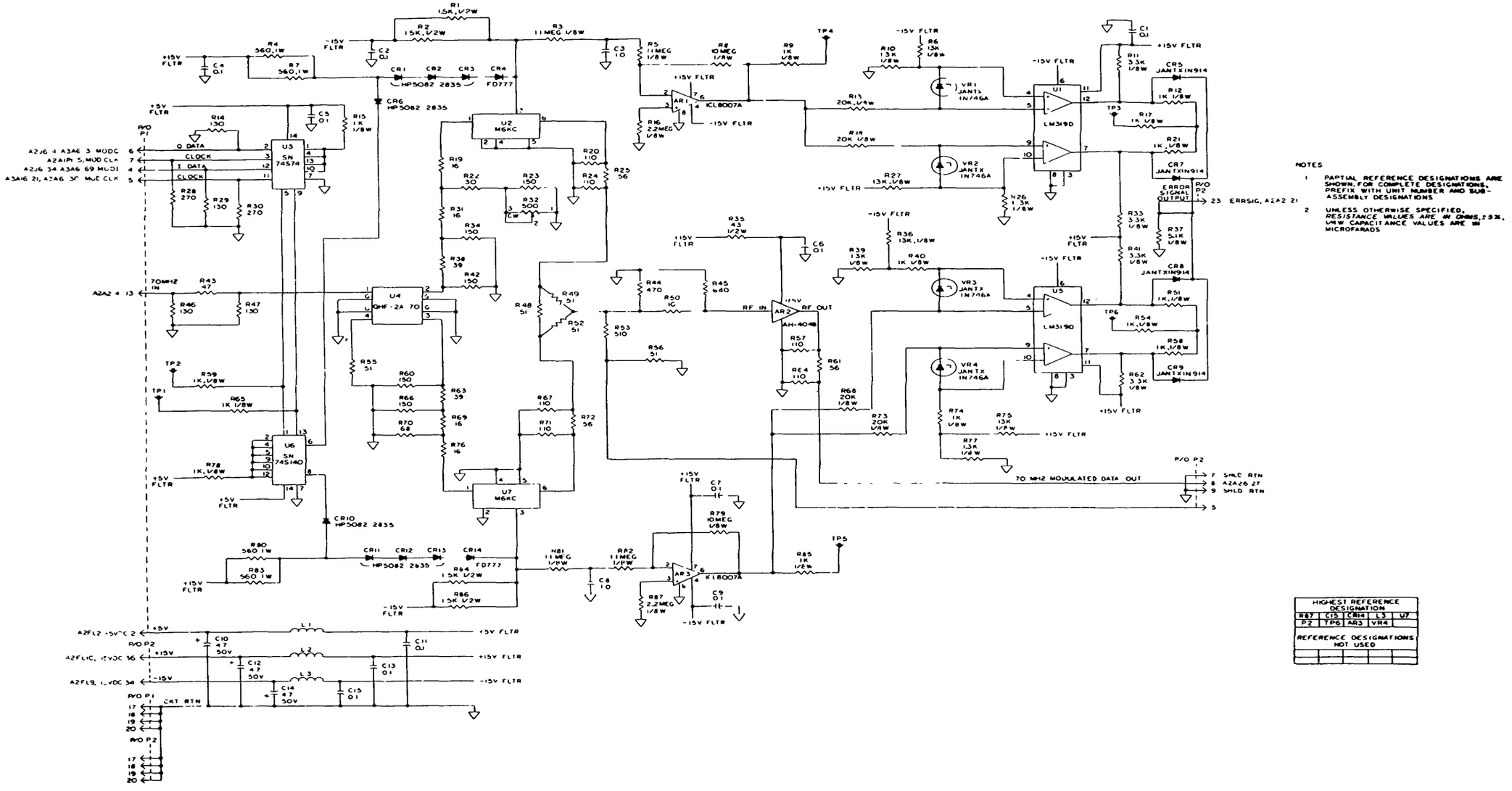
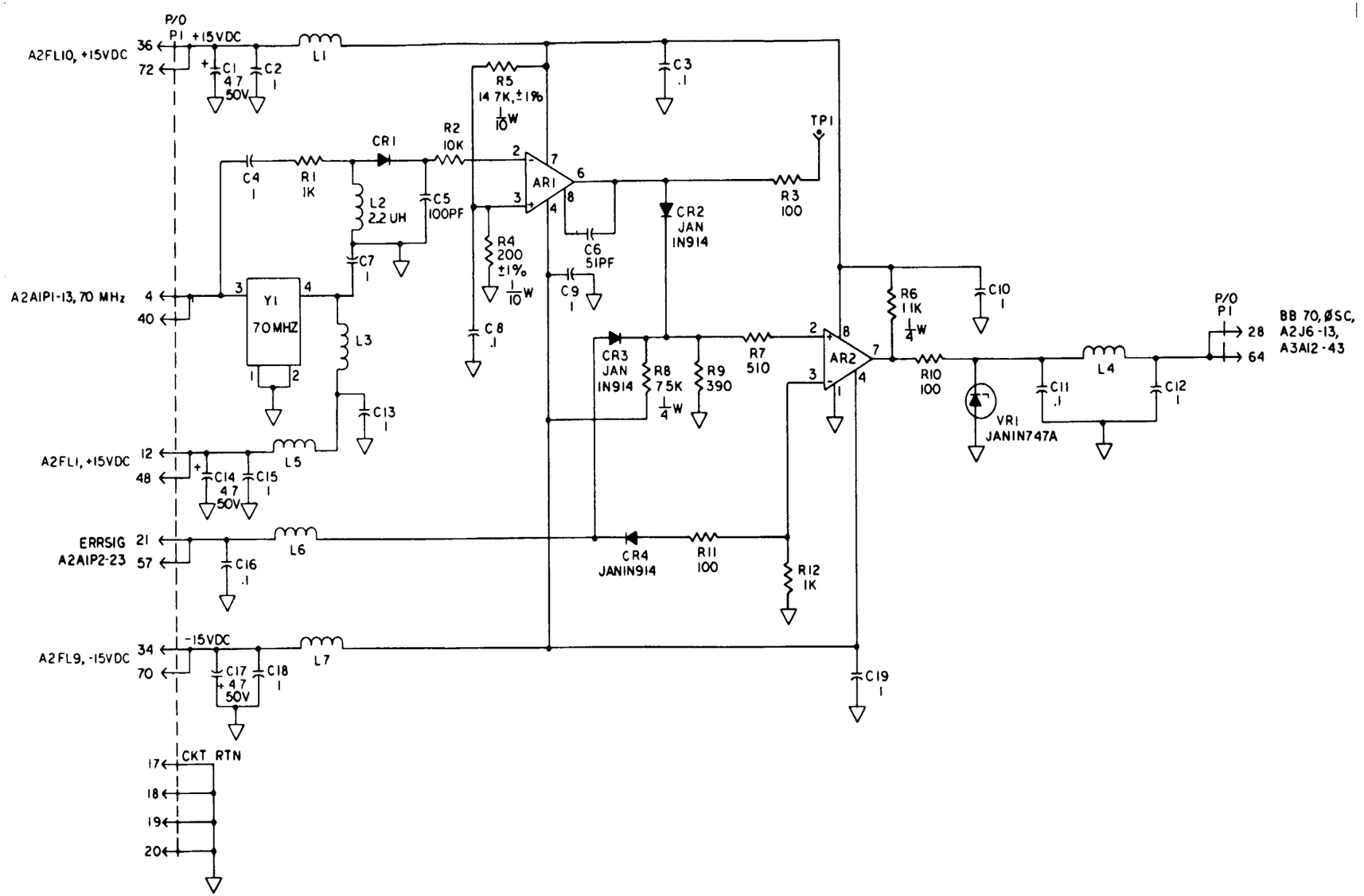


Figure FO-20. QPSK/BPSK data receiver and modulator, A2A1 (SM-D-877650), schematic diagram.



NOTES:

1. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO AND SUBASSY DESIGNATIONS.
2. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, ±5%, 1/8W. CAPACITANCE VALUES ARE IN MICROFARADS.
3. AR1 PART NO. IS 741HC
   AR2 PART NO. IS HA2-2311-5

HIGHEST REFERENCE DESIGNATION				
AR2	C19	CR4	L7	P1
R12	VR1	Y1	TP1	
REFERENCE DESIGNATIONS NOT USED				

ELIKP069

Figure FO-21. 70MHz crystal oscillator, A2A (SM-D-731193), schematic diagram.

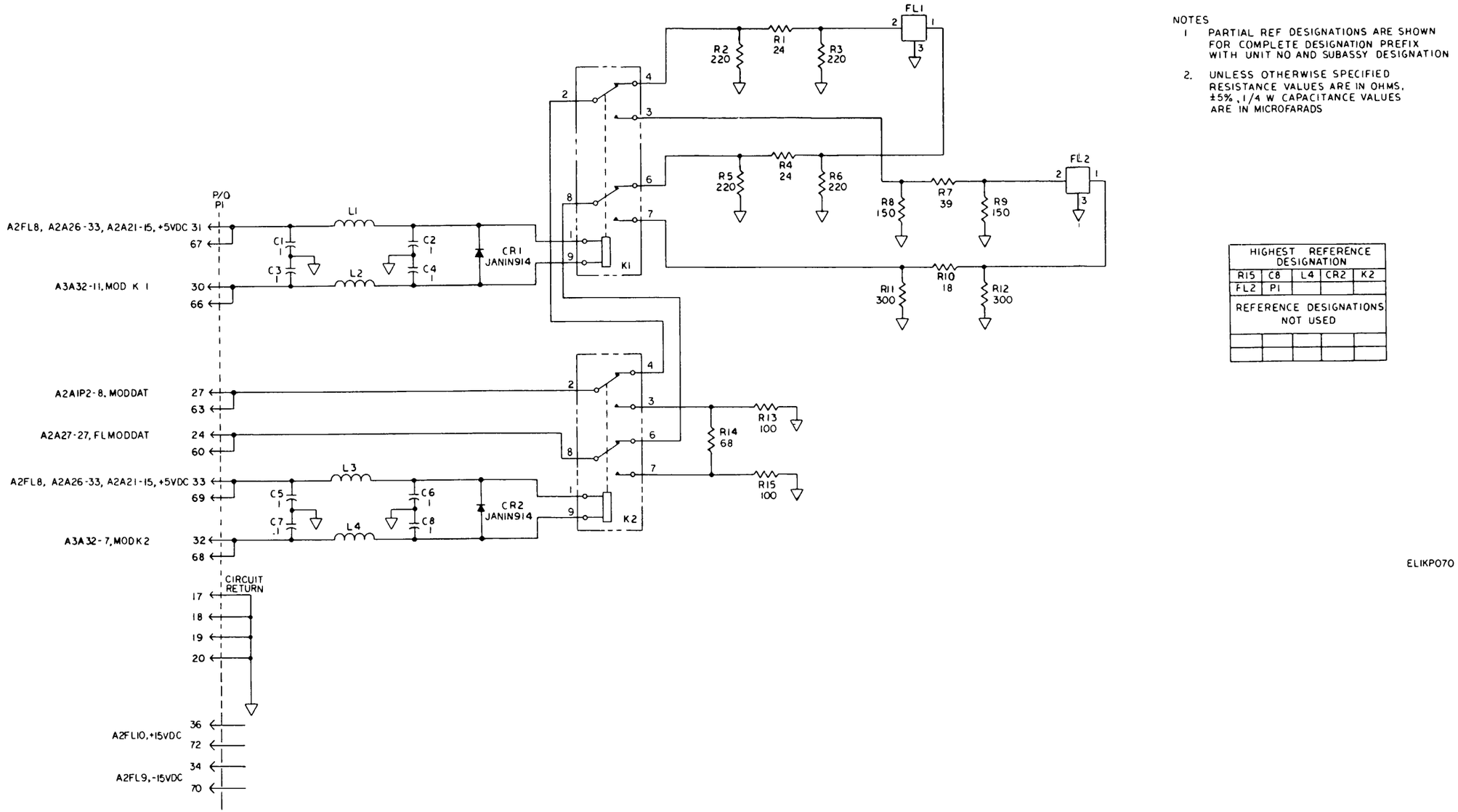


Figure FO-22. Modulation filter, A2A26 (SM-D-D-731185), schematic diagram.

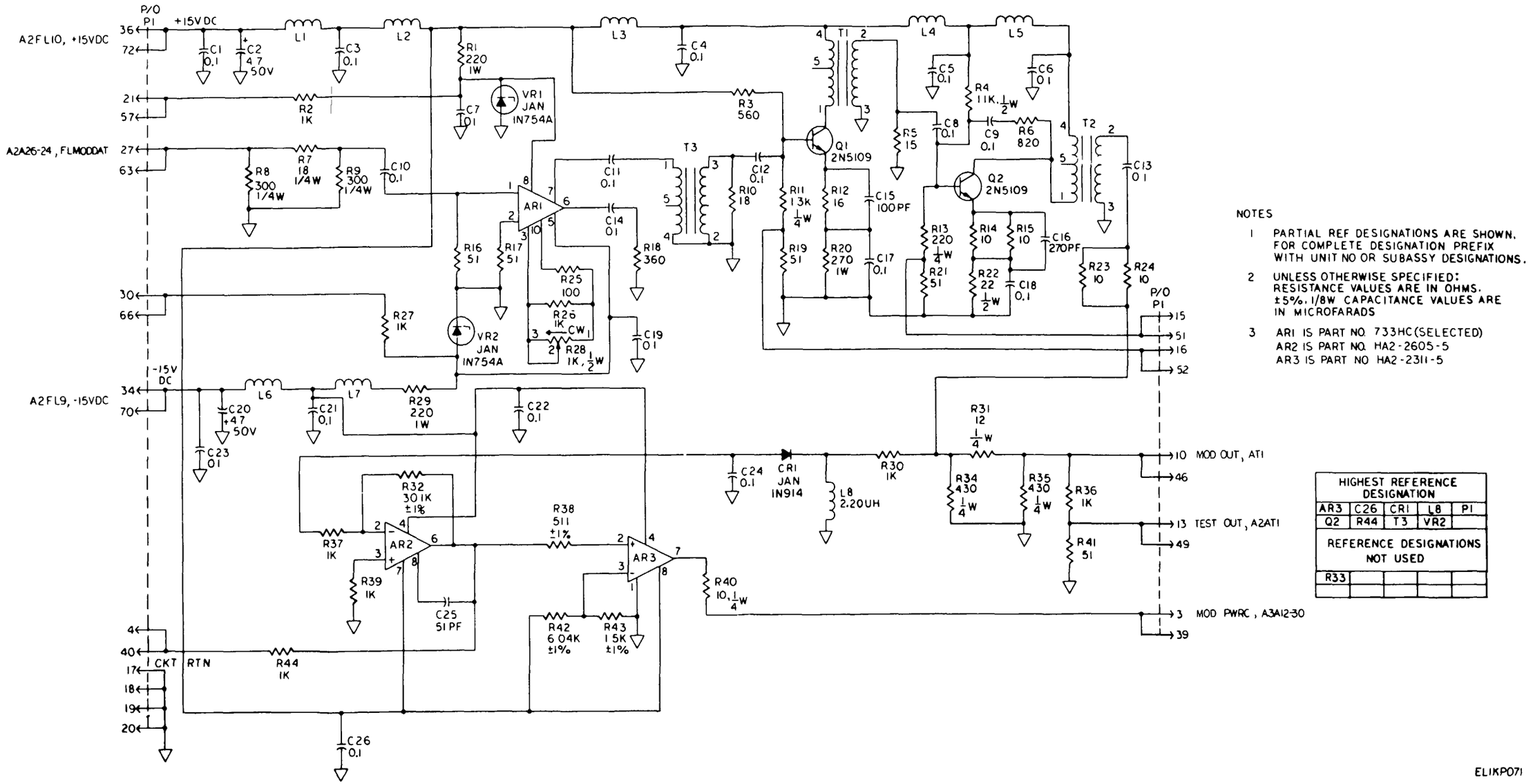


Figure FO-23. 70 MHz output amplifier, A2A27 (SM-D-731189), schematic diagram.)

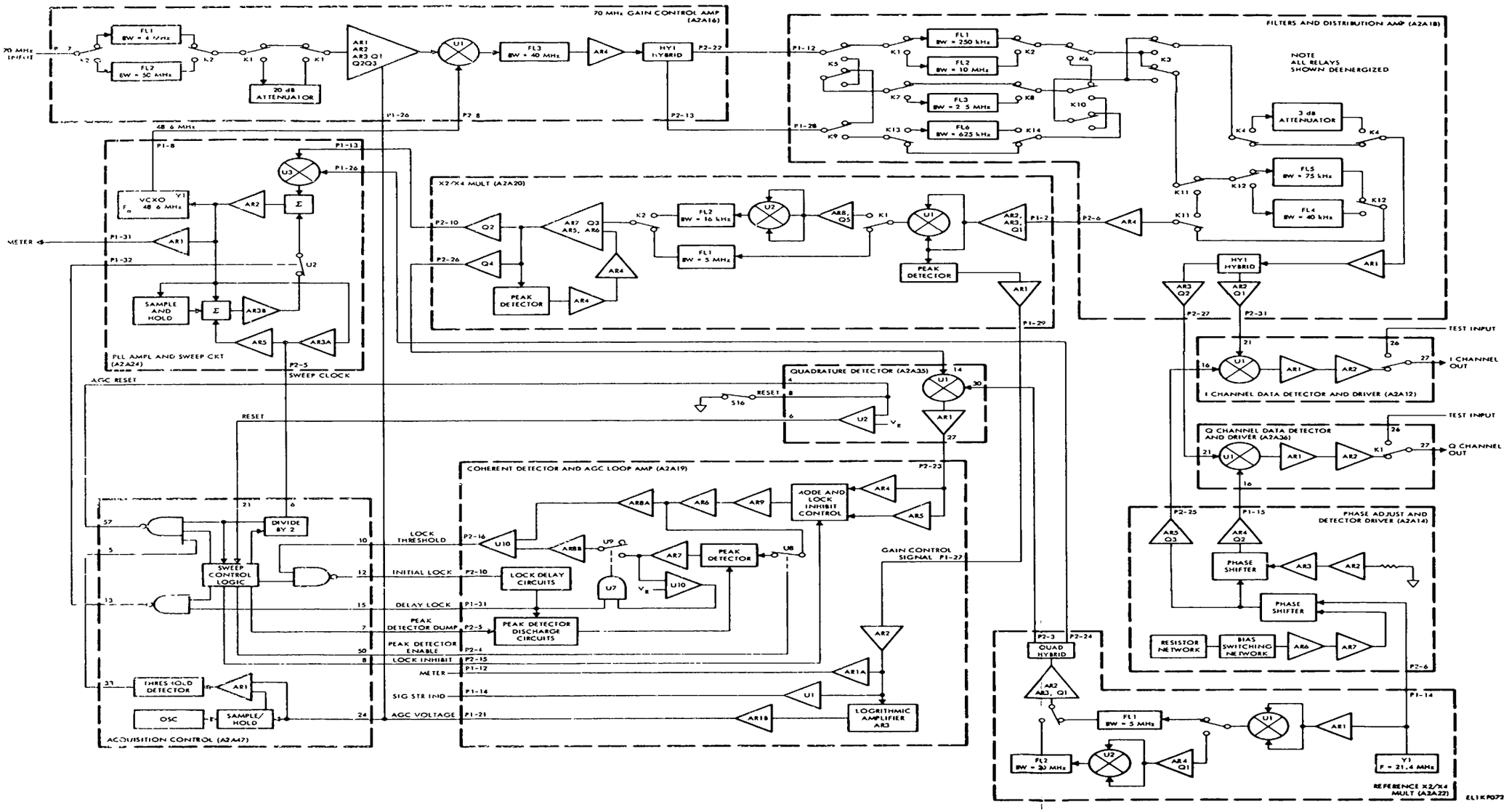


Figure FO-24. RF demodulator, functional block diagram.

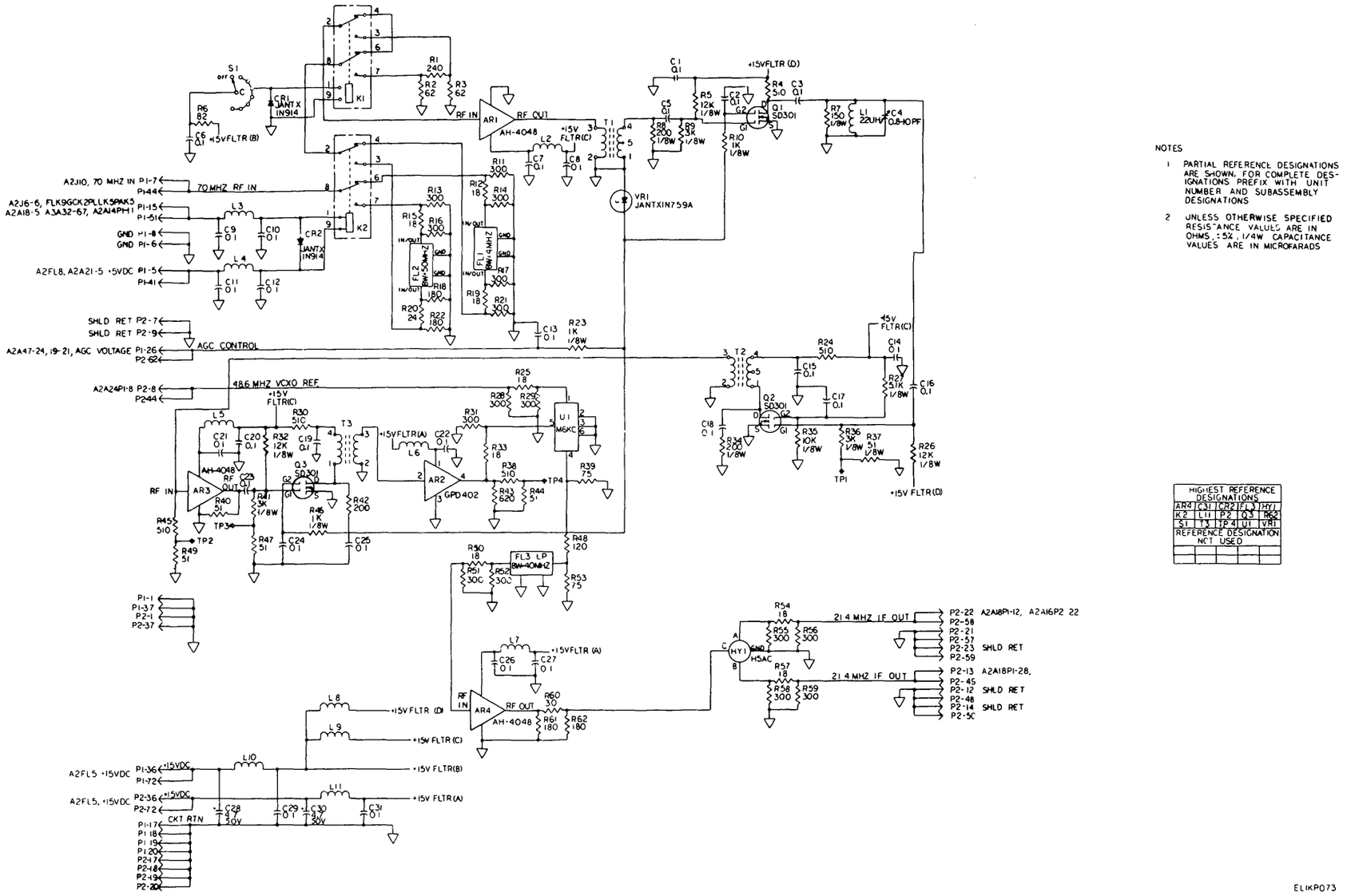


Figure FO-25. 70-MHz gain control amplifier, A2A16 (SM-D-877675), schematic diagram.

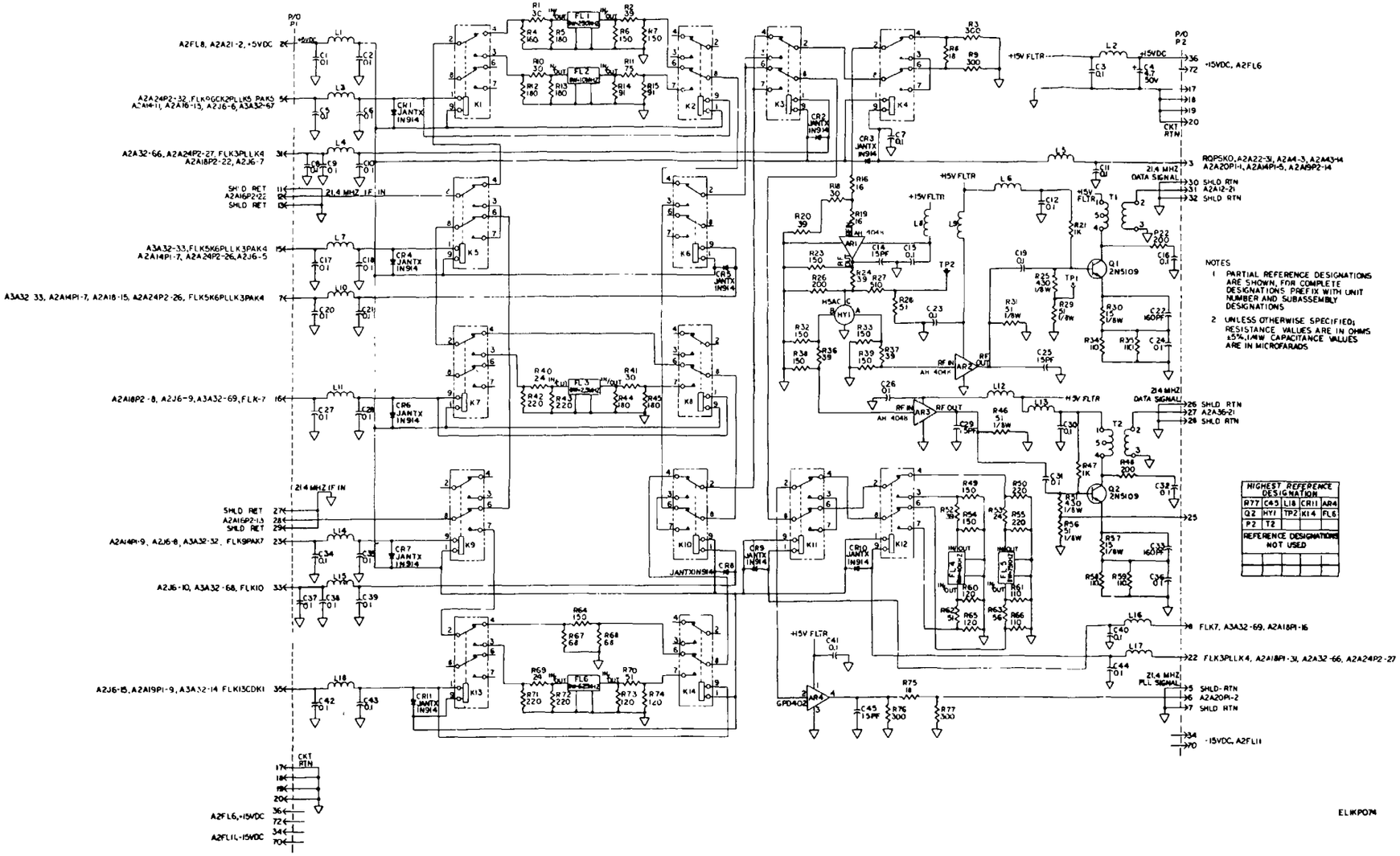


Figure FO-26. Filters and distribution amplifiers, A2A18 (SM-D-877645), schematic diagram.

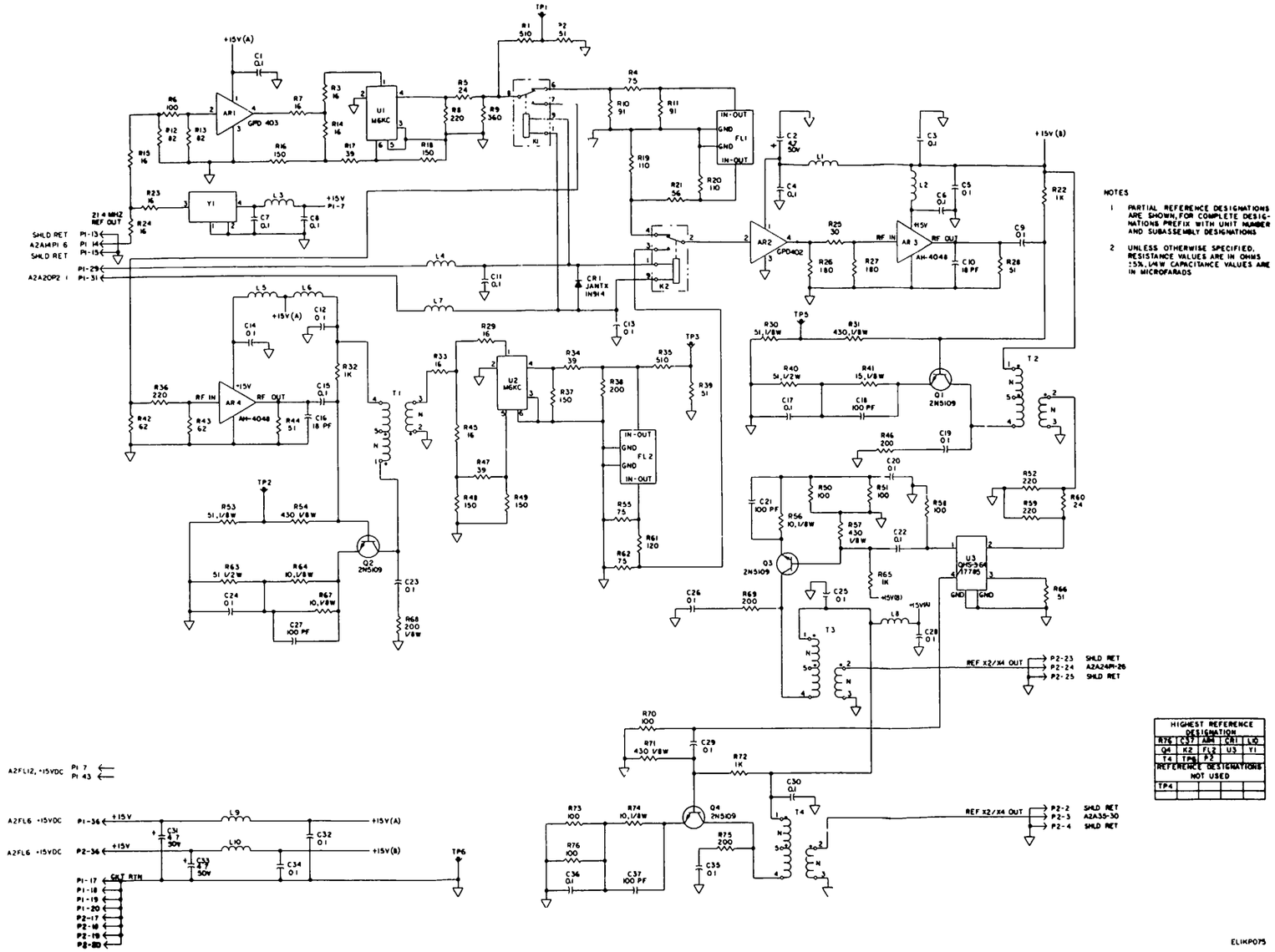


Figure FO-27. Reference X2/X4 multiplier, A2A22 (SM-D-877655), schematic diagram.

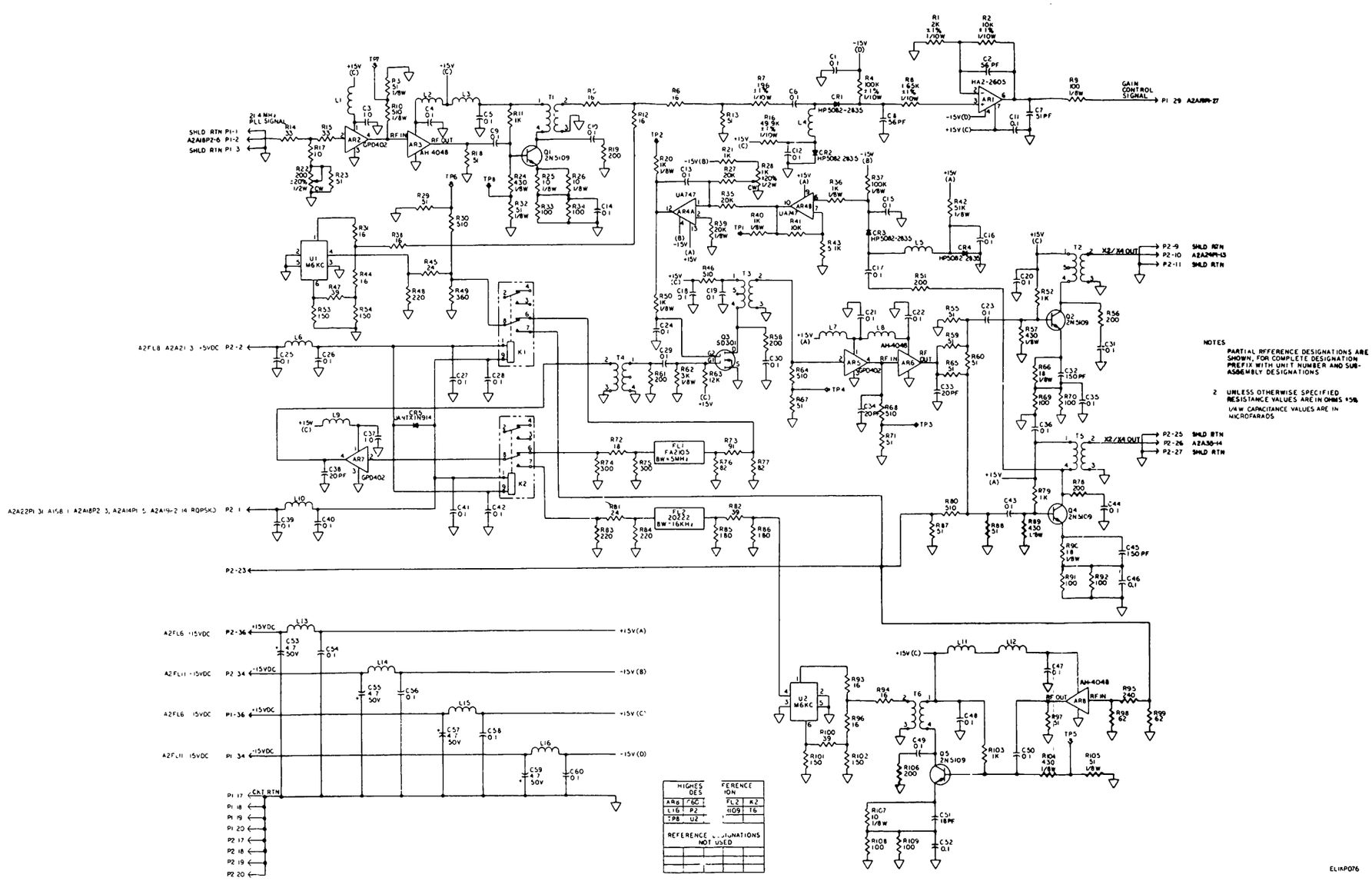


Figure FO-28. X2/X4 multiplier, A2A20 (SM-D-8776660), schematic diagram.

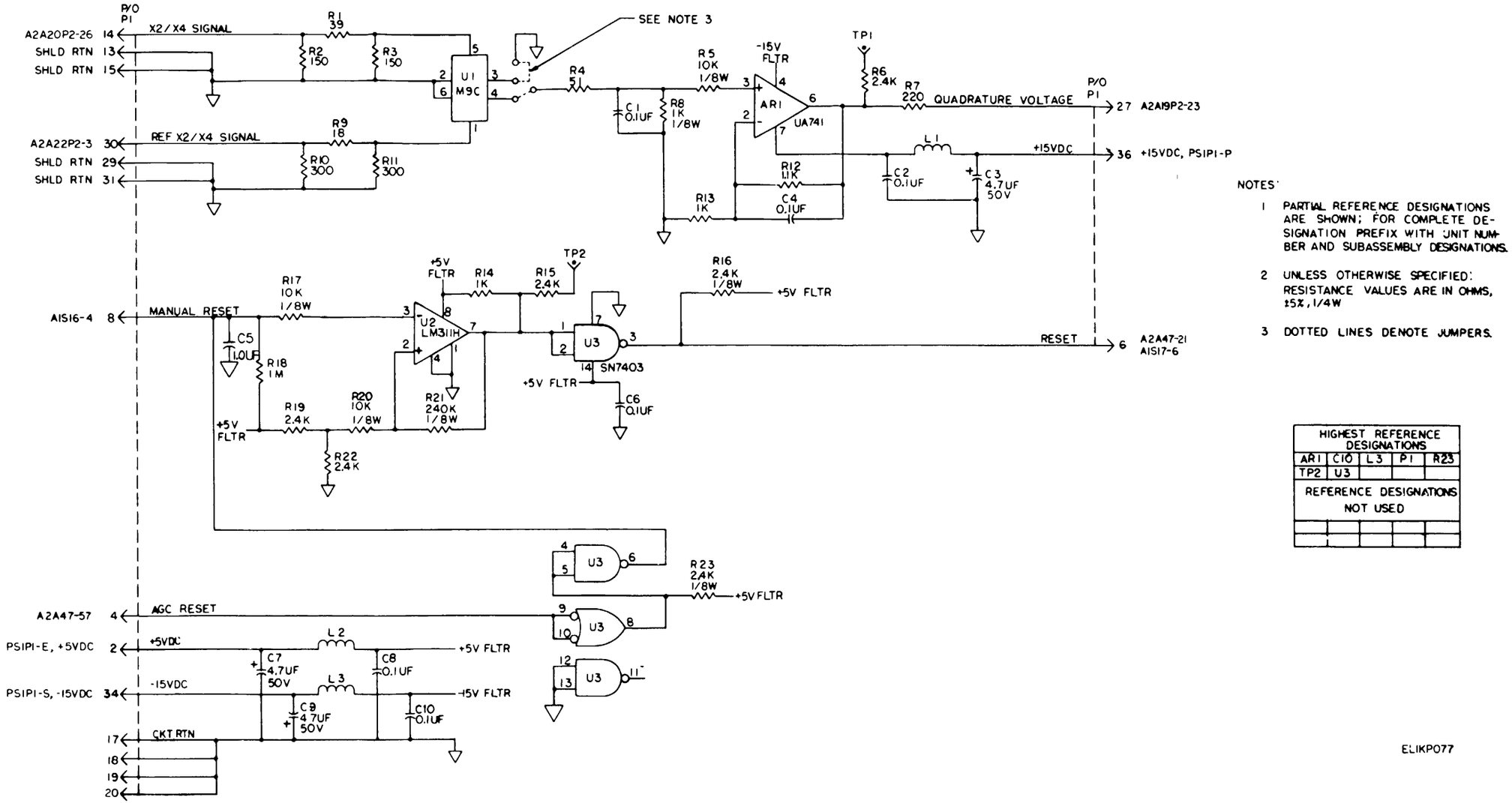


Figure FO-29. Quadrature deter, A2A35 (SM-D-877690), schematic diagram.

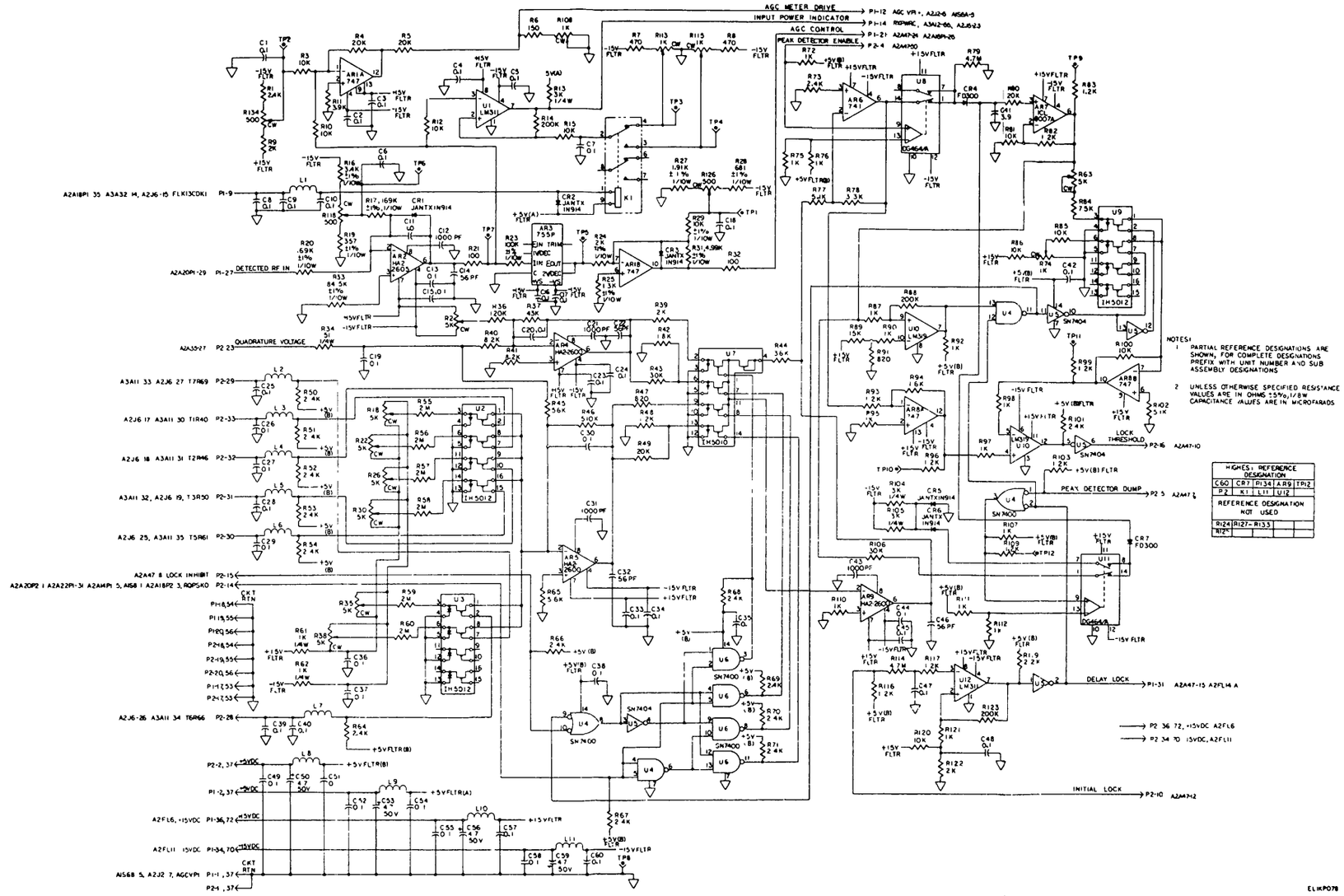


Figure FO-30. Coherent detector and AGC loop amplifier, A2A19 (SM-D-877665), schematic diagram.

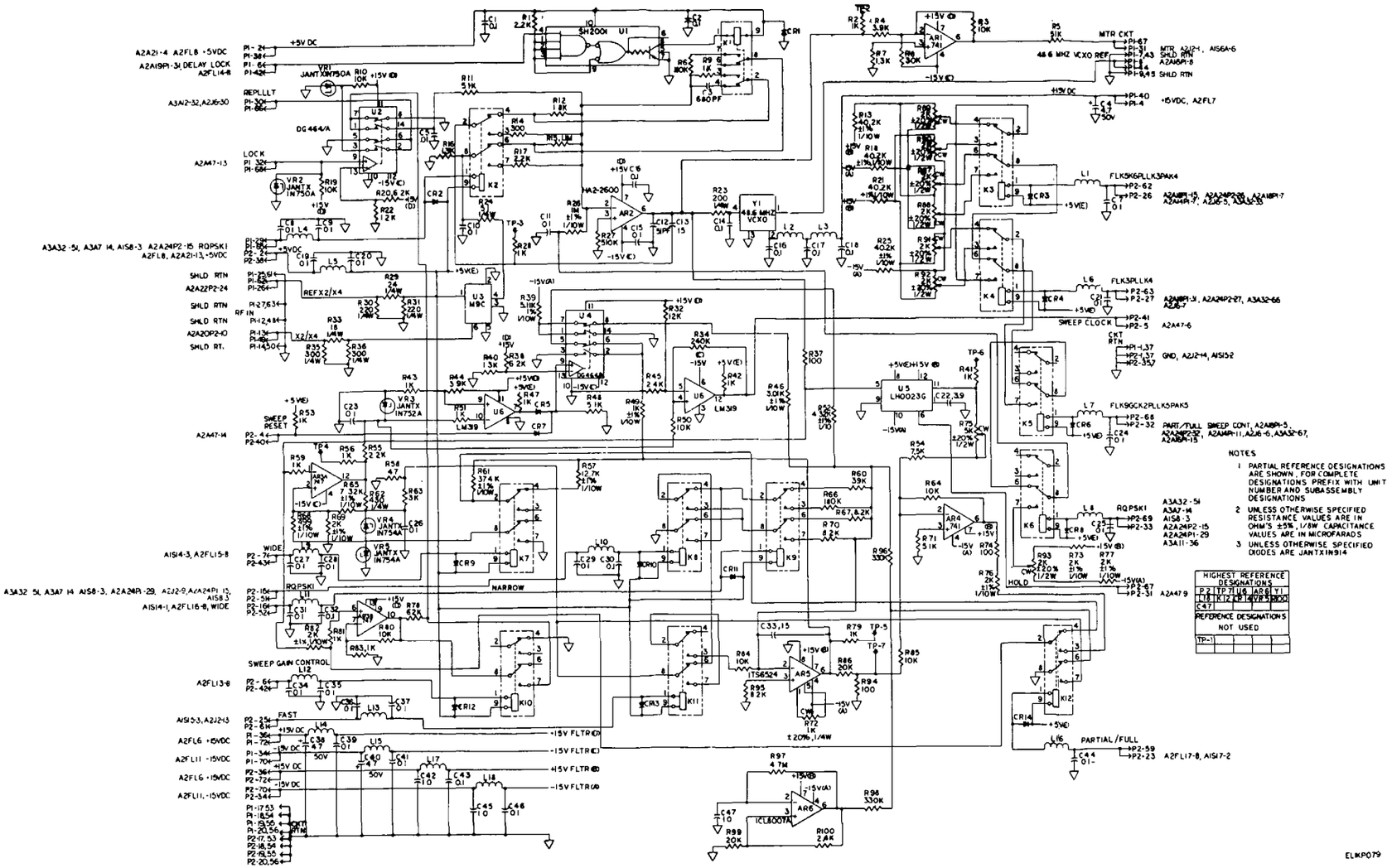


Figure FO-31. PLL amplifier and sweep generator, A2A24 (SM-D-877670), schematic diagram.

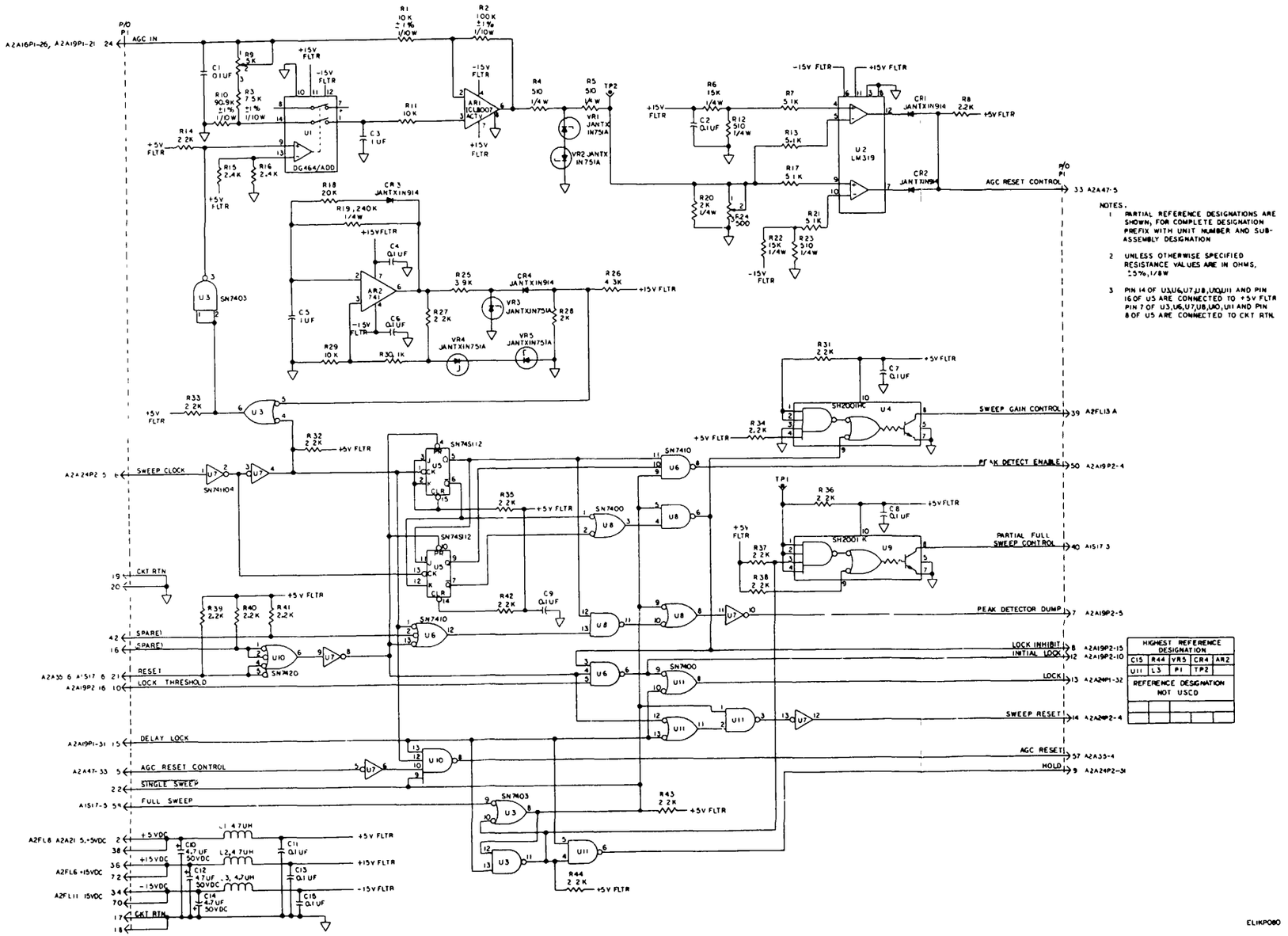


Figure FO-32. Acquisition control, A2A47 (SM-D-877685), schematic diagram.

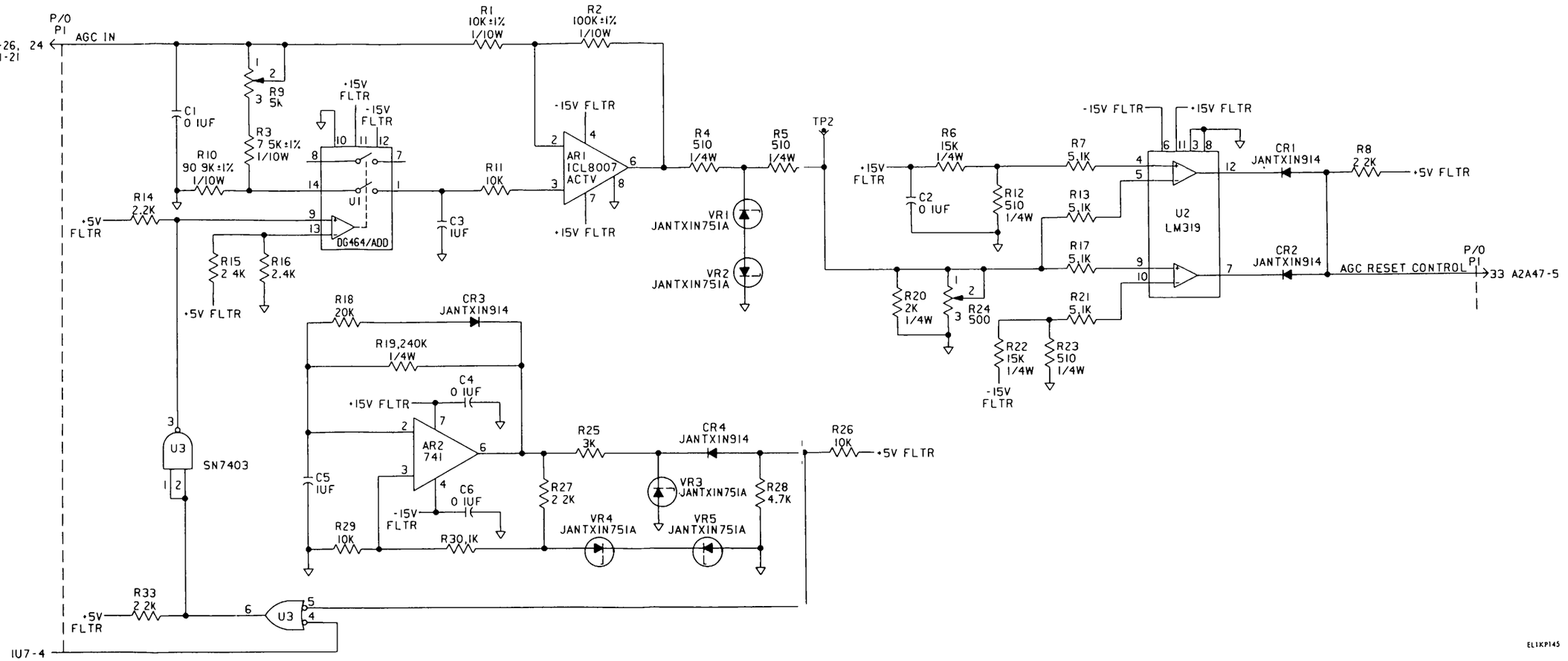
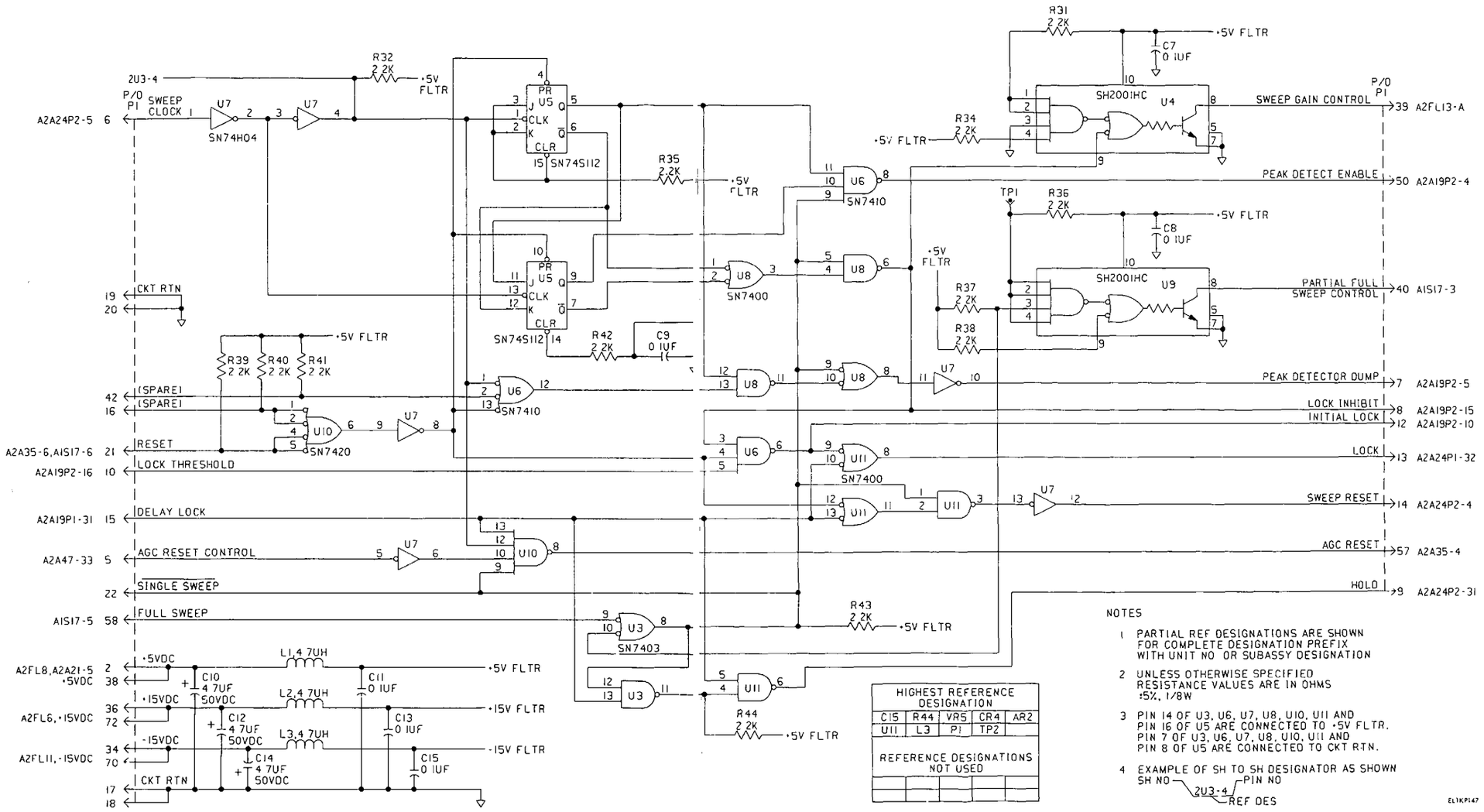


Figure FO-32.1 (1). *Acquisition control A2A47 (SM-D-877935), schematic diagram (provided on contract DAAB07-79-C-0289) (sheet 1 of 2).*



FO-32.1 (2). *Acquisition control A2A46 (SM-D-877935), schematic diagram (provided on Contract DAAB07-79-C-0289) (sheet 2 of 2)*

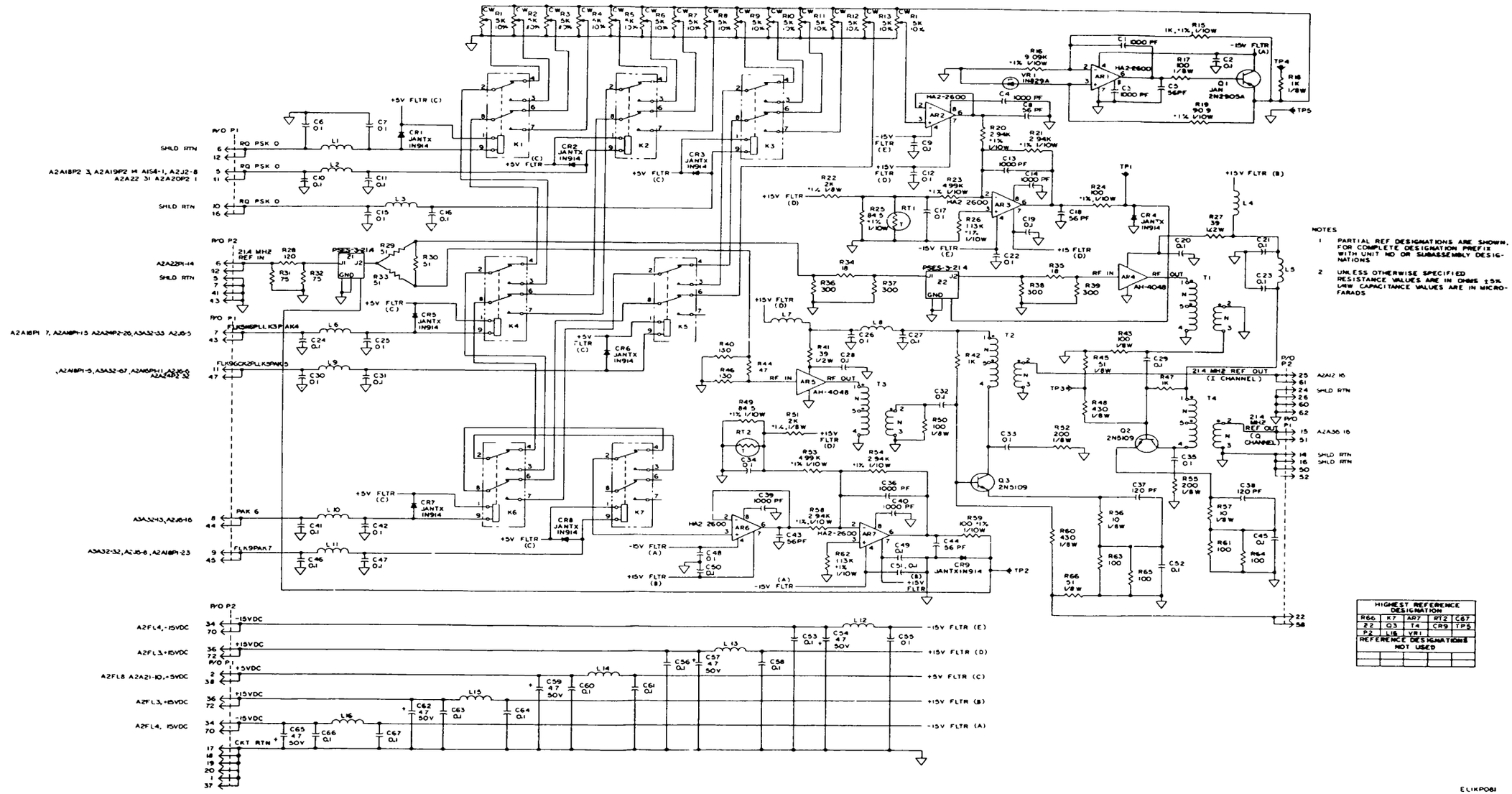


Figure FO-33. Phase adjust and detector drive, A2A14 (SM-D-877680), schematic diagram.

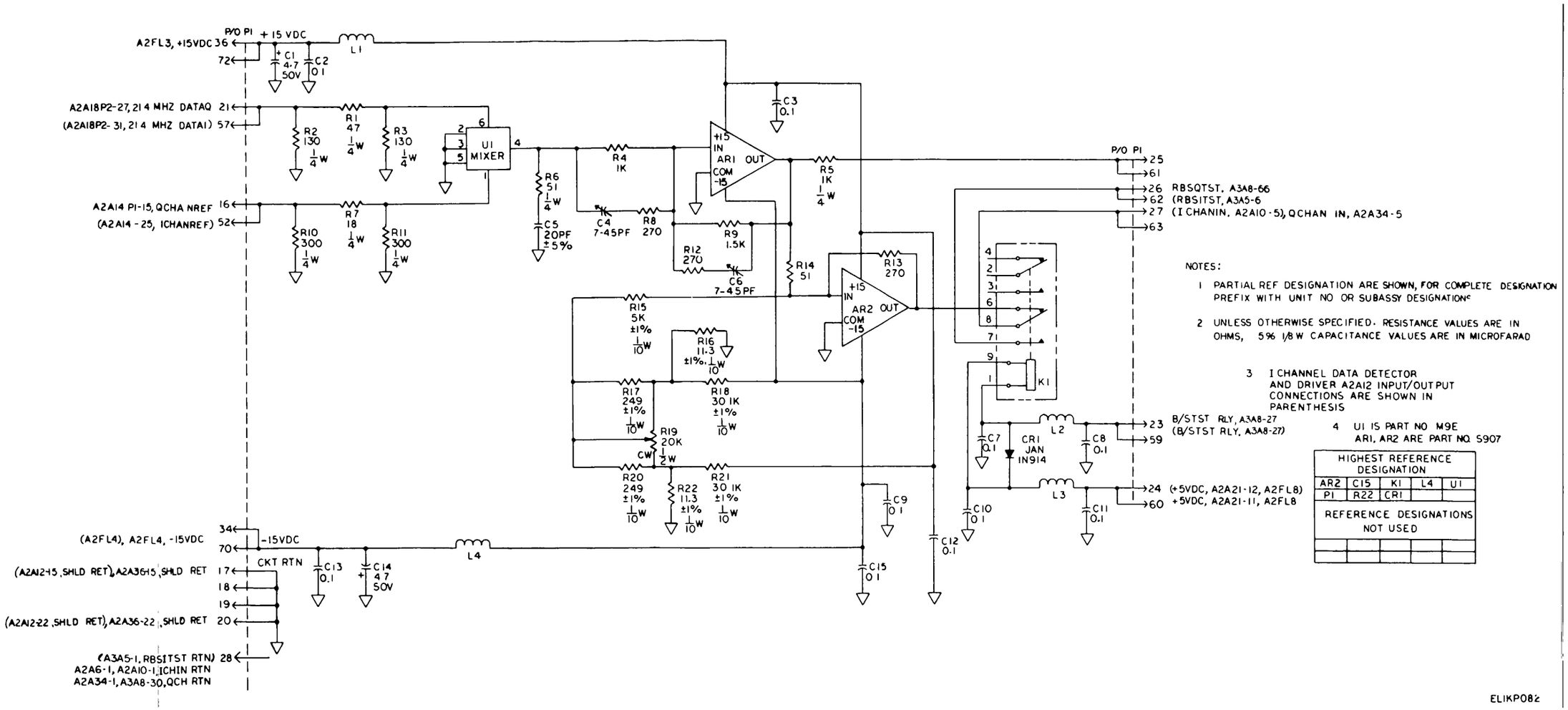


Figure FO-34. Data detector and driver, A2A12 and A2A36 (SM-D-731173), schematic diagram.

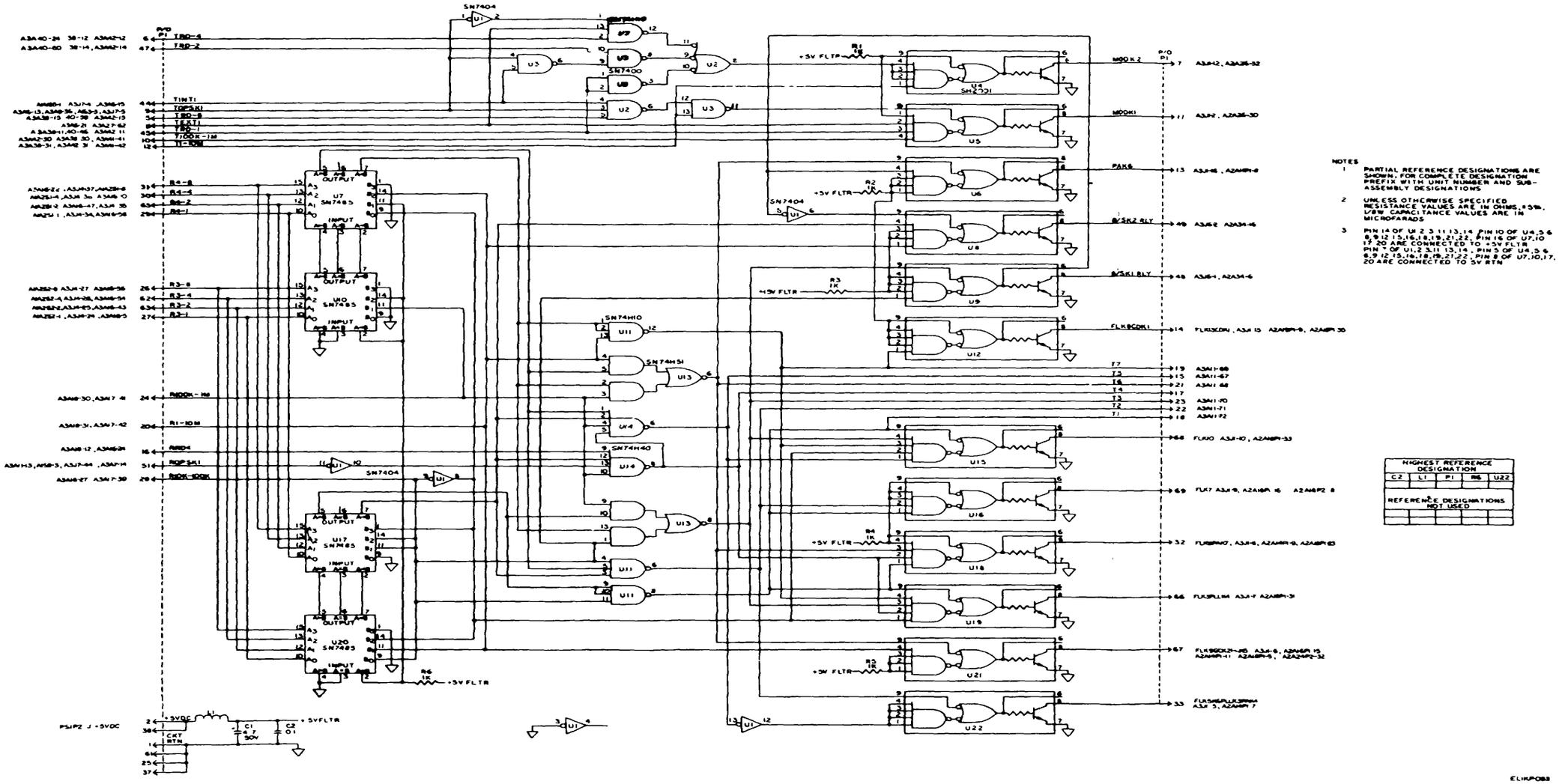


Figure FO-35. Relay control, A3A32 (SM-D-877710), schematic diagram.

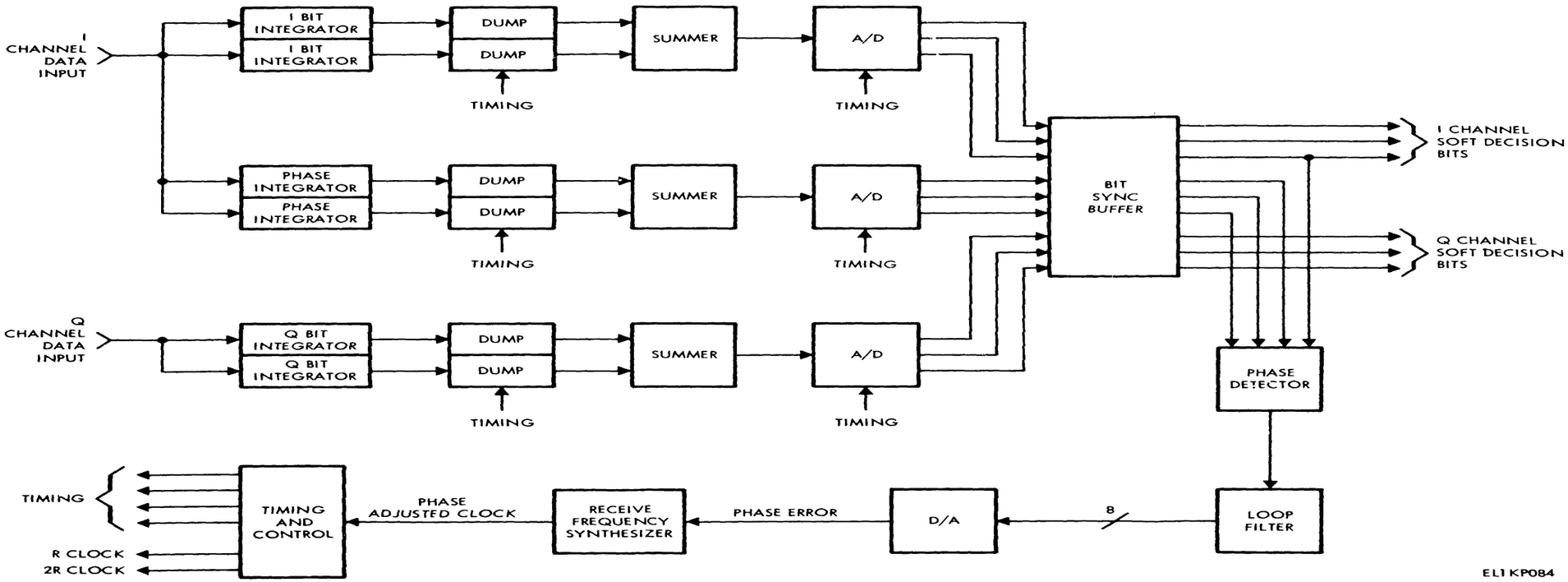


Figure FO-36. Receive bit synchronizer, general block diagram.

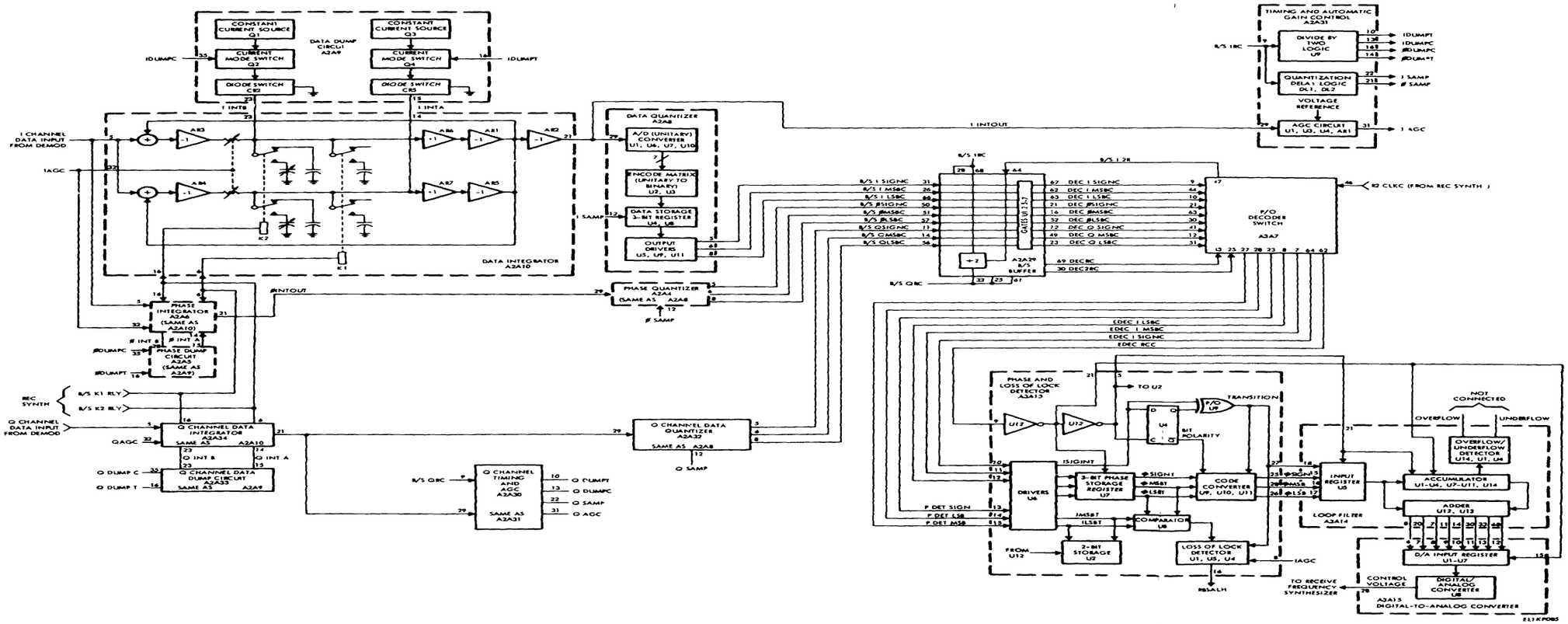
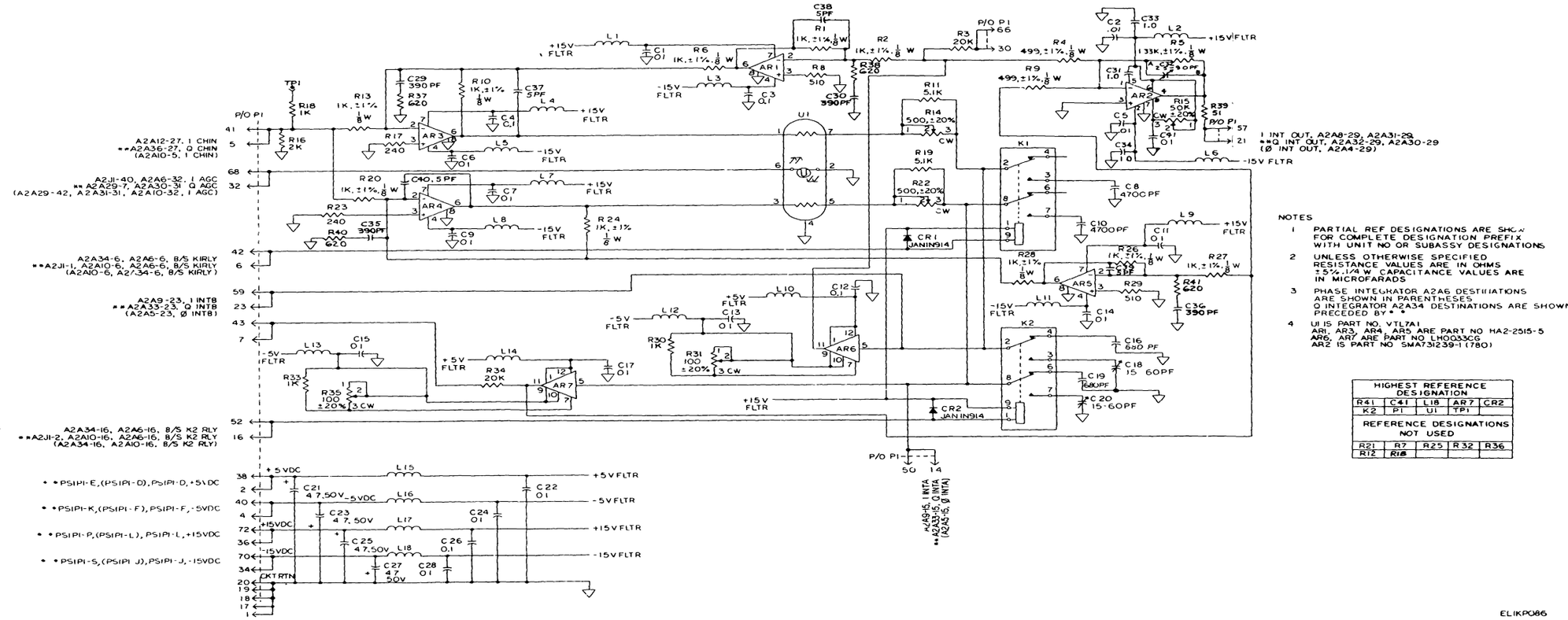


Figure FO-37. Receiver bit synchonizer, functional block diagram.



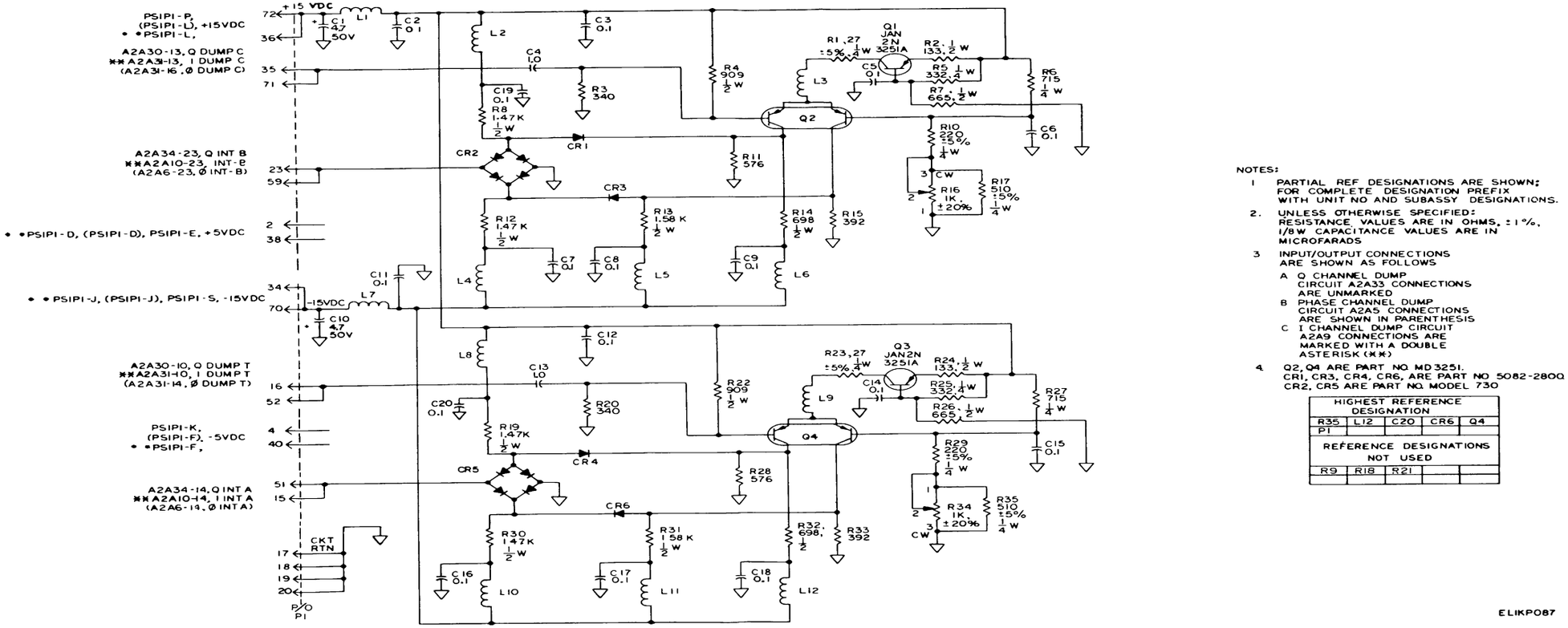
NOTES

1. PARTIAL REF DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO OR SUBASSY DESIGNATIONS.
2. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS ±5%-1/4 W CAPACITANCE VALUES ARE IN MICROFARADS
3. PHASE INTEGRATOR A2A6 DESTINATIONS ARE SHOWN IN PARENTHESES Q INTEGRATOR A2A34 DESTINATIONS ARE SHOWN PRECEDED BY * *
4. U1 IS PART NO. VTL7A1
   AR1, AR3, AR4, AR5 ARE PART NO HA2-2515-5
   AR6, AR7 ARE PART NO LH0033CG
   AR2 IS PART NO SMA731239-1 (780)

HIGHEST REFERENCE DESIGNATION				
R41	C41	L18	AR7	CR2
K2	P1	U1	TP1	
REFERENCE DESIGNATIONS NOT USED				
R21	R7	R25	R32	R36
R12	R18			

ELIKP086

Figure FO-38. Integrator, A2A6, A2A10, and A2A34 (SM-D731205), schematic diagram.



NOTES:

1. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO AND SUBASSY DESIGNATIONS.
2. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, ±1%, 1/8W CAPACITANCE VALUES ARE IN MICROFARADS
3. INPUT/OUTPUT CONNECTIONS ARE SHOWN AS FOLLOWS
   - A Q CHANNEL DUMP CIRCUIT A2A33 CONNECTIONS ARE UNMARKED
   - B PHASE CHANNEL DUMP CIRCUIT A2A5 CONNECTIONS ARE SHOWN IN PARENTHESIS
   - C I CHANNEL DUMP CIRCUIT A2A9 CONNECTIONS ARE MARKED WITH A DOUBLE ASTERISK (**)
4. Q2, Q4 ARE PART NO MD3251. CR1, CR3, CR4, CR6, ARE PART NO 5082-2800 CR2, CR5 ARE PART NO MODEL 730

HIGHEST REFERENCE DESIGNATION				
R35	L12	C20	CR6	Q4
P1				
REFERENCE DESIGNATIONS NOT USED				
R9	R18	R21		

ELIKP087

Figure FO-39. Dump circuit, A2A5, AA9, and A2A33 (SM-D-7321209), schematic diagram.

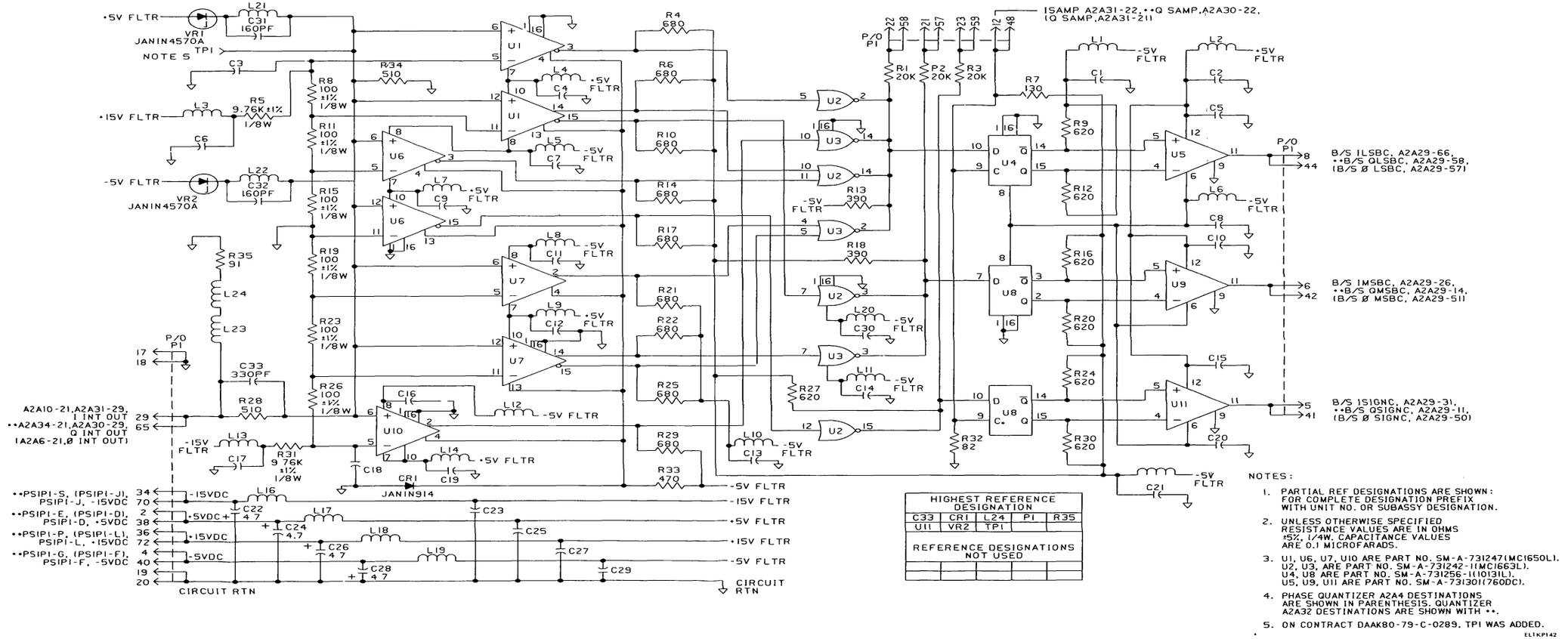


Figure FO-40. Quantizer A2A4, A2A8, and A2A32 (SM-D-7321213), schematic diagram.

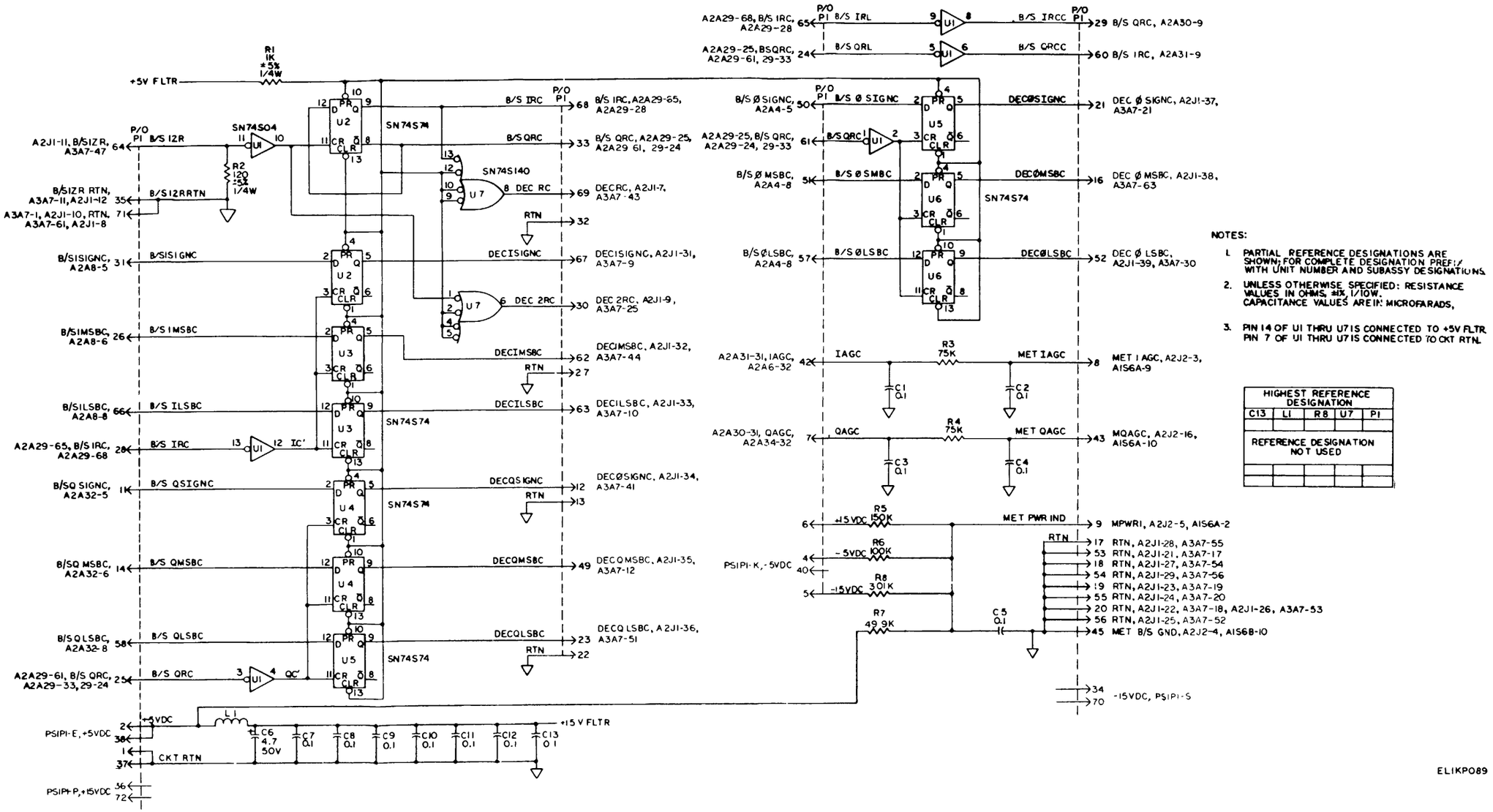


Figure FO-41. Bit sync buffer, A2A29 (SM-D-877695), schematic diagram.

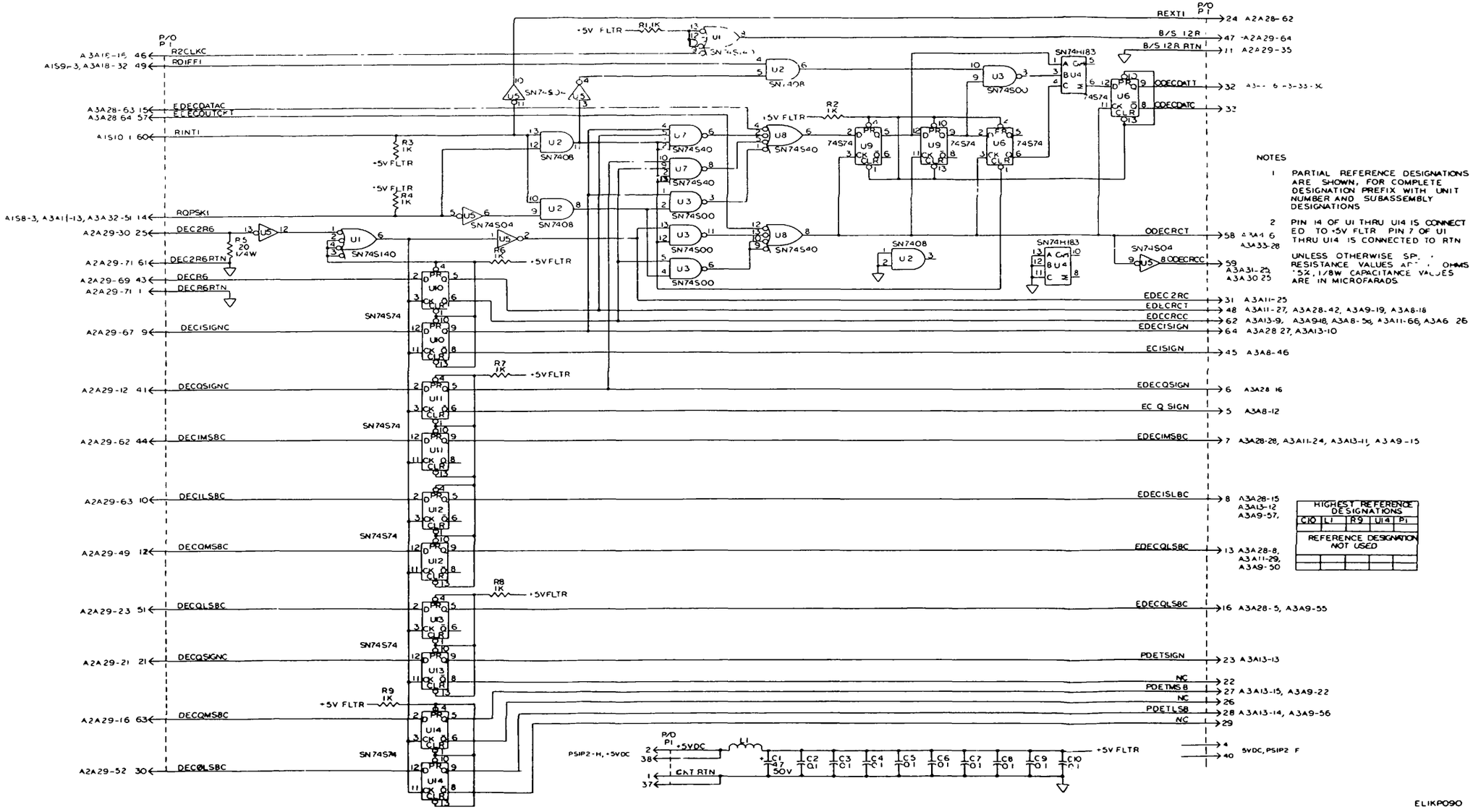


Figure FO-42. Decoder switch , A3A7 (SM-D-877700), schematic diagram.

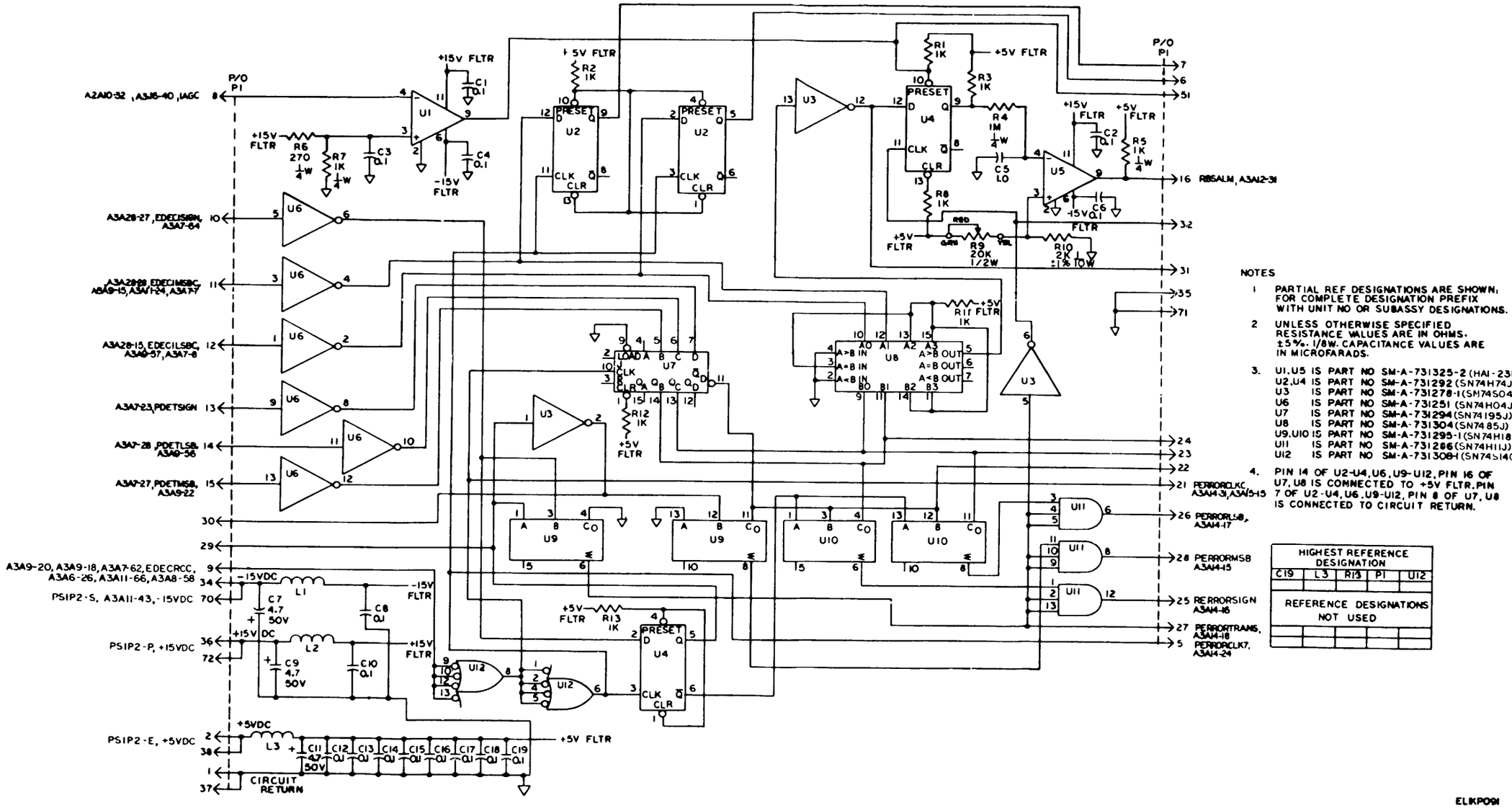


Figure FO-43. Phase and loss of lock detector, A3A13 (SM-D-731225), schematic diagram.

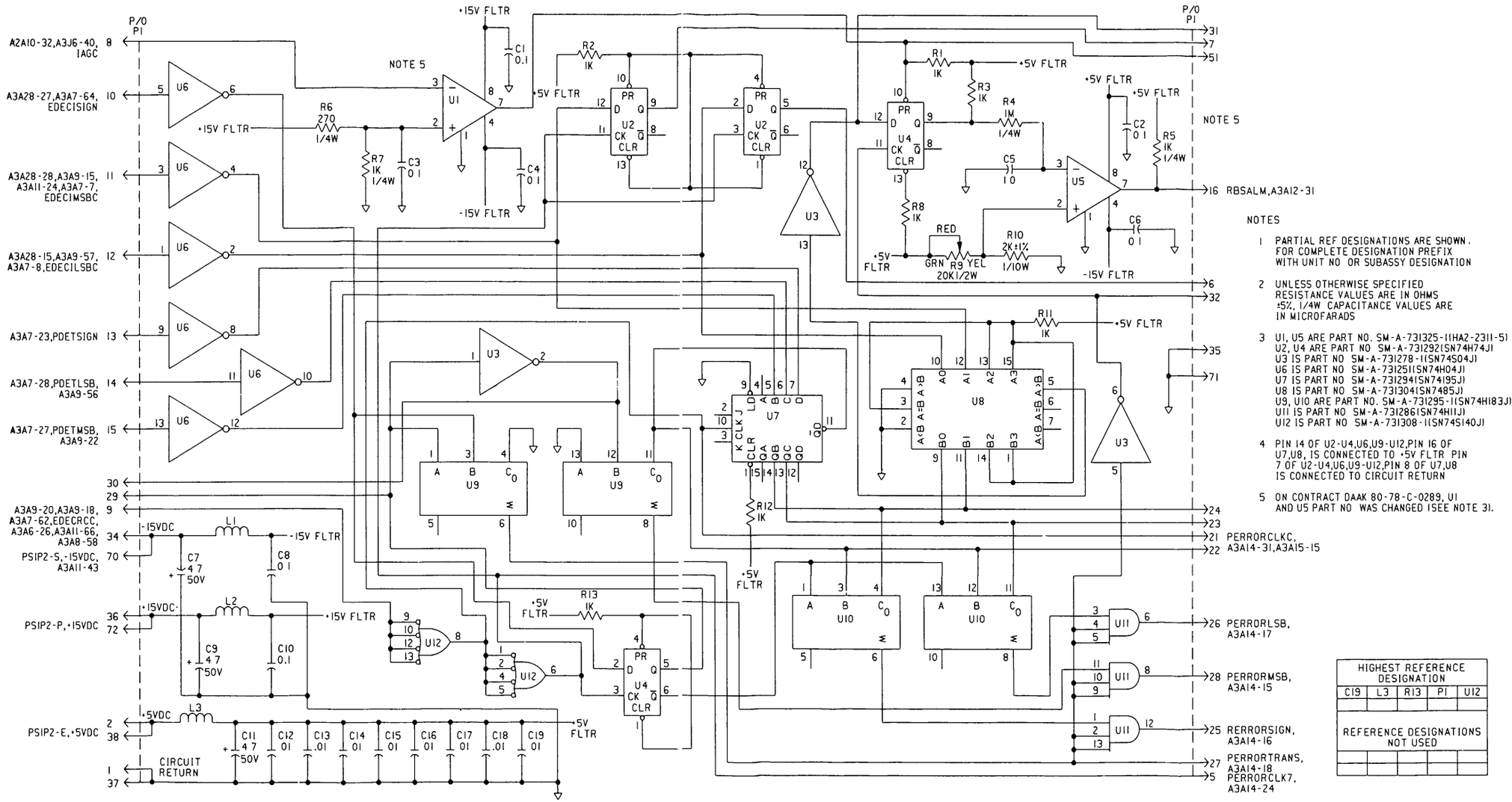


Figure FO-43.1. Phase and loss of lock detector, A3A13 (SM-D-877926), schematic diagram (Contract DAAB07-79-C-0289).

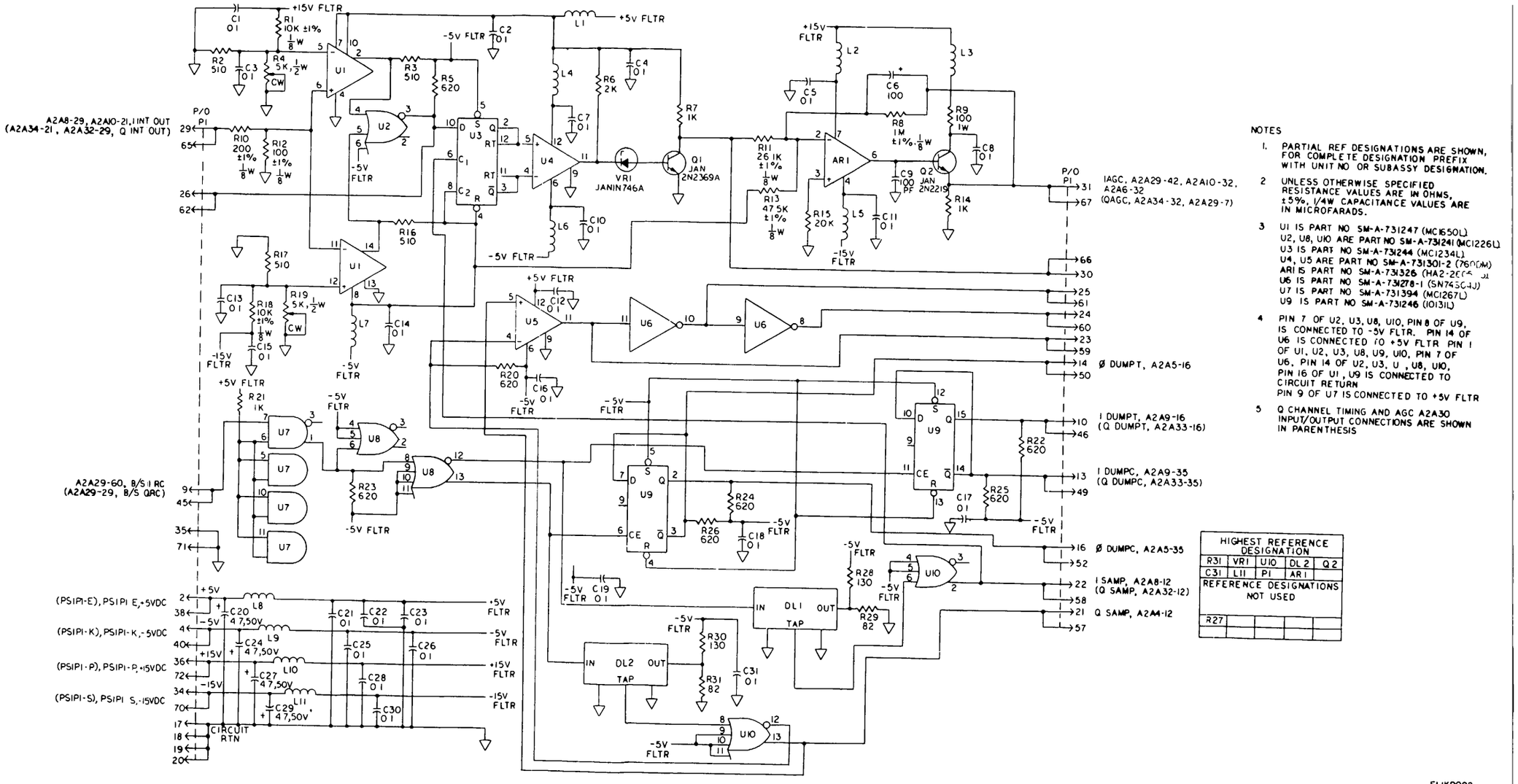


Figure FO-44. Timing and automatic gain control, A2A30 and A2A31 (SM-D-731229), schematic diagram.

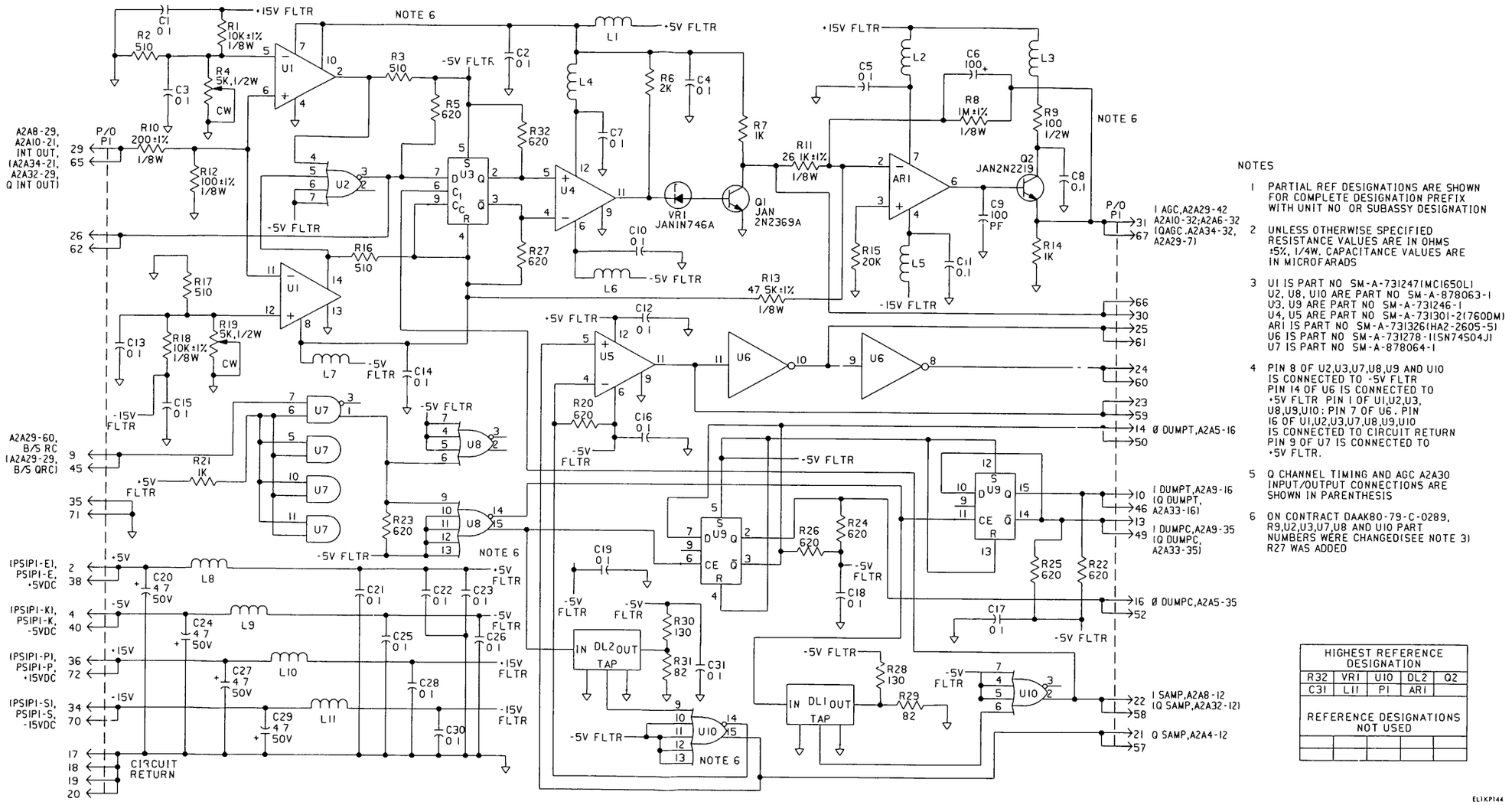


Figure FO-44.1

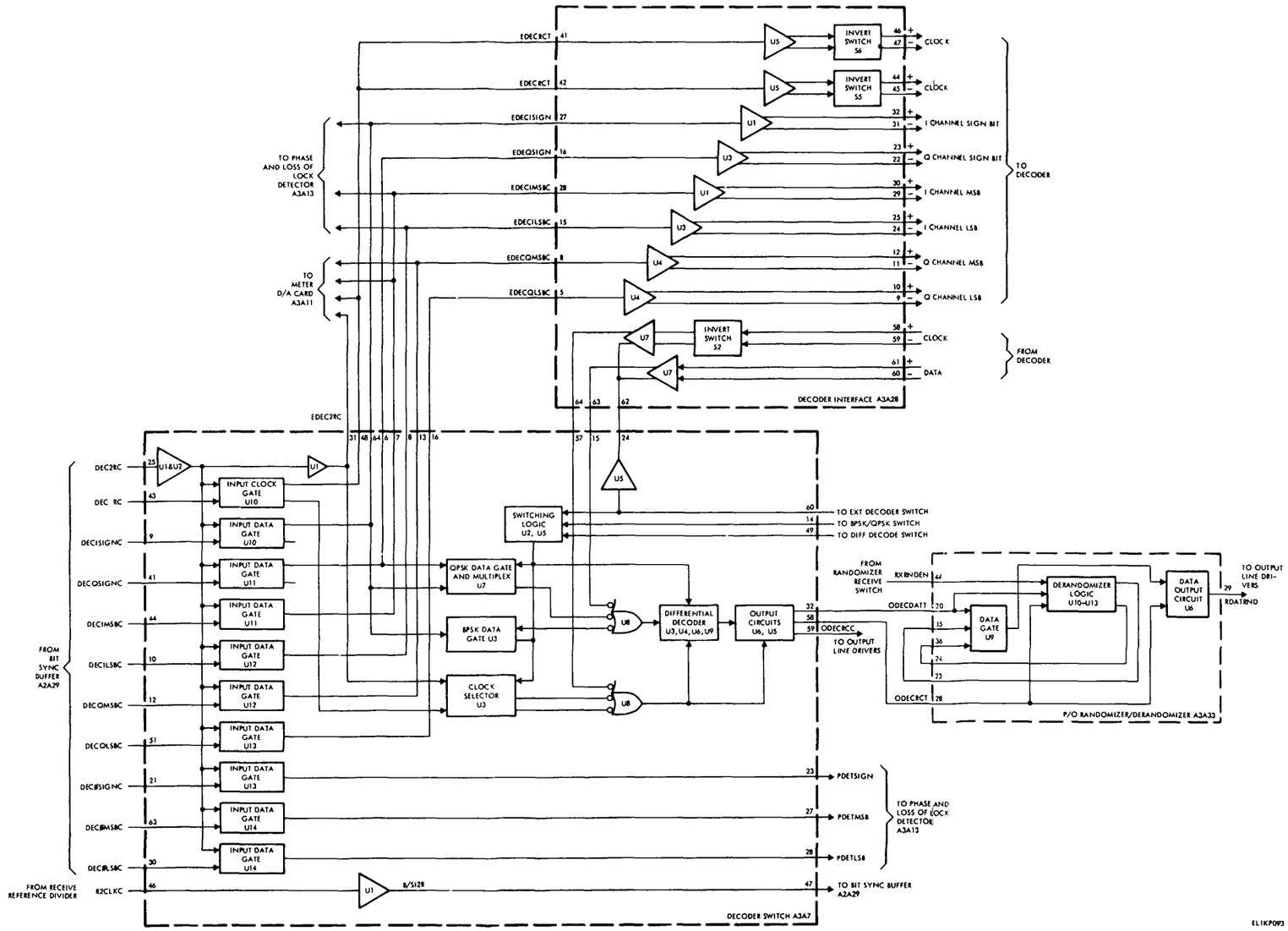


Figure FO-45. Decoder and interface, functional block diagram.

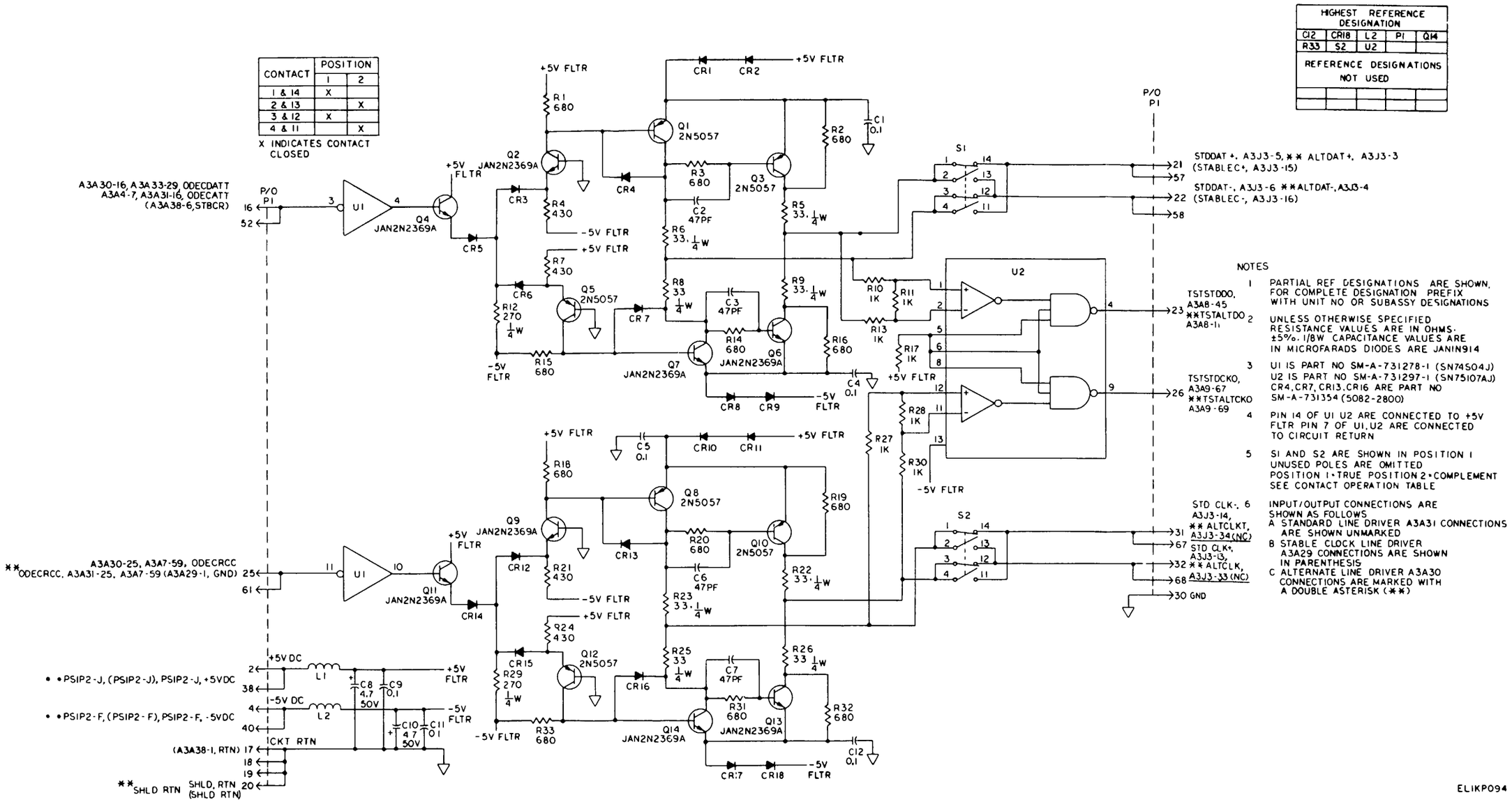


Figure FO-46. Line driver, A3A29, A3A30, and A#A31 (SM-D-742053), schematic diagram.

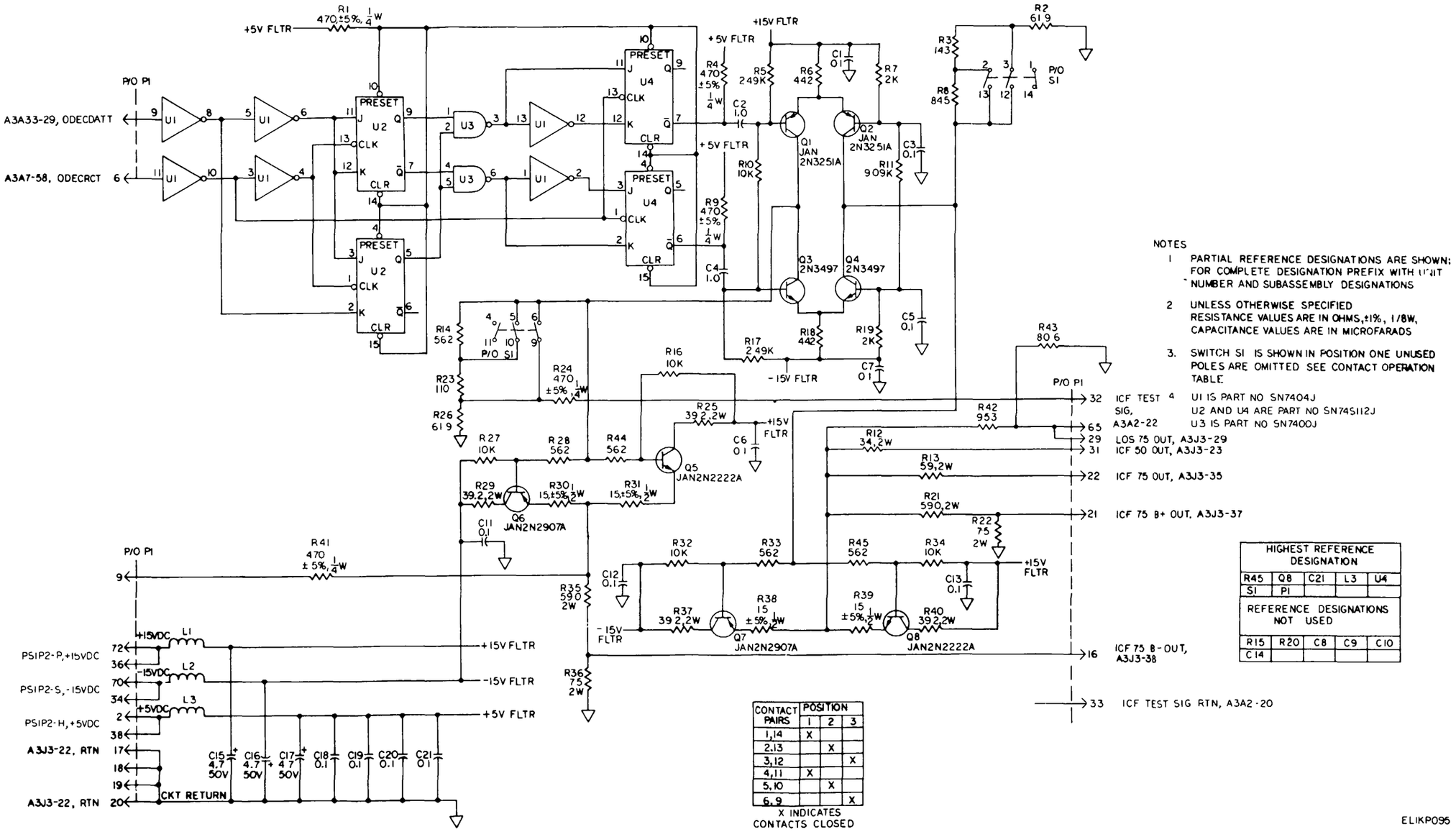


Figure FO-47. LOS/cable driver, A3A4 (SM-D-74081), schematic diagram.

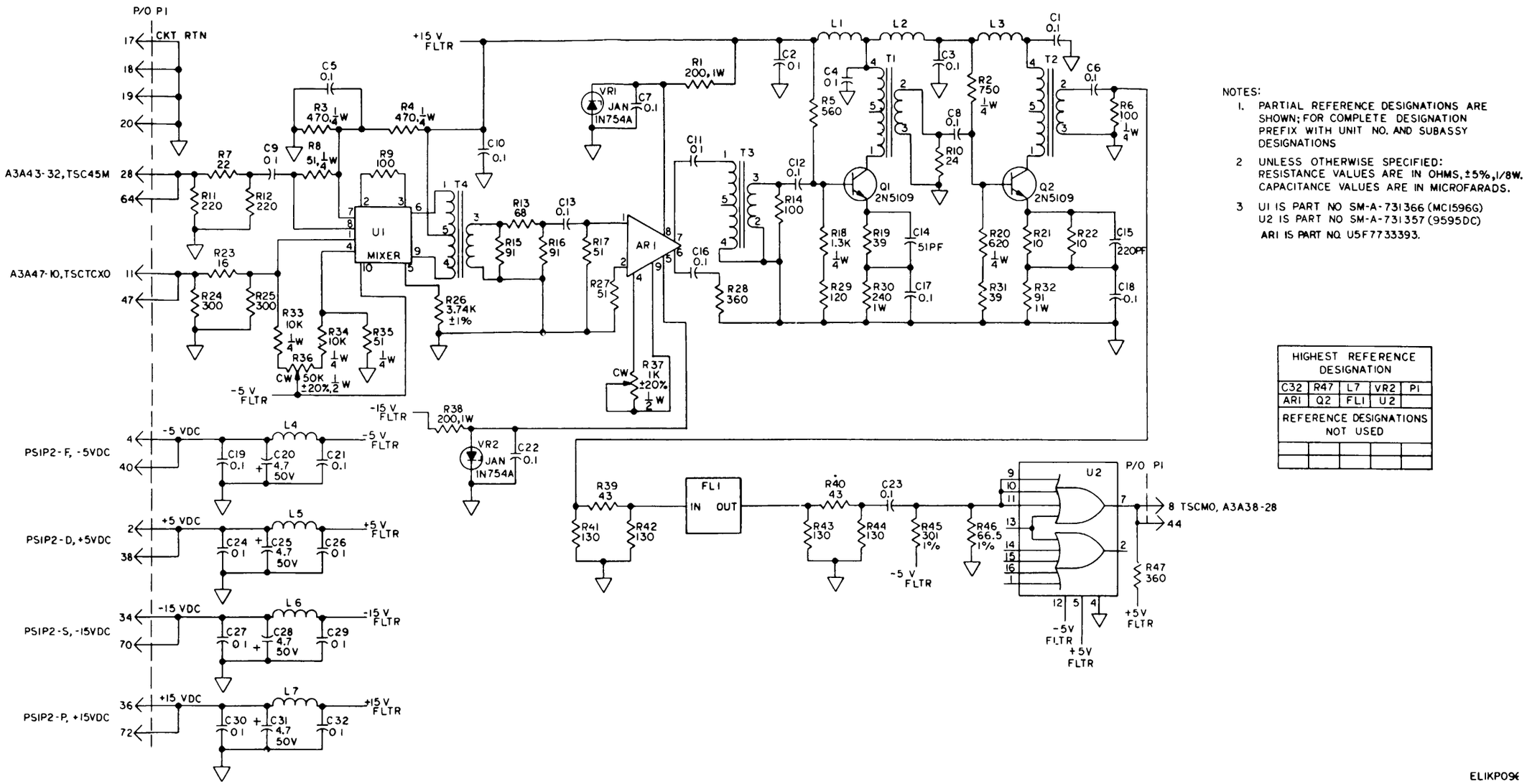


Figure FO-48. Stable clock, A3A99 (SM-D-731201), schematic diagram.

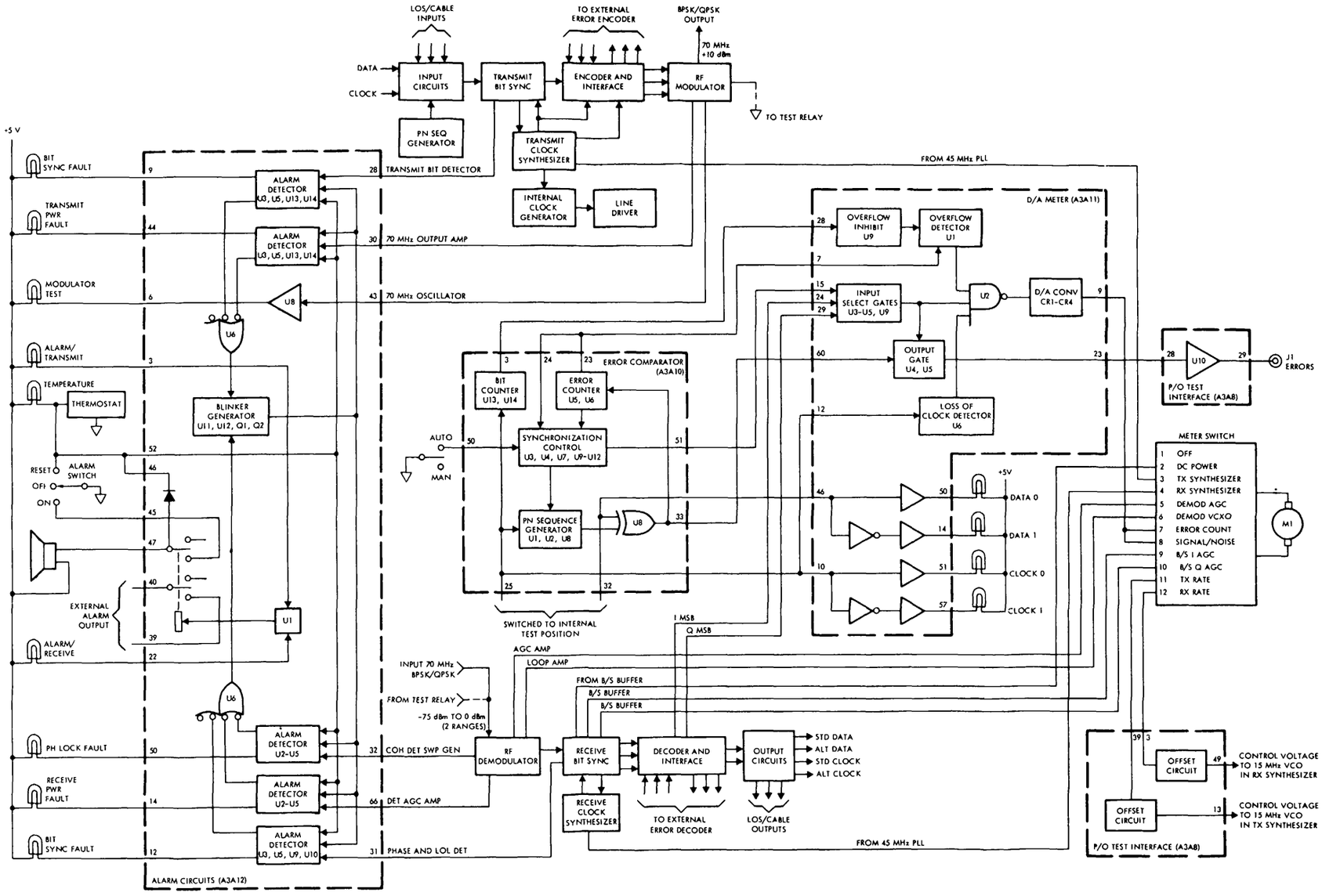


Figure FO-49. Fault and status monitor,, functional block diagram.

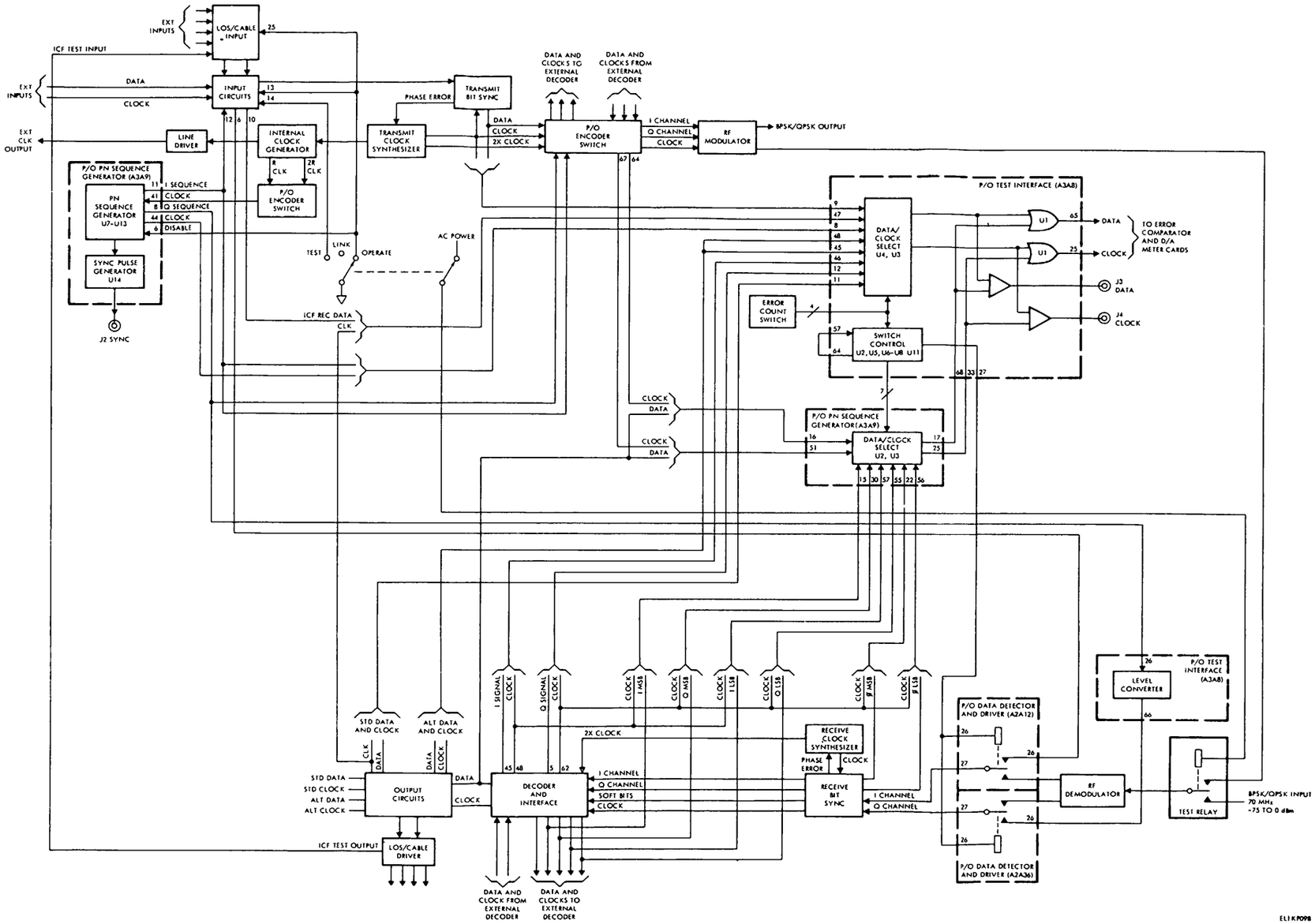
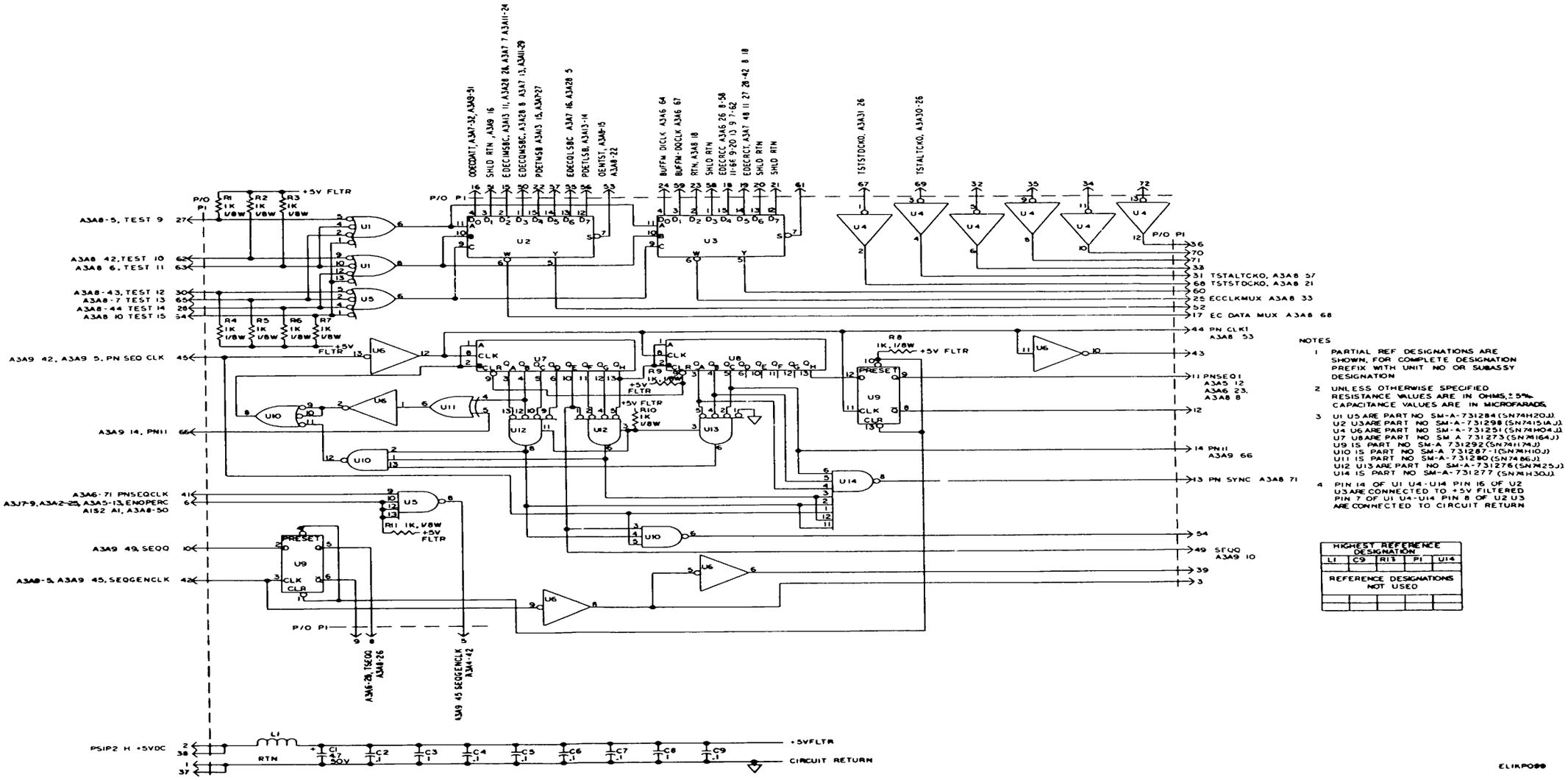


Figure FO-50. Test circuits, functional block diagram.



ELIKP088

Figure FO-51. 11-bit pseudo-random sequence generator, A3A9 (SM-D-742057), schematic diagram.

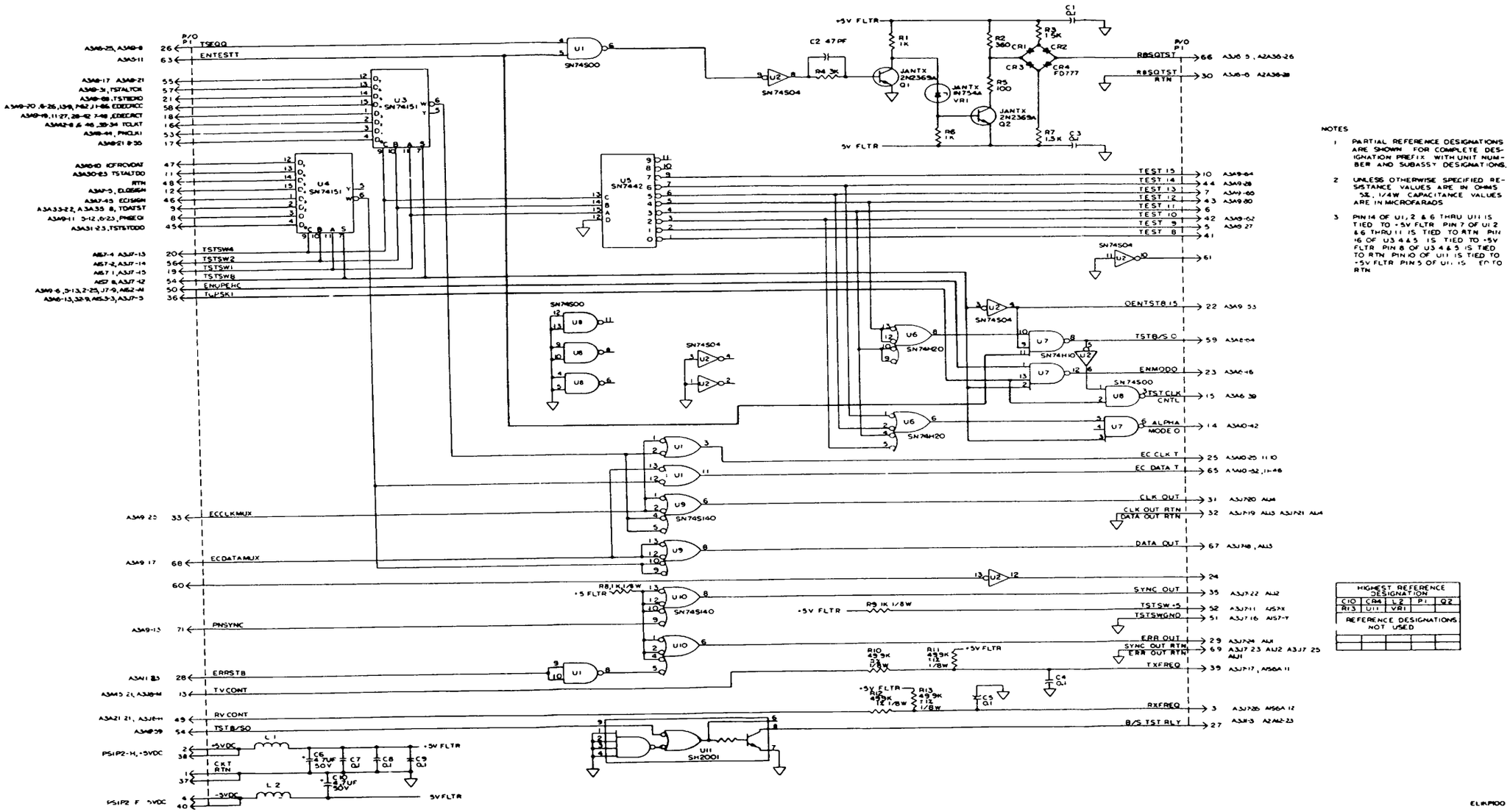


Figure FO-52. Test interface, A3A8 (SM-D-877705), schematic diagram.

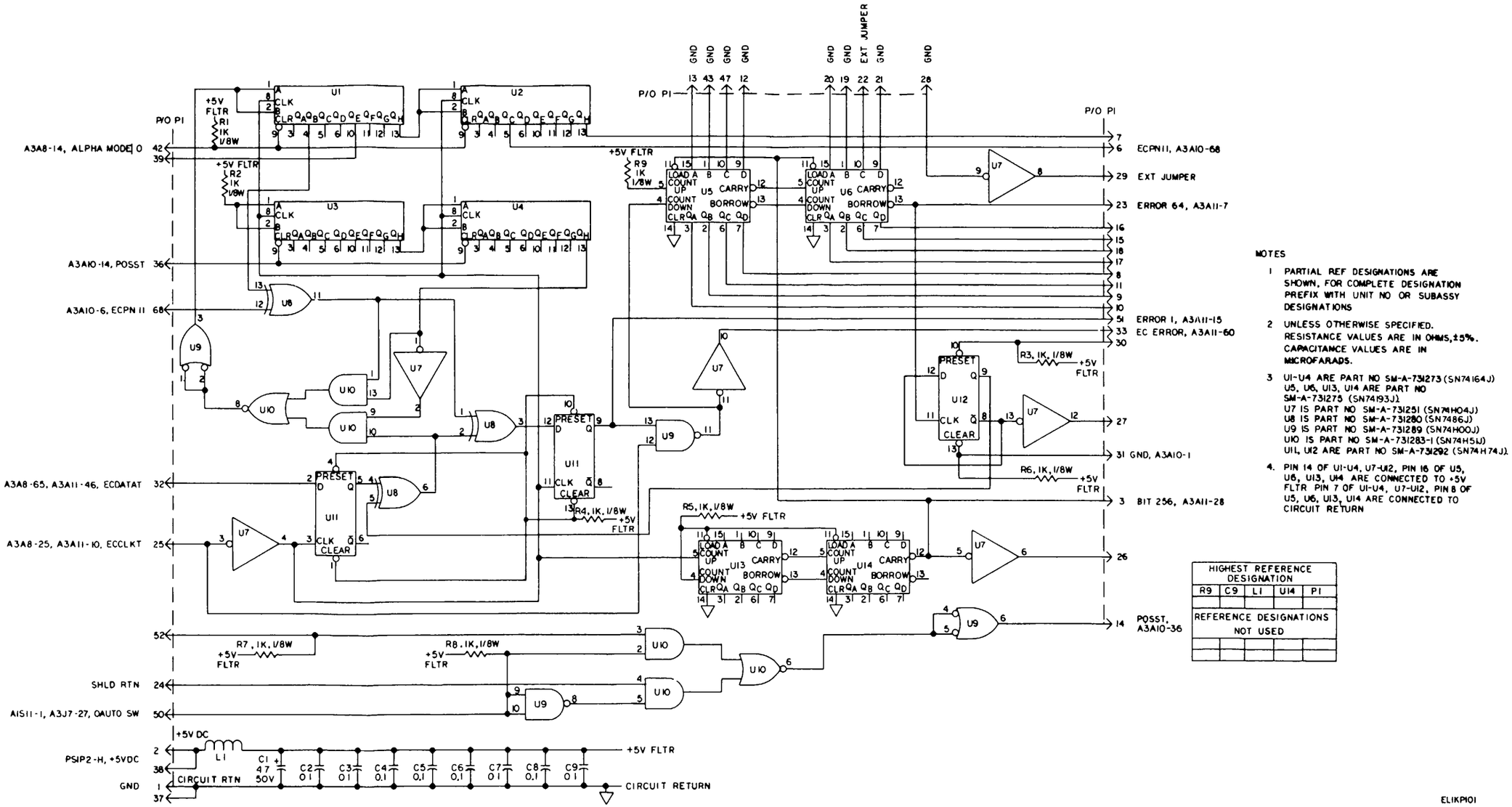


Figure FO-53. Error comparator, A3A10 (SM-D-742061), schematic diagram.

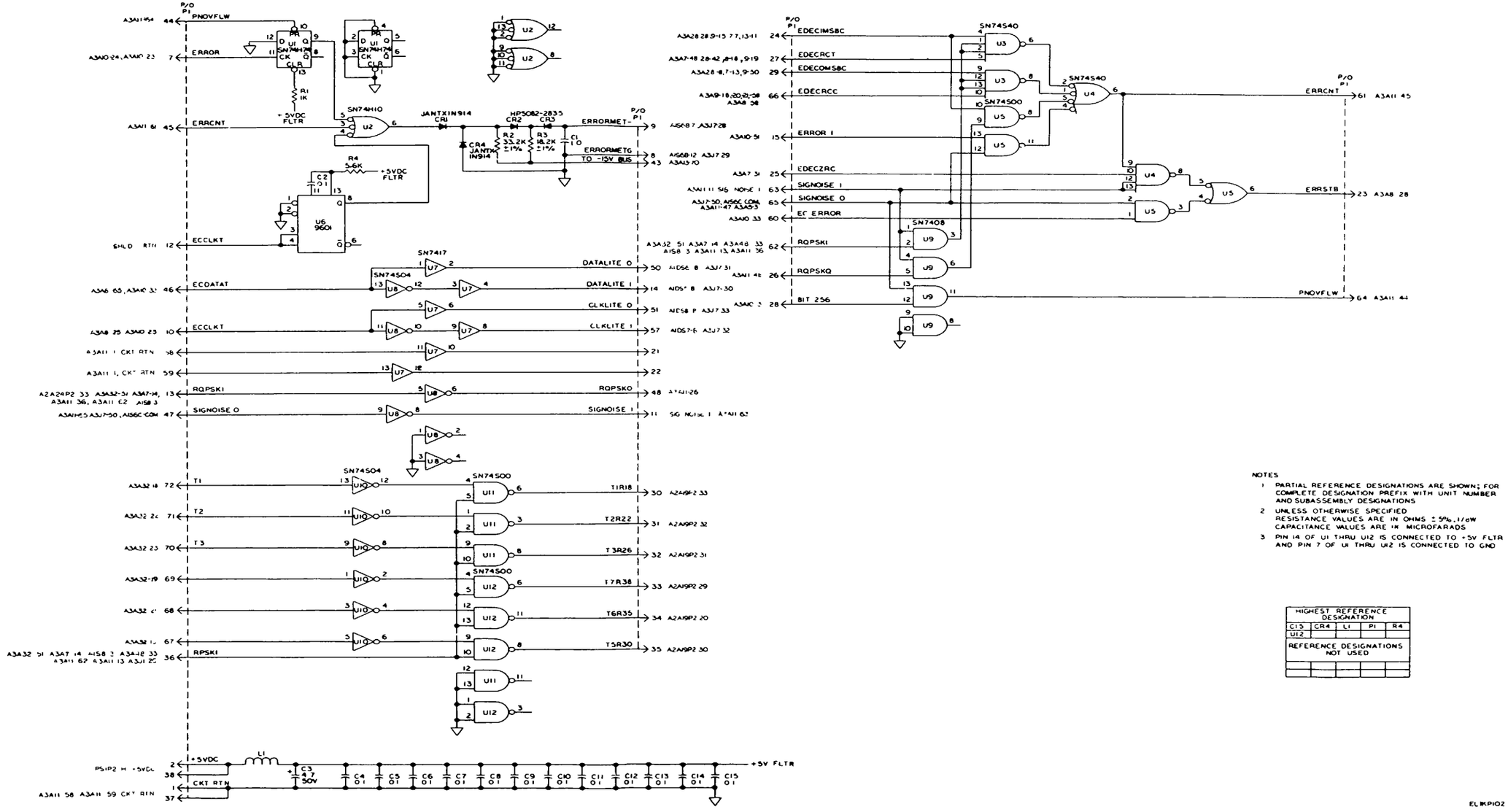


Figure FO-54. Dialog-to-analog meter, A3A11 (SM-D-877725), schematic diagram.

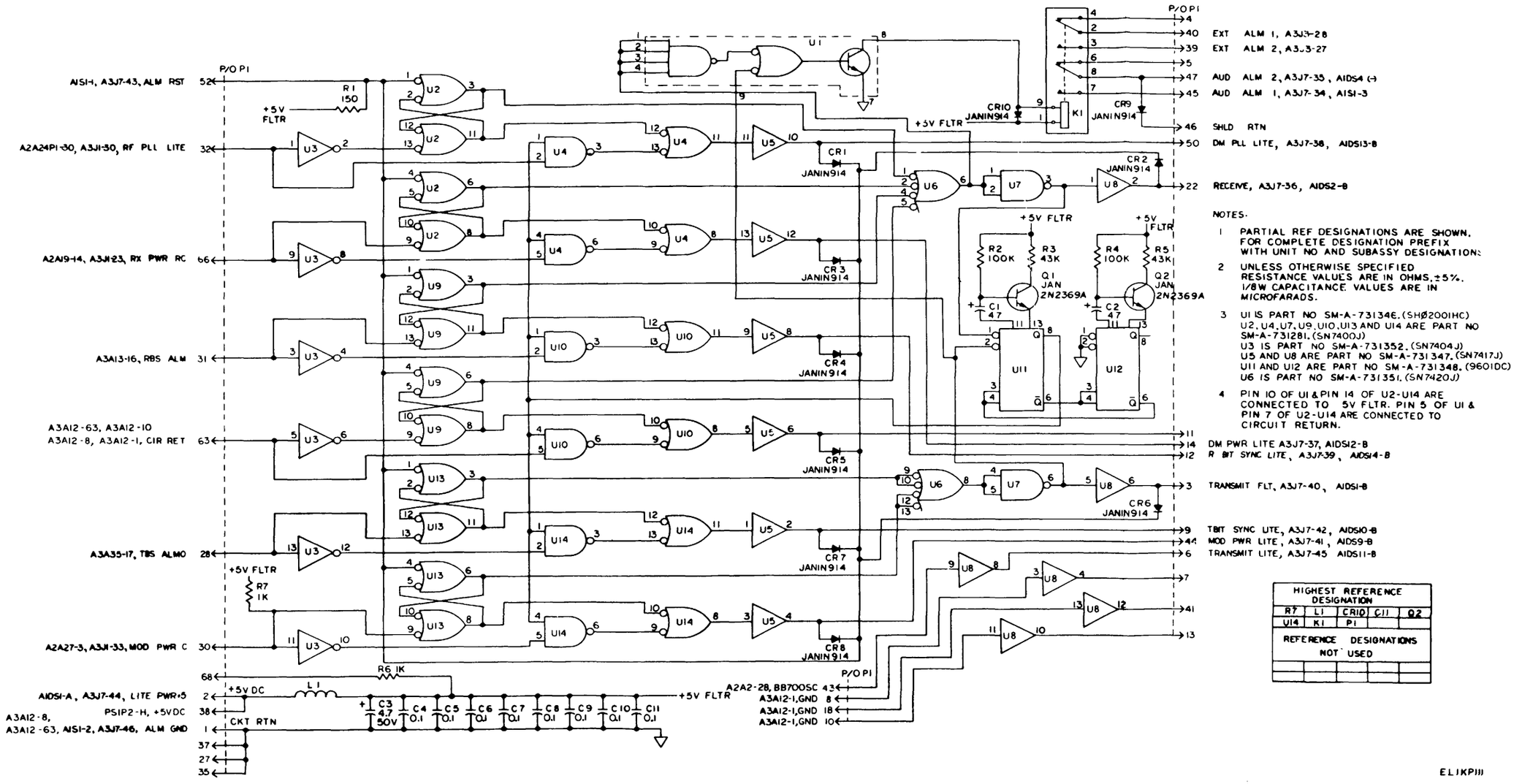


Figure FO-55. Alarm circuit A3A12 (SM-D-742033), schematic diagram.

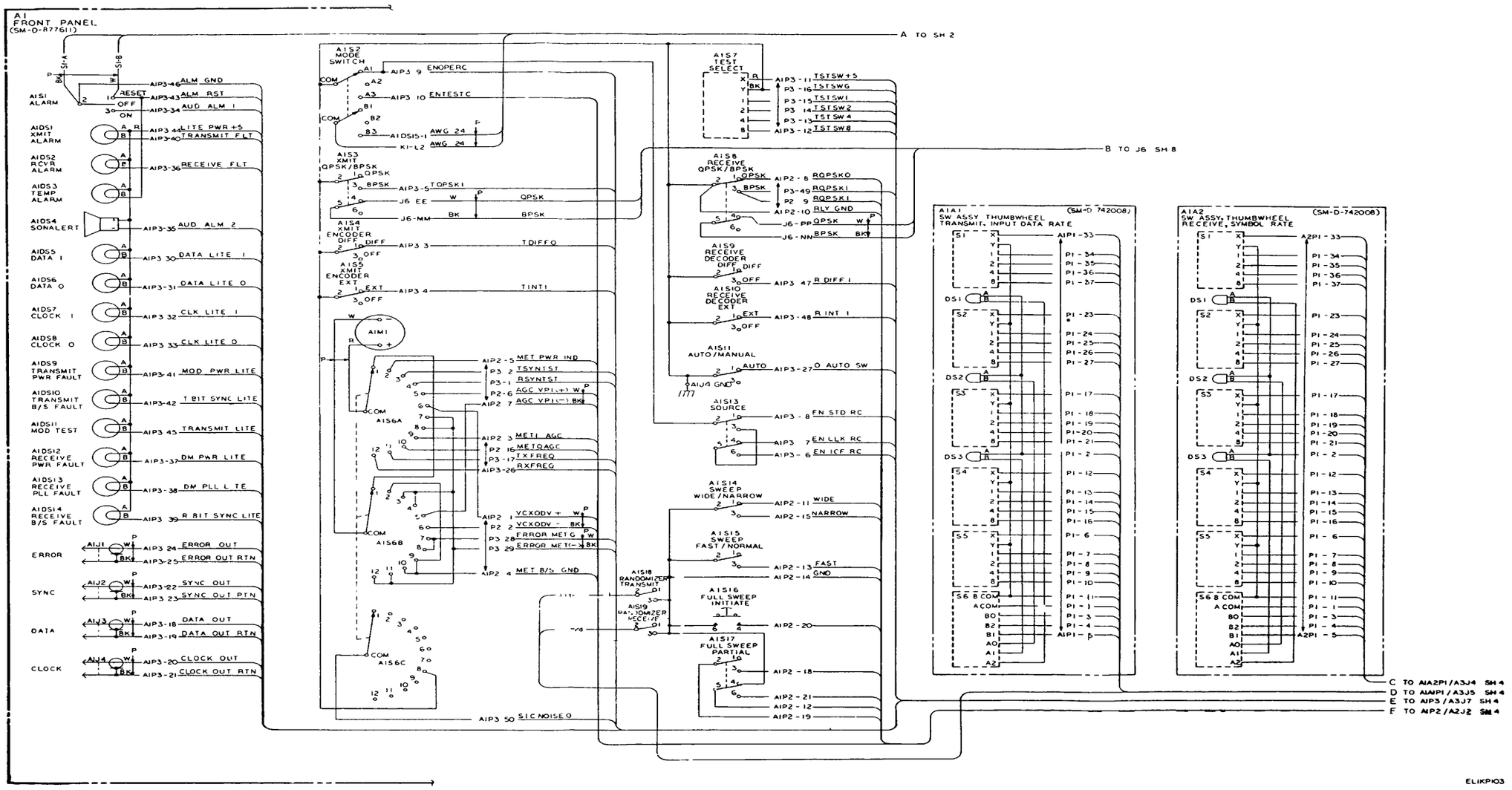


Figure FO-56. QPSK/BPSK connection diagram (sheet 1 of 8).

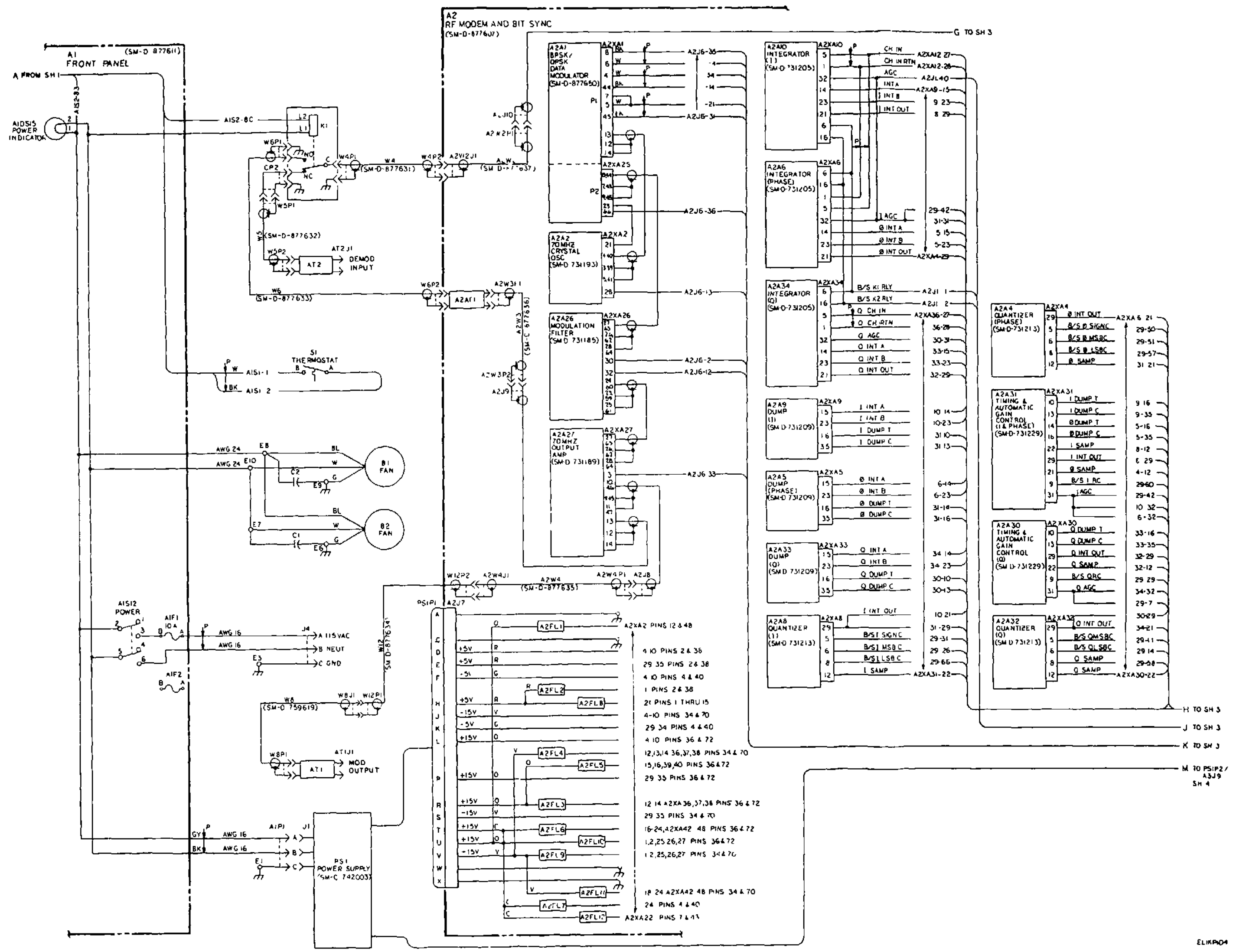


Figure FO-56 (2). QPSK/BPSK connection diagram (sheet 2 of 8)

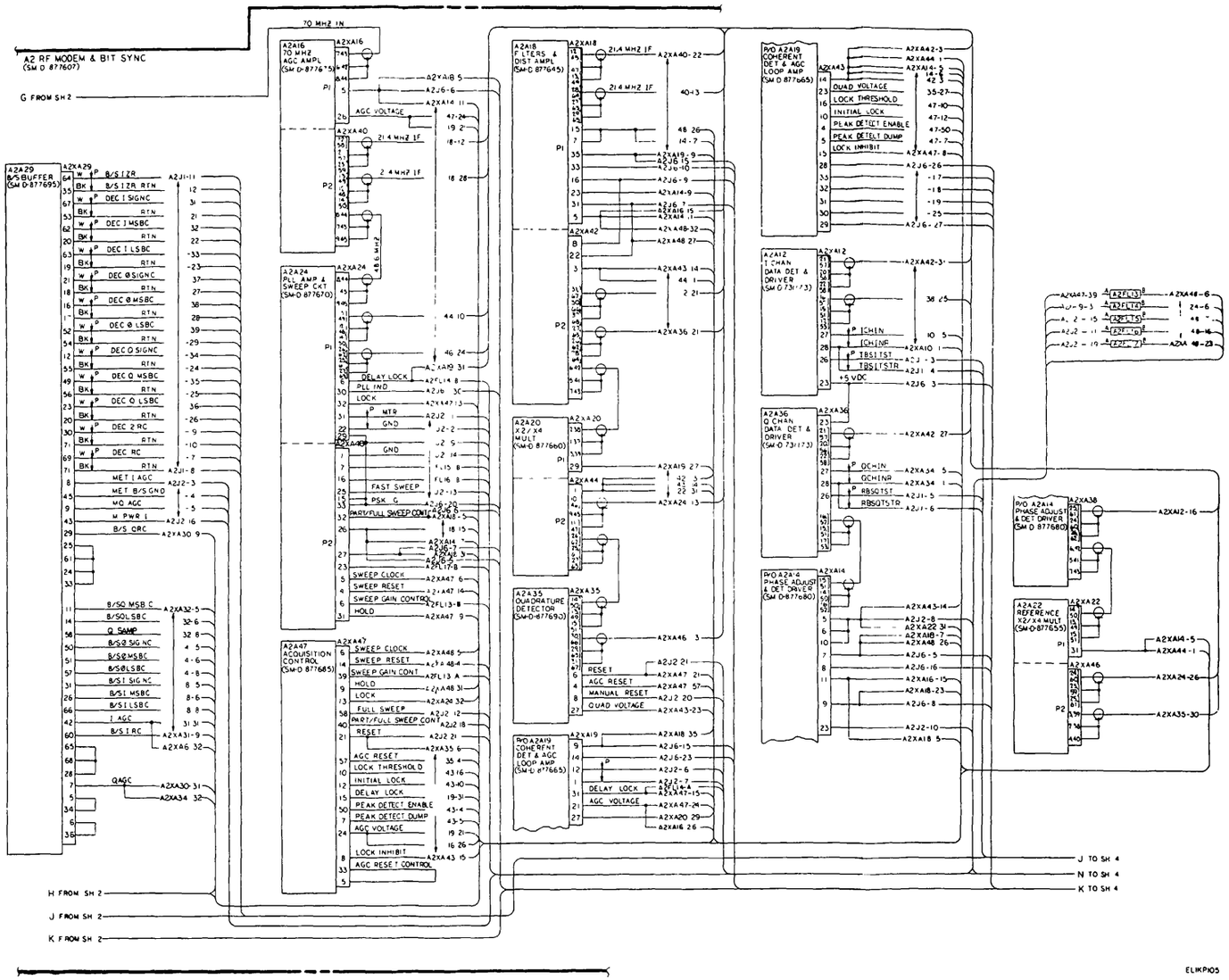


Figure FO-56 (3). QPSK/BPSK connection diagram (sheet 3 of 8)

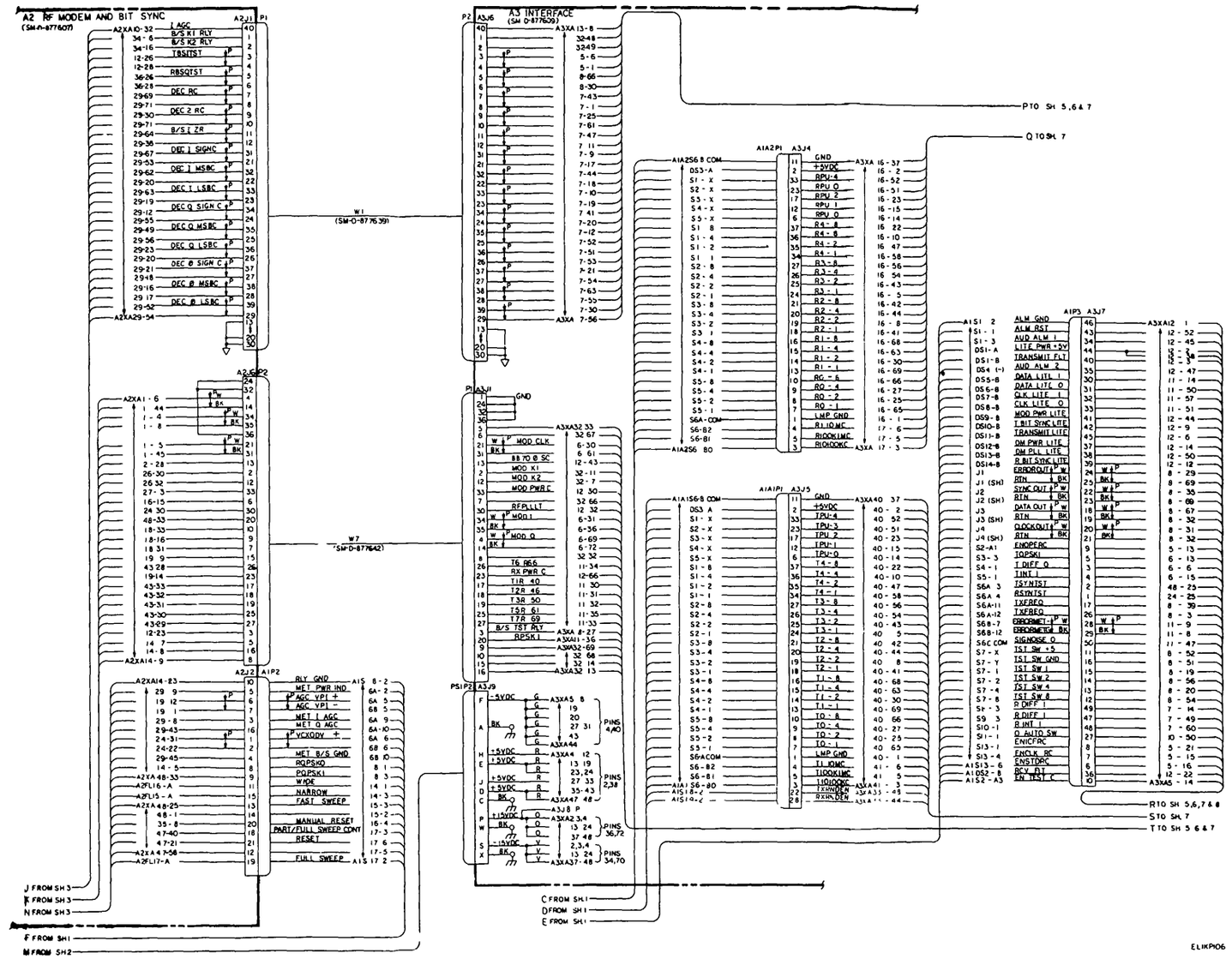


Figure FO-56 (4). QPSK/BPSK connection diagram (sheet 4 of 8)

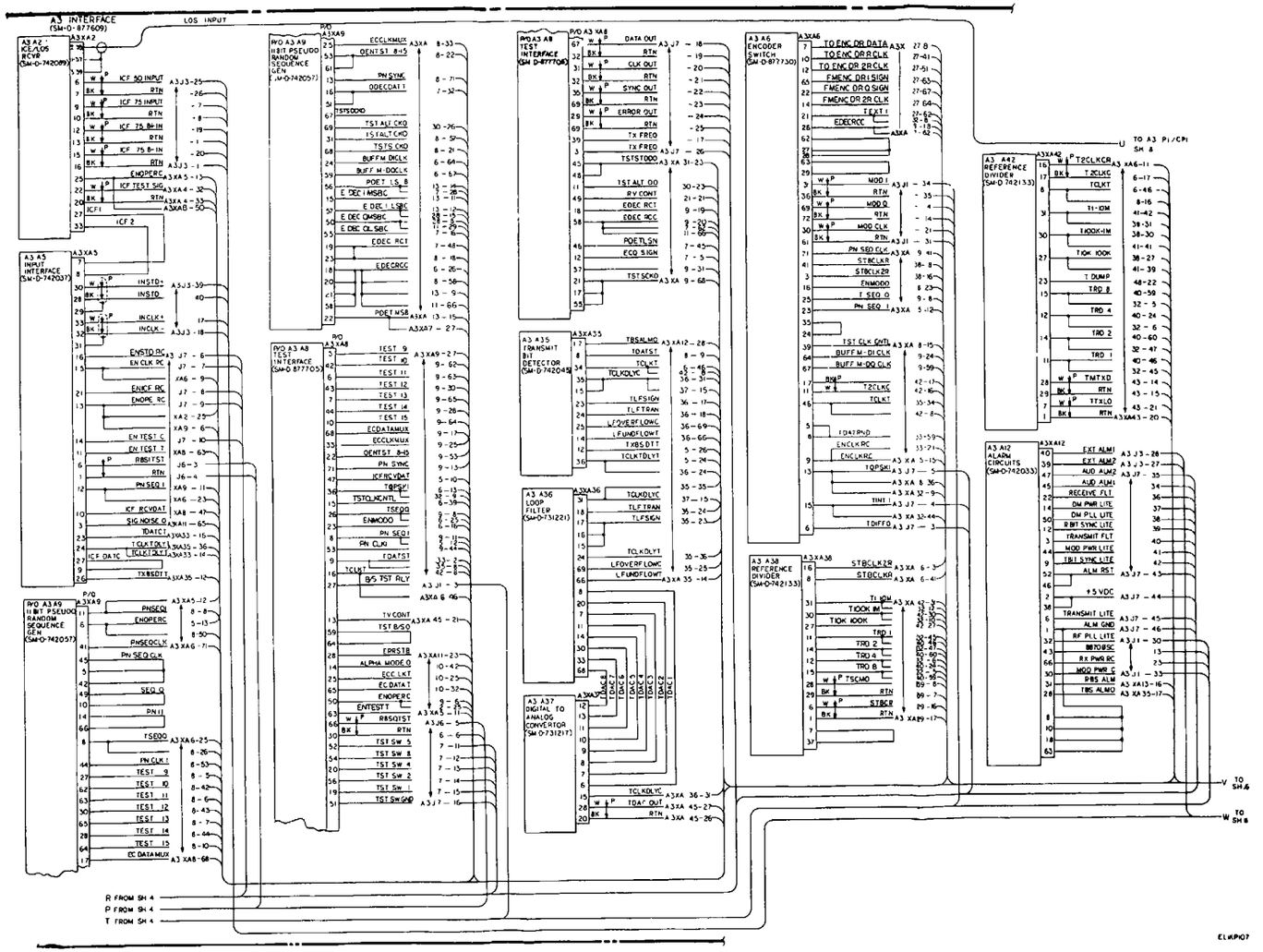


Figure FO-56 (5). QPSK/BPSK connection diagram (sheet 5 of 8)

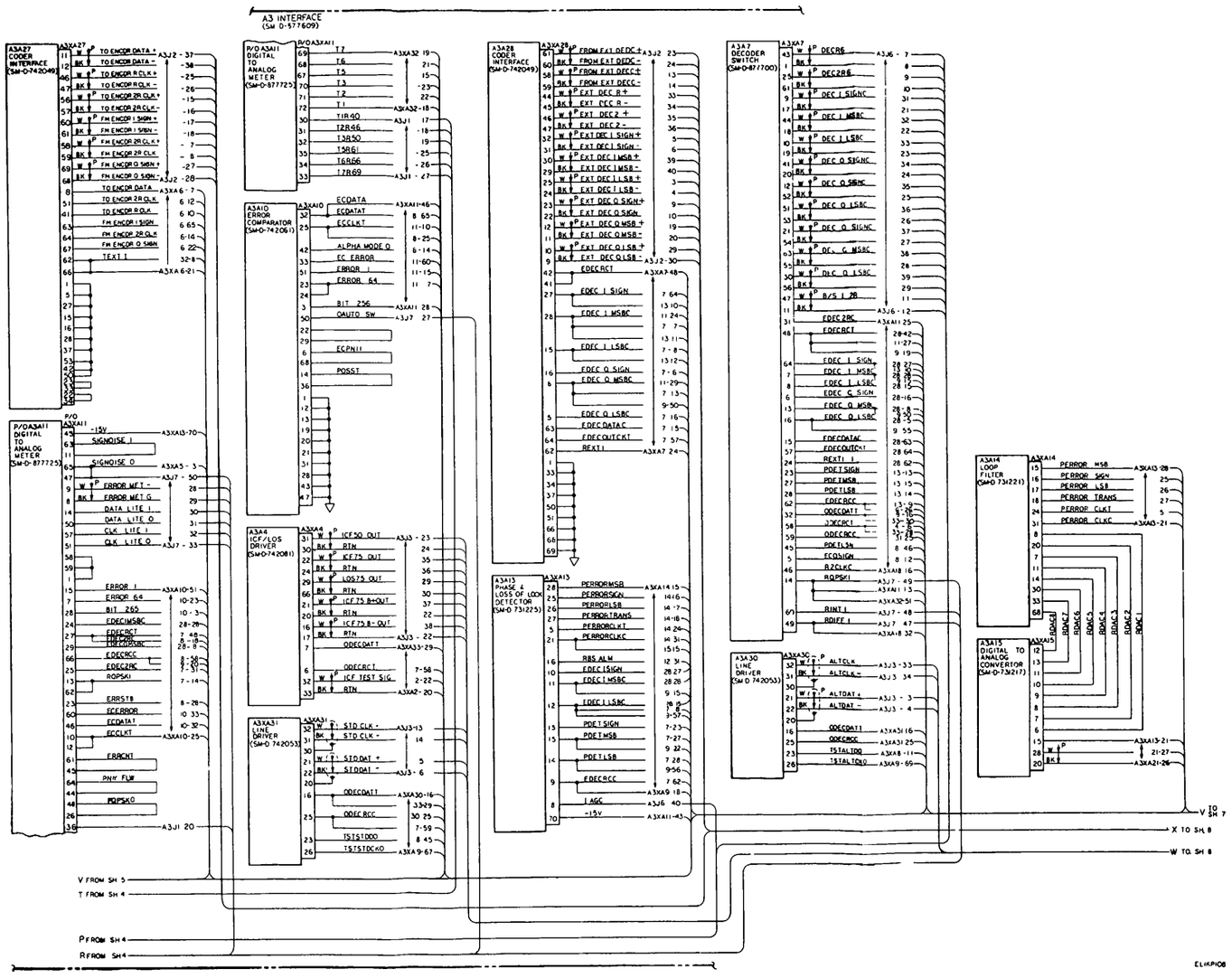


Figure FO-56 (6). QPSK/BPSK connection diagram (sheet 6 of 8)

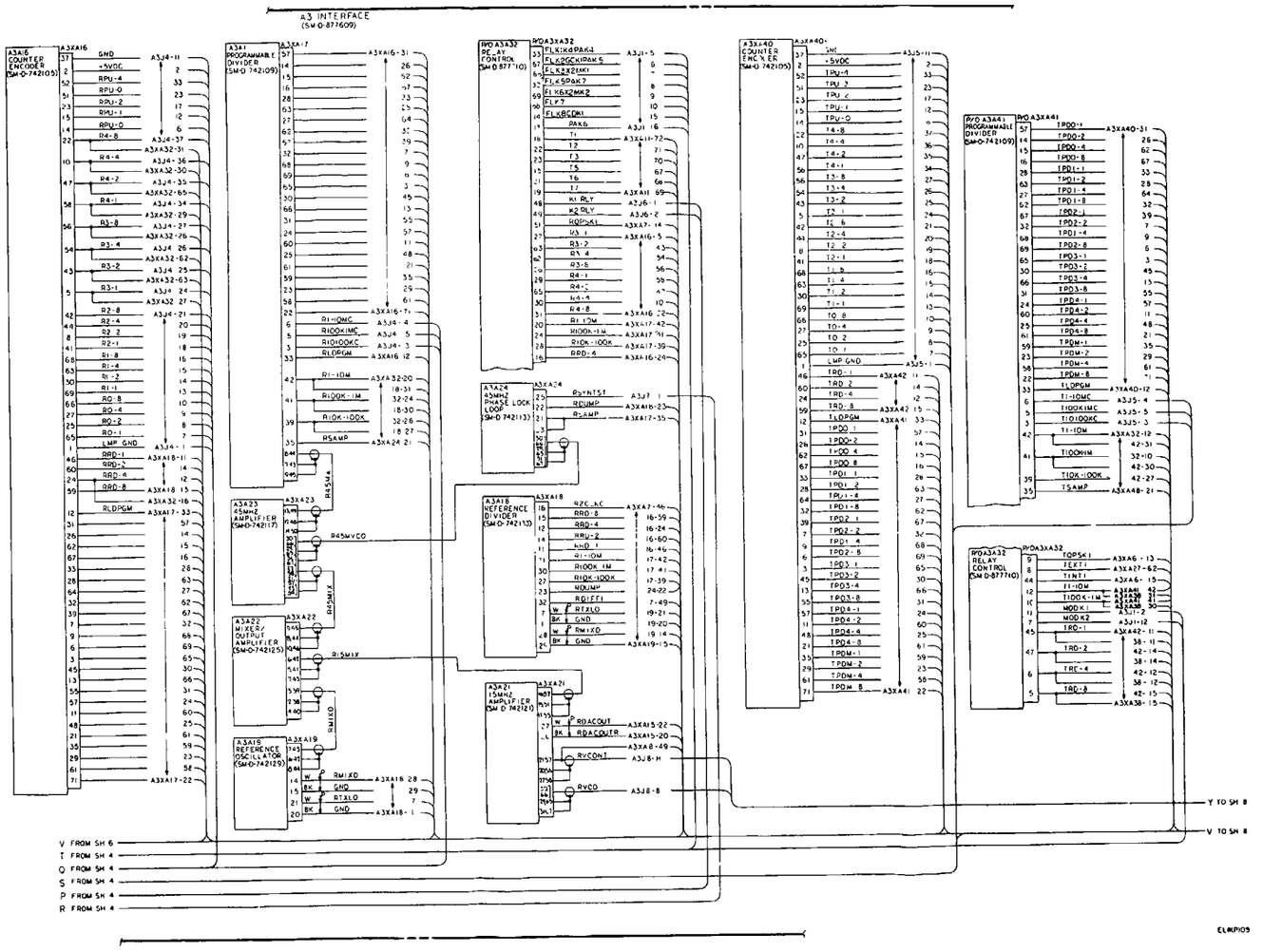


Figure FO-56 (7). QPSK/BPSK connection diagram (sheet 7 of 8)

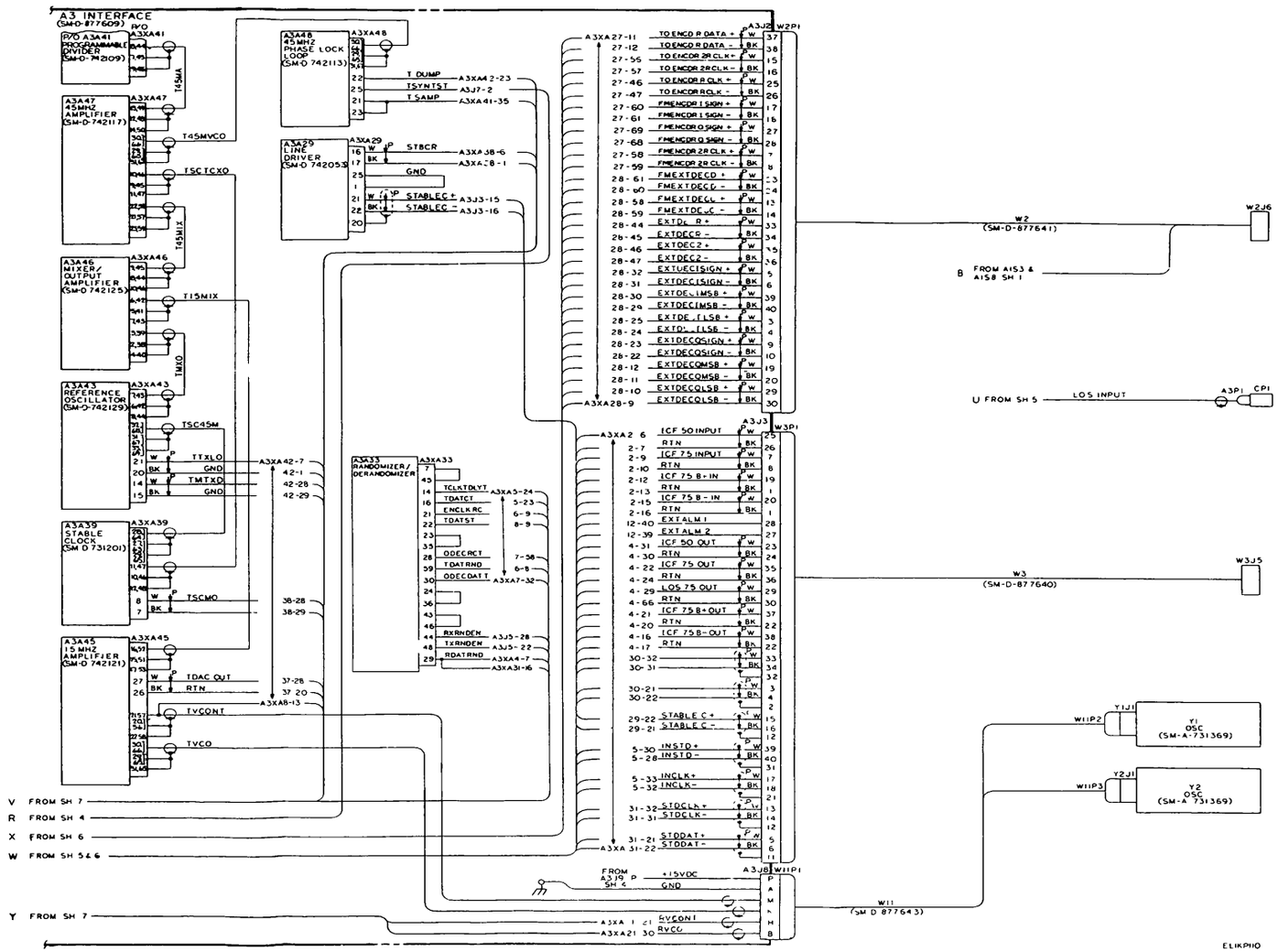


Figure FO-56 (8). QPSK/BPSK connection diagram (sheet 8 of 8)

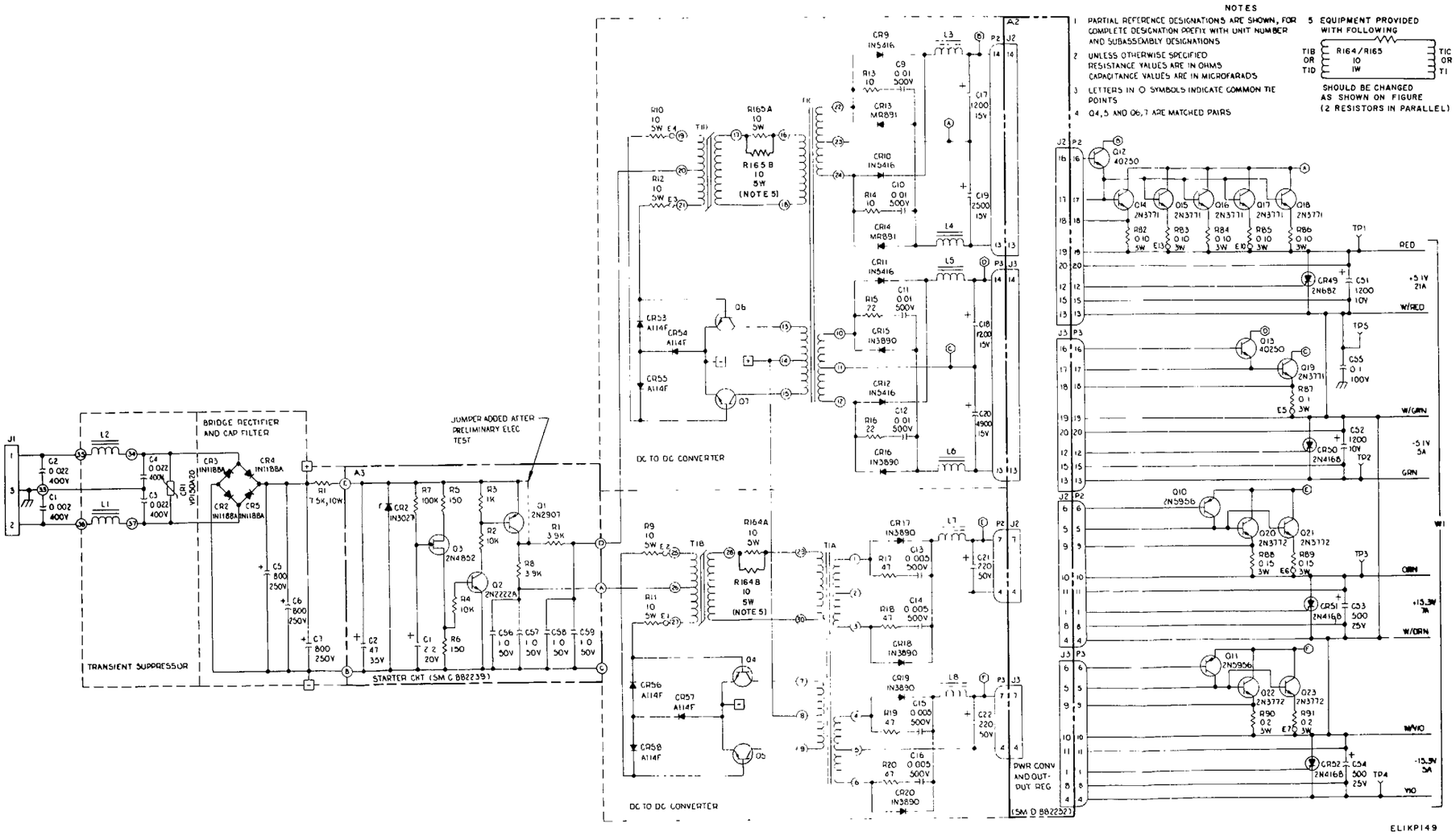


Figure FO-57. Power supply PS1 (SM-C-742003, schematic diagram

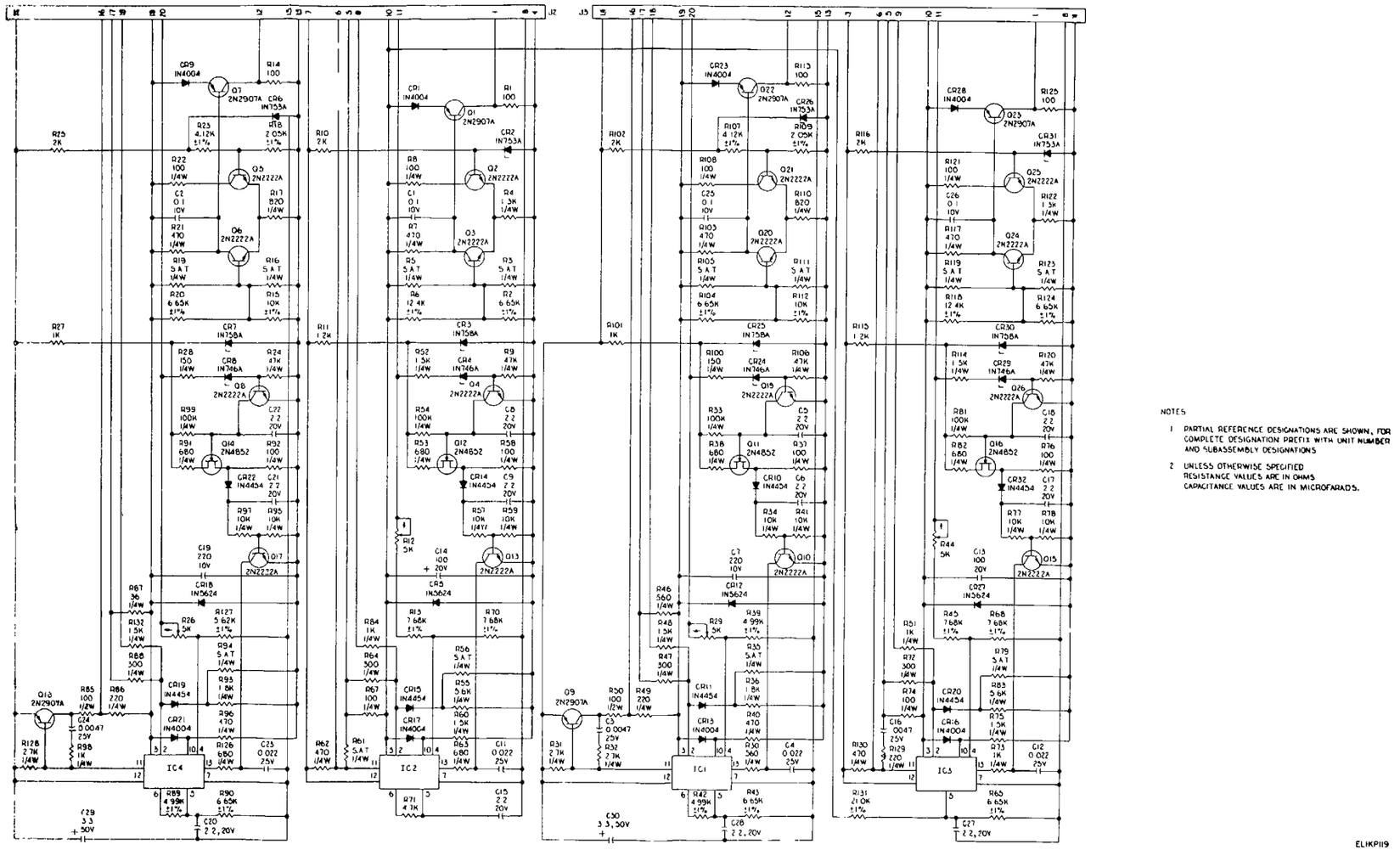


Figure FO-58. Power supply PS1 assembly A2 (SM-C-882232), schematic diagram

TEAR ALONG PERFORATED LINE

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

SOMETHING WRONG WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)

DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE

BE EXACT. . .PIN-POINT WHERE IT IS

PAGE NO.	PARA-GRAPH	FIGURE NO	TABLE NO.

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

PRINTED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER	SIGN HERE:

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ▸ ARE OBSOLETE.

P.S.—IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.